DATA SHEET

P82B96
Dual bi-directional bus buffer

Product specification

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IC12 Data Handbook

Philips
Semiconductors

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Dual bi-directional bus buffer P82B96

FEATURES

- Dual Interface handles both SCL and SDA signals
- Bi-directional data transfer
- Splits I^2C signal into forward/reverse Tx, Ty, Rx and Ry signals
- Low power supply current.
- Wide supply voltage range (I^2C logic levels at Sx Sy independent of IC supply voltage).
- Inhibits data transfer (releases bus) if supply fails.
- Supports 100 kHz clock speed on short busses.

TYPICAL INTERFACES

- Provides interface between I^2C busses operating at different logic levels (e.g., 5V and 3V)
- Provides interface between I^2C and SMB (350 μA) bus standard.
- Simple conversion of I^2C SDA or SCL signals to multi-drop differential bus hardware, e.g., via compatible PCA82C250.
- Interfaces with Opto-couplers to provide Opto isolation between I^2C bus nodes.

DESCRIPTION

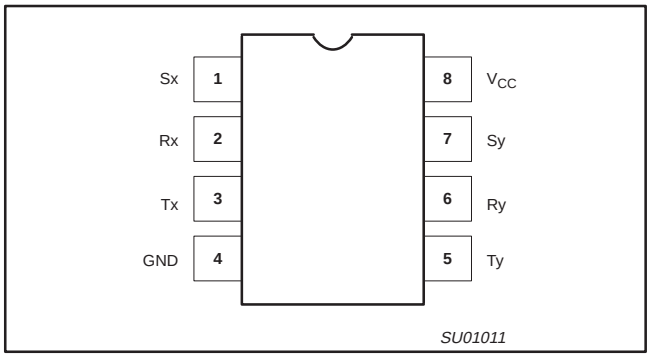
The P82B96 is a bipolar IC which creates a non-latching, bi-directional, logic interface between the normal I^2C bus and a range of other bus configurations. It can interface I^2C bus logic signals to similar busses having different voltage and current levels.

For example it can interface to the 350 μA SMB bus, to 3.3 V logic devices, and to 15 V levels and/or low impedance lines to improve noise immunity on longer bus lengths.

It achieves this interface without any restrictions on the normal I^2C protocols or 100 kHz clock speed. The IC adds minimal loading to the I^2C node, and loadings of the new bus or remote I^2C nodes are not transmitted or transformed to the local node. Restrictions on the number of I^2C devices in a system, or the physical separation between them, are virtually eliminated. Transmitting SDA/SCL signals via balanced transmission lines (twisted pairs) or with galvanic isolation (opto-coupling) is simple because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be directly connected, without causing latching, to provide an alternative bi-directional signal line with I^2C properties.

PIN CONFIGURATIONS

8-pin dual in-line or SO



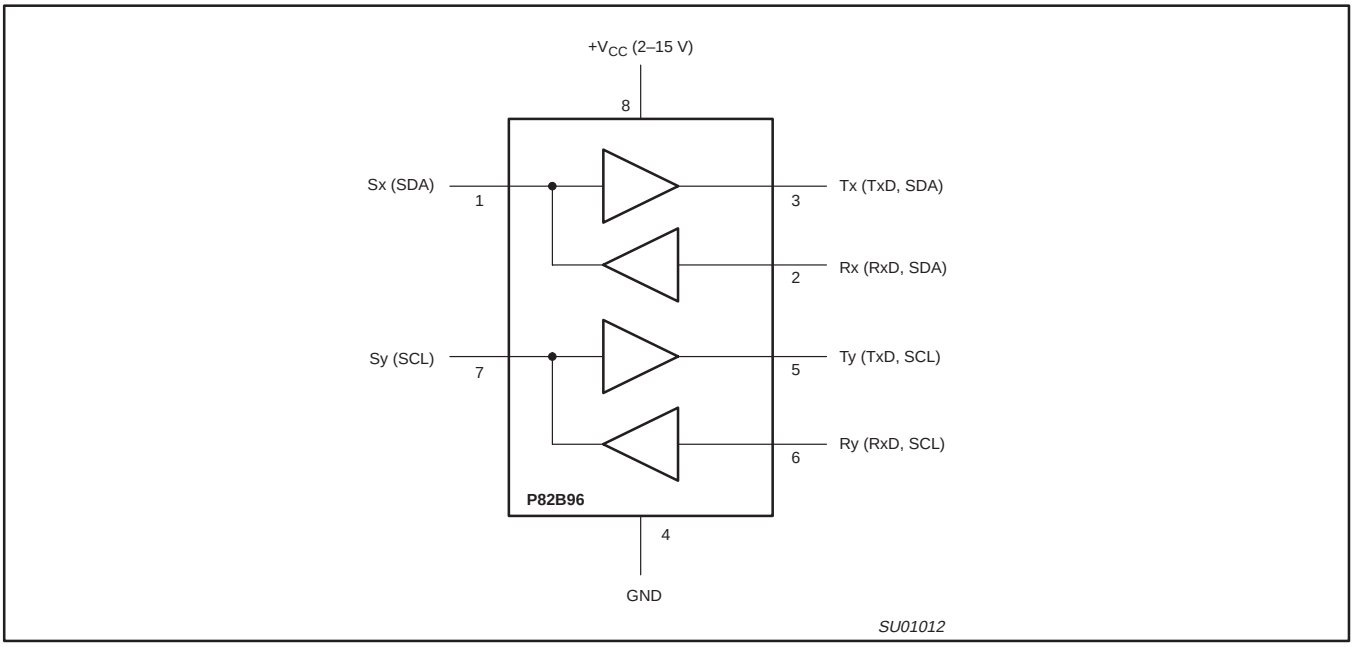
PINNING

SYMBOL	PIN	DESCRIPTION
Sx	1	I^2C Bus (SDA or SCL)
Rx	2	Receive signal
Tx	3	Transmit signal
GND	4	Negative Supply
Ty	5	Transmit signal
Ry	6	Receive signal
Sy	7	I^2C Bus (SDA or SCL)
V_{CC}	8	Positive supply

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
P82B96PN	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97–1
P82B96TD	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96–1

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The P82B96 has two identical buffers allowing buffering of both of the I^2C (SDA and SCL) signals. Each buffer is made up of two logic signal paths, a forward path from the I^2C interface pin which drives the buffered bus, and a reverse signal path from the buffered bus input to drive the I^2C bus interface.

Thus these paths are:

1. Sense the voltage state of the I^2C pin Sx (or Sy) and transmit this state to the pin Tx (Ty resp.), and
2. Sense the state of the pin Rx (Ry) and pull the I^2C pin low whenever Rx (Ry) is low.

The rest of this discussion will address only the “x” side of the buffer: the “y” side is identical.

The I^2C pin (Sx) is designed to interface with a normal I^2C bus.

The logic threshold voltage levels on the I^2C bus are independent of the IC supply V_{CC} The maximum I^2C bus supply voltage is 15 V and the guaranteed static sink current is 3 mA.

The logic level of Rx is determined from the power supply voltage V_{CC} of the chip. Logic LOW is below 42 % of V_{CC} and logic HIGH is above 58 % of V_{CC}: with a typical switching threshold of half V_{CC}.

Tx is an open collector output without ESD protection diodes to V_{CC}. It may be connected via a pull-up resistor to a supply voltage in excess of $V_{CC,}$ as long as the 15 V rating is not exceeded. It has a larger current sinking capability than a normal I^2C device, being able to sink a static current of greater than 30 mA, and typical 100 mA dynamic pull-down capability as well.

A logic LOW is only transmitted to Tx when the voltage at the I^2C pin (Sx) is below 0.6 V. A logic LOW at Rx will cause the I^2C bus (Sx) to be pulled to a logic LOW level in accordance with I^2C requirements (max. 1.5 V in 5 V applications) but not low enough to be looped back to the Tx output and cause the buffer to latch low.

The minimum LOW level this chip can achieve on the I^2C bus by a LOW at Rx is typically 0.8 V.

If the supply voltage V_{cc} fails then neither the I^2C nor the Tx output will be held low. Their open collector configuration allows them to be pulled up to the rated maximum of 15 V even without V_{CC} present. The input configuration on Sx and Rx also present no loading of external signals even when V_{CC} is not present.

MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages with respect to pin GND (pin 4).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC} to GND	Supply voltage range V_{CC}	-0.3	+18	V
V_{bus}	Voltage range on I^2C Bus, SDA or SCL	-0.3	+18	V
V_{Tx}	Voltage range on buffered output	-0.3	+18	V
V_{Rx}	Voltage range on receive input	-0.3	+18	V
I	DC current (any pin)		250	mA
R_{tot}	Power dissipation		300	mW
T_{stg}	Storage temperature range	-55	+125	°C
T_{amb}	Operating ambient temperature range	-40	+85	°C

CHARACTERISTICS

At T_{amb} = 25°C; Voltages are specified with respect to GND with V_{CC} = 5 V unless otherwise stated.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Power Supply					
V_{CC}	Supply voltage (operating)	2.0	—	15	V
I_{CC}	Supply current, busses HIGH	—	0.9	1.8	mA
I_{CC}	Supply current at V_{CC} = 15V, busses HIGH	—	1.1	2.5	mA
I_{CC}	Additional supply current per Tx or Ty LOW	—	1.7	3.5	mA
Bus pull-up (load) voltages and currents					
V_{Sx}, V_{Sy}	Maximum input/output voltage level Open collector I^2C bus and V_{Rx}, V_{Ry} = HIGH	—	—	15	V
I_{Sx}, I_{Sy}	Static output loading on I^2C bus V_{Sx}, V_{Sy} = 1.2 V V_{Rx}, V_{Ry} = LOW	0.2	—	3	mA
I_{Sx}, I_{Sy}	Dynamic output sink capability on I^2C bus V_{Sx}, V_{Sy} > 2 V V_{Rx}, V_{Ry} = LOW	7	18	—	mA
I_{Sx}, I_{Sy}	Leakage current on I^2C bus V_{Sx}, V_{Sy} = 5 V, and V_{Rx}, V_{Ry} = HIGH	—	—	1	μA
I_{Sx}, I_{Sy}	Leakage current on I^2C bus V_{Sx}, V_{Sy} = 15 V, and V_{Rx}, V_{Ry} = HIGH	—	1	—	μA
V_{Tx}, V_{Ty}	Maximum output voltage level Open collector	—	—	15	V
I_{Tx}, I_{Ty}	Static output loading on buffered bus V_{Tx}, V_{Ty} = 0.4 V V_{Sx}, V_{Sy} = LOW on I^2C bus = 0.4V	—	—	30	mA
I_{Tx}, I_{Ty}	Dynamic output sink capability, buffered bus: V_{Tx}, V_{Ty} > 1 V V_{Sx}, V_{Sy} = LOW on I^2C bus = 0.4V	60	100	—	mA
I_{Tx}, I_{Ty}	Leakage current on buffered bus V_{Tx}, V_{Ty} = V_{CC} = 15 V, and V_{Sx}, V_{Sy} = HIGH	—	1	—	μA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Input Currents					
I_{Sx}, I_{Sy}	Input current from I^2C bus, bus LOW V_{Rx}, V_{Ry} = HIGH	—	-1	—	μA
I_{Rx}, I_{Ry}	Input current from buffered bus, bus LOW V_{Rx}, V_{Ry} = 0.4 V	—	-1	—	μA
I_{Rx}, I_{Ry}	Leakage current on buffered bus input V_{Rx}, V_{Ry} = V_{CC}	—	1	—	μA
Input Thresholds					
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I^2C bus I_{Sx}, I_{Sy} = 3 mA	0.8	0.9	1.0	V
V_{Sx}, V_{Sy}	Output logic level LOW, on normal I^2C bus I_{Sx}, I_{Sy} = 0.2 mA	—	750	—	mV
V_{Sx}, V_{Sy}	Input logic level LOW threshold On normal I^2C bus	600	650	—	mV
dV_{Sx}/dT, dV_{Sy}/dT	Temperature coefficient of thresholds	—	-2	—	mV/K
V_{Rx}, V_{Ry}	Input logic HIGH level Fraction of applied V_{CC}	0.58	—	—	
V_{Rx}, V_{Ry}	Input threshold Fraction of applied V_{CC}	—	0.5	—	
V_{Rx}, V_{Ry}	Input logic LOW level Fraction of applied V_{CC}	—	—	0.42	
Bus Release on V_{CC} Failure					
V_{Sx}, V_{Sy}, V_{Tx}, V_{Ty}	V_{CC} voltage at which all busses are guaranteed to be released	—	—	1	V
dV/dT	Temperature coefficient of guaranteed release voltage	—	-4	—	mV/K
Buffer response time					
$T_{fall\ delay}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on FALLING input between V_{Sx} = input switching threshold: and V_{Tx} output falling 50%. R_{Tx} pull up = 160 Ω, no capacitive load, V_{CC} = 5 V	—	100	—	ns
$T_{rise\ delay}$ V_{Sx} to V_{Tx} V_{Sy} to V_{Ty}	Buffer time delay on RISING input between V_{Sx} = input switching threshold, and V_{Tx} output reaching 50%. R_{Tx} pull up = 160 Ω, no capacitive load, V_{CC} = 5 V	—	100	—	ns
$T_{fall\ delay}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on FALLING input between V_{Rx} = input switching threshold, and V_{Sx} output falling 50%. R_{Sx} pull up = 1600 Ω, no capacitive load, V_{CC} = 5 V	—	300	—	ns
$T_{rise\ delay}$ V_{Rx} to V_{Sx} V_{Ry} to V_{Sy}	Buffer time delay on RISING input between V_{Rx} = input switching threshold, and V_{Sx} output reaching 50%. R_{Sx} pull up = 1600 Ω, no capacitive load, V_{CC} = 5 V	—	300	—	ns

TYPICAL APPLICATIONS

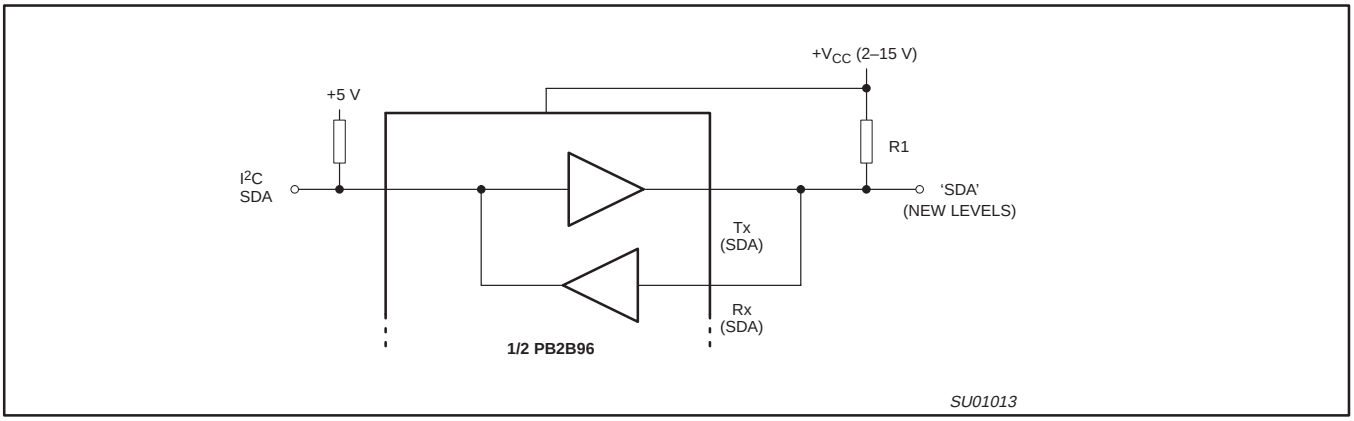


Figure 1. Interfacing an 'I^{2}C' type of bus with different logic levels.

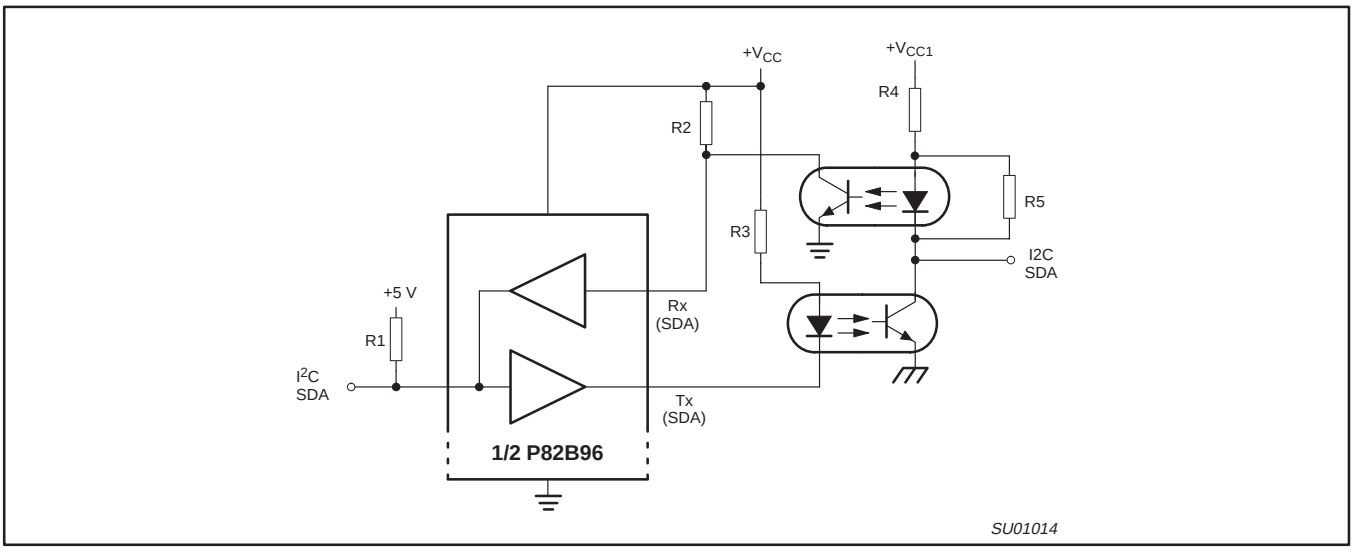
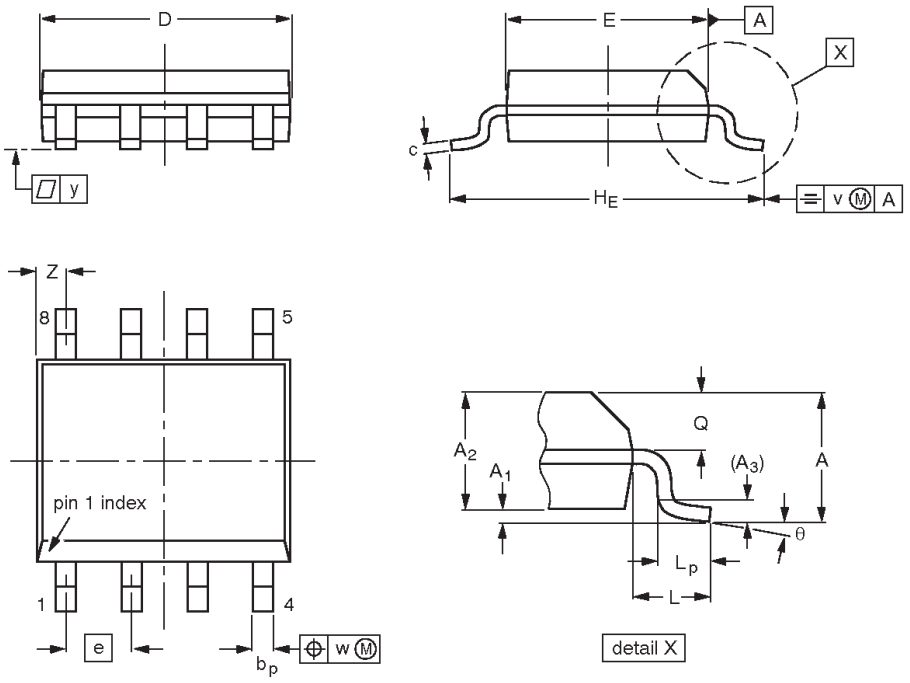
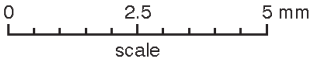


Figure 2. Galvanic isolation of I^{2}C nodes via opto-couplers

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

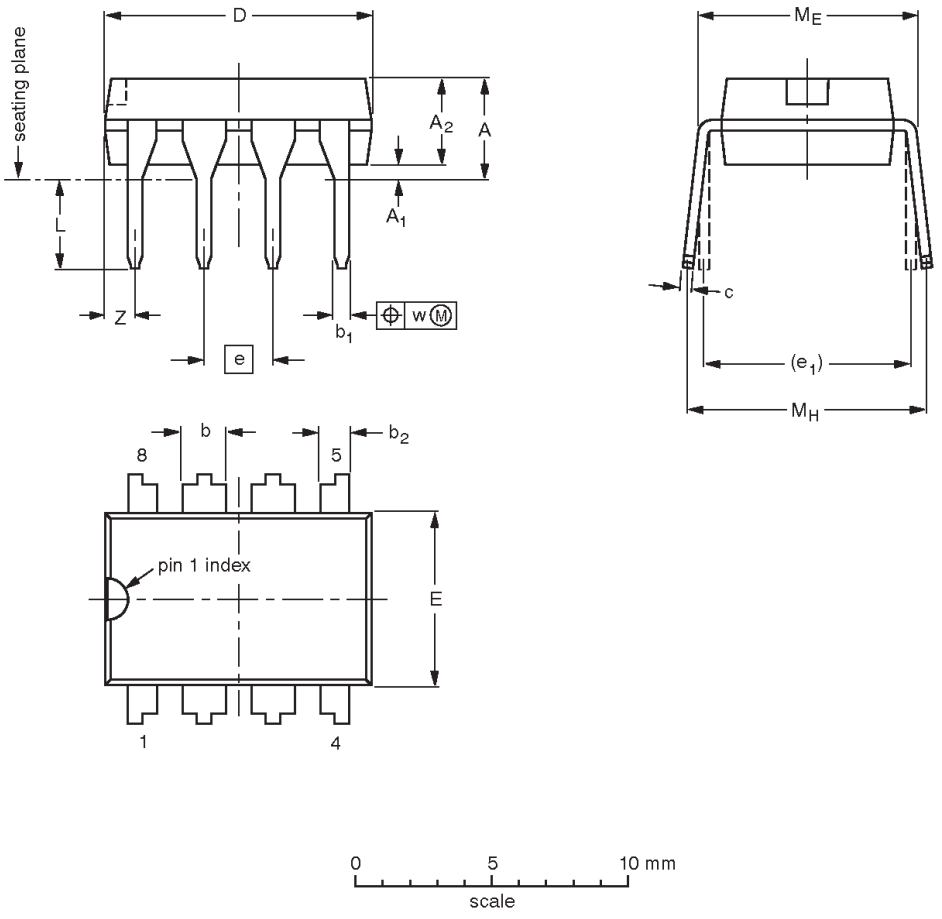
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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