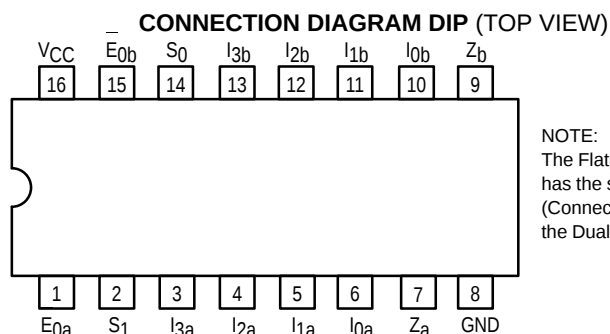




DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (E_0) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects



PIN NAMES

S_0, S_1 Common Select Inputs

Multiplexer A

E_{0a} Output Enable (Active LOW) Input

$I_{0a}-I_{3a}$ Multiplexer Inputs

Z_a Multiplexer Output (Note b)

Multiplexer B

E_{0b} Output Enable (Active LOW) Input

$I_{0b}-I_{3b}$ Multiplexer Inputs

Z_b Multiplexer Output (Note b)

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

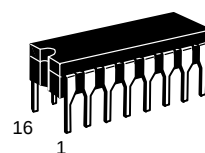
LOADING (Note a)

	HIGH	LOW
S_0, S_1	0.5 U.L.	0.25 U.L.
E_{0a}	0.5 U.L.	0.25 U.L.
$I_{0a}-I_{3a}$	0.5 U.L.	0.25 U.L.
Z_a	65 (25) U.L.	15 (7.5) U.L.
E_{0b}	0.5 U.L.	0.25 U.L.
$I_{0b}-I_{3b}$	0.5 U.L.	0.25 U.L.
Z_b	65 (25) U.L.	15 (7.5) U.L.

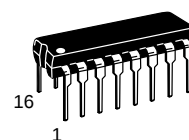
SN54/74LS253

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

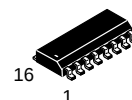
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

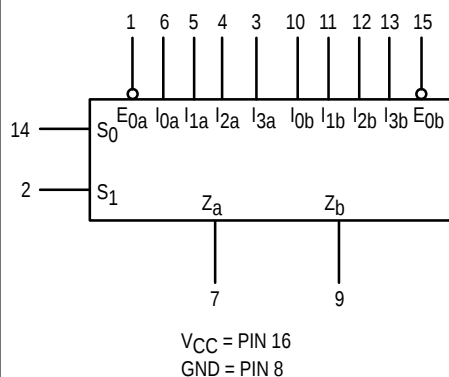


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

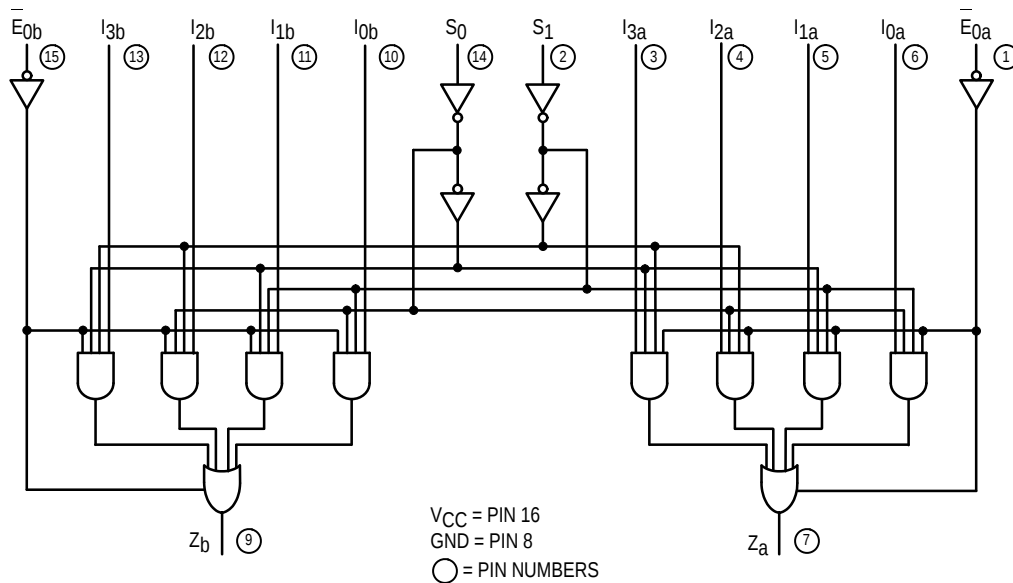
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXD SOIC

LOGIC SYMBOL



SN54/74LS253

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable (E_{0a} , E_{0b}) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.

The LS253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \bar{E}_{0a} \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_{0b} \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	E_0	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level

L = LOW Level

X = Irrelevant

(Z) = High Impedance (off)

Address inputs S_0 and S_1 are common to both sections.

SN54/74LS253

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW				−20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				−0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				12	mA	V _{CC} = MAX, V _E = 0 V	
					14	mA	V _{CC} = MAX, V _E = 4.5 V	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V) See SN54LS251 for Waveforms

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay, Data to Output			17 13	25 20	ns	Figure 1	C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Select to Output			30 21	45 32	ns	Figure 1	
t _{PZH} t _{PZL}	Output Enable Time			15 15	28 23	ns	Figures 4, 5	
t _{PHZ} t _{PLZ}	Output Disable Time			27 18	41 27	ns	Figures 3, 5	C _L = 5.0 pF, R _L = 667 Ω