

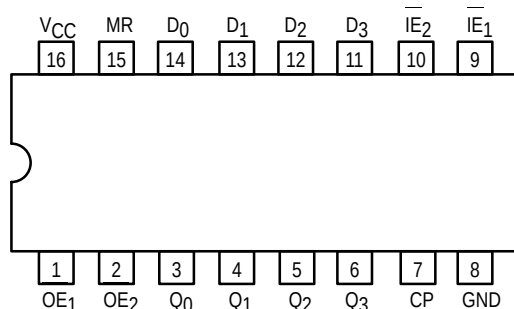


4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines ($\overline{IE}_1$, $\overline{IE}_2$). A HIGH on either Output Enable line ($\overline{OE}_1$, $\overline{OE}_2$) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset ($\overline{MR}$) input resets the Register regardless of the state of the Clock (CP), the Output Enable ($\overline{OE}_1$, $\overline{OE}_2$) or the Input Enable ($\overline{IE}_1$, $\overline{IE}_2$) lines.

- Fully Edge-Triggered
- 3-State Outputs
- Gated Input and Output Enables
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In-Line Package.

PIN NAMES

D_0-D_3	Data Inputs
$\overline{IE}_1-\overline{IE}_2$	Input Enable (Active LOW)
$\overline{OE}_1-\overline{OE}_2$	Output Enable (Active LOW) Inputs
CP	Clock Pulse (Active HIGH Going Edge)
	Input
MR	Master Reset Input (Active HIGH)
Q_0-Q_3	Outputs (Note b)

NOTES:

- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

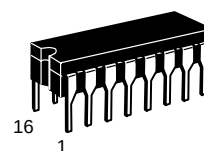
LOADING (Note a)

	HIGH	LOW
D_0-D_3	0.5 U.L.	0.25 U.L.
$\overline{IE}_1-\overline{IE}_2$	0.5 U.L.	0.25 U.L.
$\overline{OE}_1-\overline{OE}_2$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q_0-Q_3	65 (25) U.L.	15 (7.5) U.L.

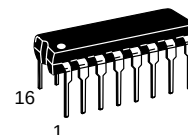
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4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

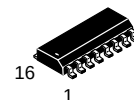
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

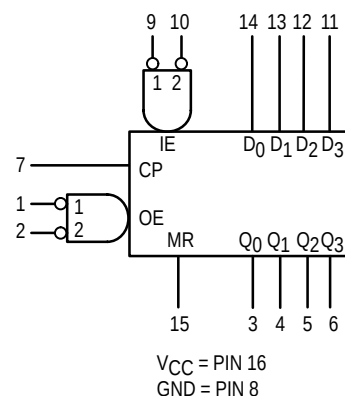


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

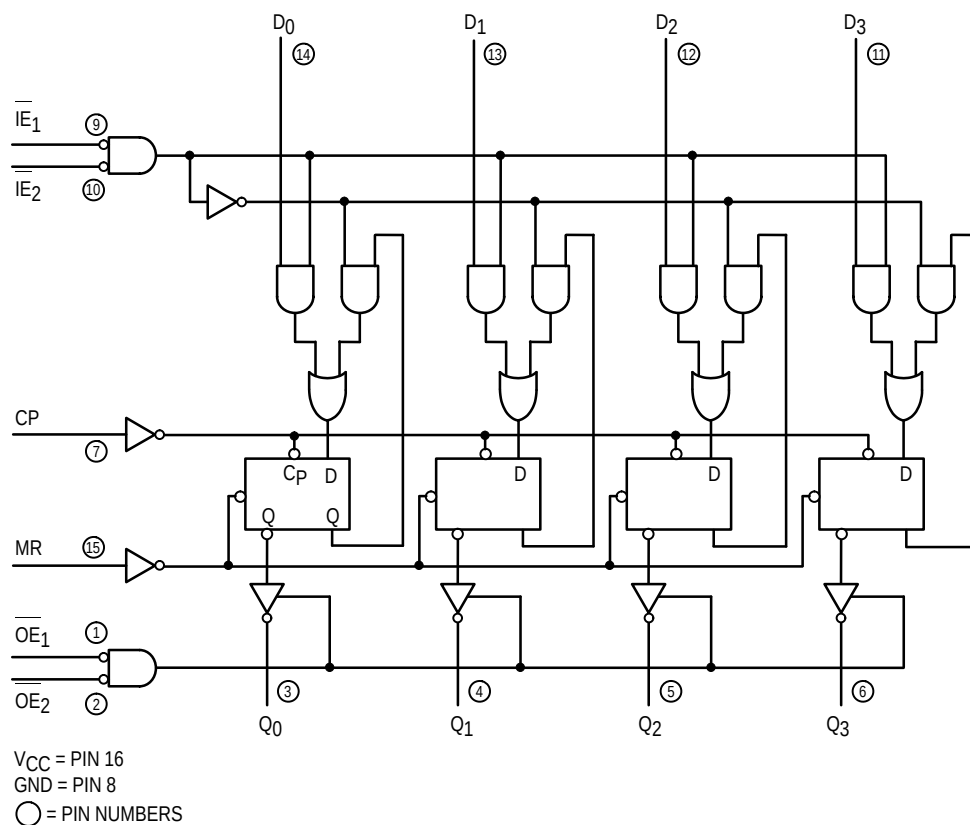
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS173A

LOGIC DIAGRAM



TRUTH TABLE

MR	CP	IE ₁	IE ₂	D _n	Q _n
H	X	X	X	X	L
L	L	X	X	X	Q _n
L	↗	H	X	X	Q _n
L	↘	X	H	X	Q _n
L	↗	L	L	L	L
L	↘	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

When either OE₁, or OE₂ are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _O = 2.7 V	
I _{OZL}	Output Off Current LOW				−20	μA	V _{CC} = MAX, V _O = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				−0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				30	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
f_{MAX}	Maximum Input Clock Frequency		30	50		MHz	$V_{CC} = 5.0 \text{ V}$ $C_L = 45 \text{ pF}$, $R_L = 667 \Omega$	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			17 22	25 30	ns		
t_{PHL}	Propagation Delay, MR to Output			26	35	ns		
t_{PZH} t_{PZL}	Output Enable Time			15 18	23 27	ns		
t_{PLZ} t_{PHZ}	Output Disable Time			11 11	17 17	ns	$C_L = 5.0 \text{ pF}$, $R_L = 667 \Omega$	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t_W	Clock or MR Pulse Width		20			ns	$V_{CC} = 5.0 \text{ V}$	
t_S	Data Enable Setup Time		35			ns		
t_S	Data Setup Time		17			ns		
t_h	Hold Time, Any Input		0			ns		
t_{rec}	Recovery Time		10			ns		

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AC WAVEFORMS

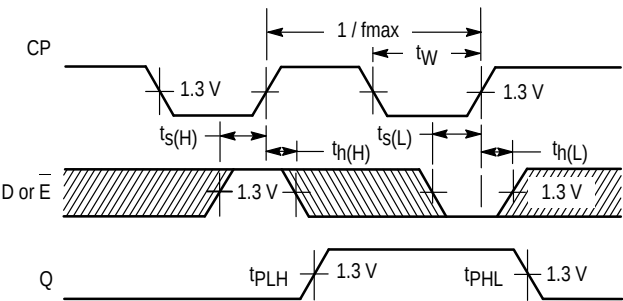


Figure 1

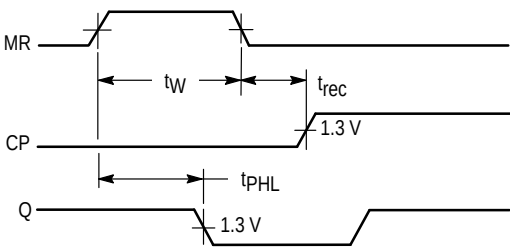


Figure 2

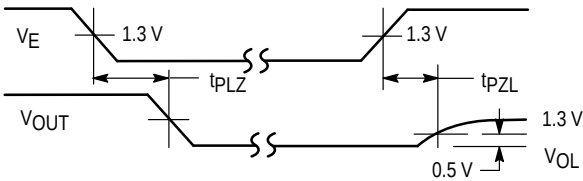


Figure 3

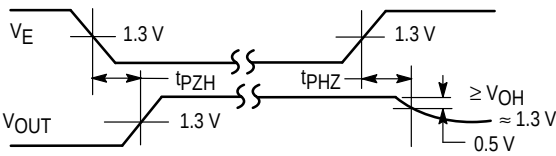
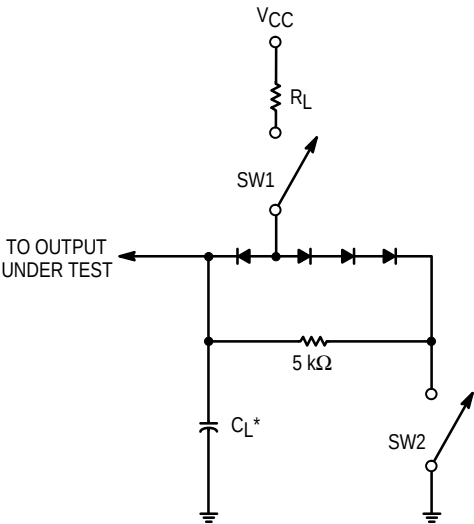


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed