Product Preview

TMOS E-FET™
High Energy Power FET
P–Channel Enhancement–Mode Silicon Gate

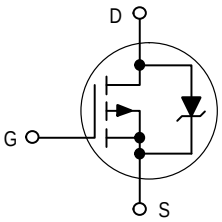
MTD1P50E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
500 VOLTS
15 Ω

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



CASE 369A–13, Style 2
DPAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 4.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_C = 25°C, when mounted to minimum recommended pad size	P_D	50 0.4 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.5 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

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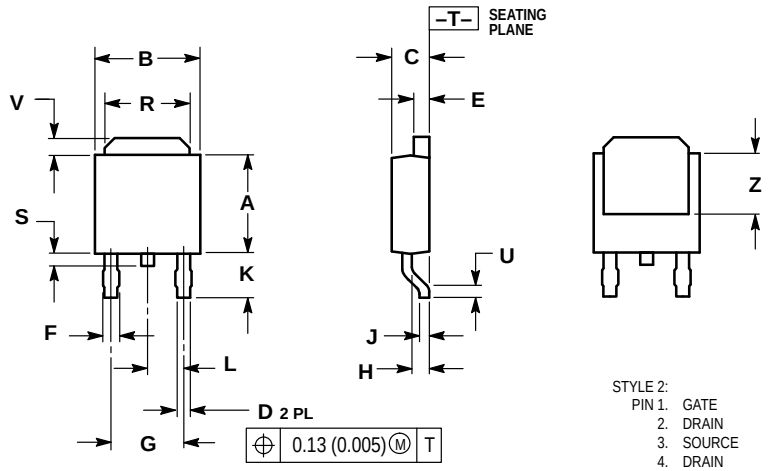
Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— TBD	— —	Vdc V/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.1 TBD	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	12	15	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	18 15.8	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.4	0.6	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	TBD	TBD	pF
Output Capacitance		C_{oss}	—	TBD	TBD	
Transfer Capacitance		C_{rss}	—	TBD	TBD	
SWITCHING CHARACTERISTICS*						
Turn–On Delay Time	(V_{DS} = 250 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	TBD	TBD	ns
Rise Time		t_r	—	TBD	TBD	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	TBD	
Fall Time		t_f	—	TBD	TBD	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	TBD	TBD	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	
		Q_3	—	TBD	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) (I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	2.0 TBD	3.5 —	Vdc
Reverse Recovery Time	(I_S = 1.0 Adc, dI_S/dt = 100 A/μs)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	μC

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

CASE 369A–13
ISSUE W

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