

Product Preview

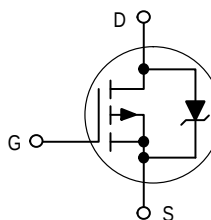
TMOS E-FET™

High Energy Power FET

P-Channel Enhancement-Mode Silicon Gate

This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor—Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



MTD1P50E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
500 VOLTS
15 Ω



CASE 369A-13, Style 2
DPAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	500	Vdc
Drain-to-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	500	Vdc
Gate-to-Source Voltage — Continuous	V _{GS}	±20	Vdc
— Single Pulse (t _p ≤ 50 μs)	V _{GSM}	±40	
Drain Current — Continuous @ T _C = 25°C	I _D	1.0	Adc
— Continuous @ T _C = 100°C	I _D	0.8	
— Single Pulse (t _p ≤ 10 μs)	I _{DM}	4.0	Apk
Total Power Dissipation @ T _C = 25°C	P _D	50	Watts
Derate above 25°C		0.4	W/°C
Total Power Dissipation @ T _C = 25°C, when mounted to minimum recommended pad size		1.75	Watts
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — Starting T _J = 25°C (V _{DD} = 100 Vdc, V _{GS} = 10 Vdc, Peak I _L = 3.0 Apk, L = 10 mH, R _G = 25 Ω)	E _{AS}	45	mJ
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THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	R _{θJC}	2.5	°C/W
— Junction to Ambient	R _{θJA}	100	
— Junction to Ambient (1)	R _{θJA}	71.4	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T _L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

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Thermal Clad is a trademark of the Bergquist Company.

Preferred devices are Motorola recommended choices for future use and best overall value.

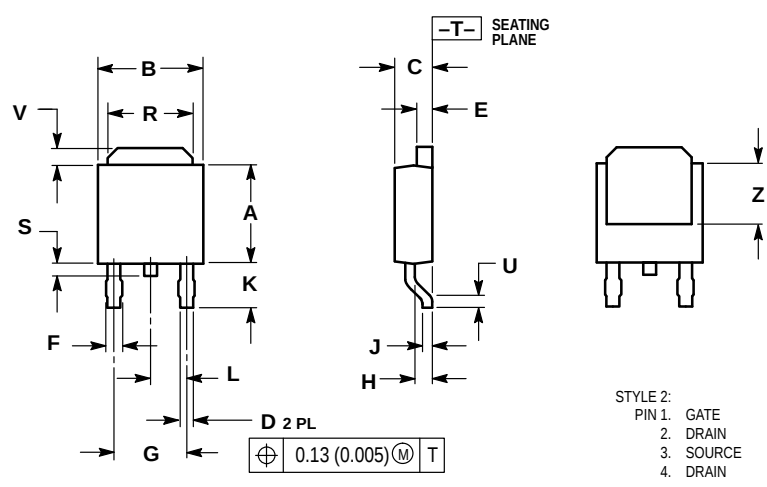
MTD1P50E

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 0.25 mAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	500 —	— TBD	— —	Vdc V/°C	
Zero Gate Voltage Drain Current (V _{DS} = 500 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 500 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	— —	— —	10 100	μAdc	
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0)	I _{GSS}	—	—	100	nAdc	
ON CHARACTERISTICS*						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 —	3.1 TBD	4.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 0.5 Adc)	R _{DS(on)}	—	12	15	Ohms	
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 1.0 Adc) (I _D = 0.5 Adc, T _J = 125°C)	V _{DS(on)}	— —	— —	18 15.8	Vdc	
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 0.5 Adc)	g _{FS}	0.4	0.6	—	mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	TBD	pF	
Output Capacitance		C _{oss}	—	TBD		
Transfer Capacitance		C _{rss}	—	TBD		
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V _{DS} = 250 Vdc, I _D = 1.0 Adc, V _{GS} = 10 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	TBD	ns	
Rise Time		t _r	—	TBD		
Turn-Off Delay Time		t _{d(off)}	—	TBD		
Fall Time		t _f	—	TBD		
Gate Charge	(V _{DS} = 400 Vdc, I _D = 1.0 Adc, V _{GS} = 10 Vdc)	Q _T	—	TBD	nC	
		Q ₁	—	TBD		
		Q ₂	—	TBD		
		Q ₃	—	TBD		
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I _S = 1.0 Adc, V _{GS} = 0 Vdc) (I _S = 1.0 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	— —	2.0 TBD	3.5 —	Vdc
Reverse Recovery Time	(I _S = 1.0 Adc, dI _S /dt = 100 A/μs)	t _{rr}	—	TBD	—	ns
		t _a	—	TBD	—	
		t _b	—	TBD	—	
Reverse Recovery Stored Charge		Q _{RR}	—	TBD	—	μC

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS



- NOTES:
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

CASE 369A-13
ISSUE W

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