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MOTOROLA

MC33349

Lithium Battery Protection Circuit for One Cell Battery Packs

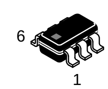
The MC33349 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of a one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection, and a low current standby mode when the cell is discharged. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection
- Low Current Standby Mode when Cells are Discharged
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in a Low Profile Surface Mount Package

Ordering Information shown on following page.

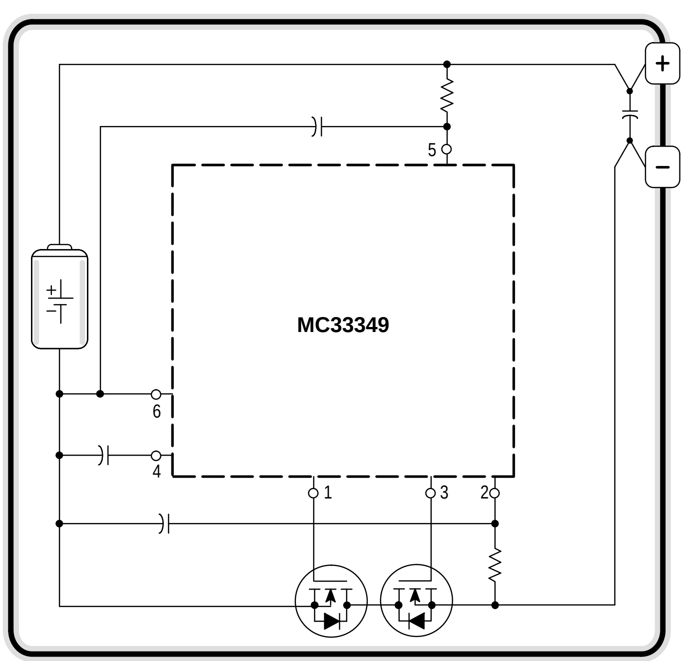
LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA

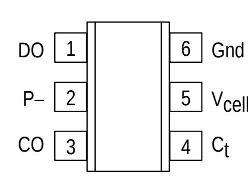


N SUFFIX
PLASTIC PACKAGE
CASE 1262
(SOT–23)

Typical One Cell Smart Battery Pack



PIN CONNECTIONS



 Rev 0

ORDERING INFORMATION

Device	Overvoltage Threshold (V)	Undervoltage Threshold (V)	Current Limit Threshold (V)	Marking	Reel Size	Tape width	Quantity
MC33349N–3R1	4.25	2.5	0.2	A1xx*	7”	8 mm	3000
MC33349N–4R1	4.25	2.5	0.075	A2xx*			
MC33349N–7R1	4.35	2.5	0.2	A0xx*			

* ″xx″ denotes the date code marking.
Consult factory for information on other threshold values.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (Pin 5 to Pin 6)	V_{DD}	–0.3 to 12	V
Input Voltage			
P– Pin Voltage (Pin 5 to Pin 2)	V_{P-}	V_{DD} – 28 to V_{DD} + 0.3	V
Ct Pin (Pin 4 to Pin 6)	V_{Ct}	Gnd – 0.3 to V_{DD} + 0.3	V
Output Voltage			
CO Pin Voltage (Pin 3 to Pin 2)	V_{CO}	V_{DD} – 28 to V_{DD} + 0.3	V
DO Pin Voltage (Pin 1 to Pin 6)	V_{DO}	Gnd – 0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	150	mW
Operating Junction Temperature	T_J	–40 to 85	°C
Storage Temperature	T_{stg}	–55 to 125	°C

ELECTRICAL CHARACTERISTICS (C_t = 0.01 µF, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit	Note[1]
VOLTAGE SENSING						
Cell Charging Cutoff (Pin 5 to Pin 6)						
Overvoltage Threshold, V_{Cell} Increasing	V_{DET1}					B
–3, –4 Suffix		4.2	4.25	4.3	V	
–7 Suffix		4.3	4.35	4.4	V	
Overvoltage Hysteresis V_{Cell} Decreasing	V_{HYS1}	150	200	250	mV	B
Cell Discharging Cutoff (Pin 5 to Pin 6)						C
Undervoltage Threshold, V_{Cell} Decreasing	V_{DET2}	2.437	2.5	2.563	V	
Overvoltage Delay Time (C_t = 0.01 µF, V_{cell} = 3.6V to 4.5 V)	$t_{(DET1)}$	55	80	105	ms	B
Undervoltage Delay Time	$t_{(DET2)}$	7.0	10	13	ms	C
CURRENT SENSING						
Excess Current Threshold (Detect rising edge of P– pin voltage)	V_{DET3}					D
–3, –7 Suffix		170	200	230	mV	
–4 Suffix		45	75	105	mV	
Short Protection Voltage ($V_{DD} = V_{(Vcell–Gnd)}$ = 3.0V)	V_{SHORT}	V_{DD} – 1.1	V_{DD} – 0.8	V_{DD} – 0.5	V	D
Current Limit Delay Time ($V_{DD} = V_{(Vcell–Gnd)}$ = 3.0V)	$t_{(DET3)}$	9.0	13	17	ms	D
	$t_{(SHORT)}$	–	5.0	50	µs	D
Reset Resistance for Short Protection	R_{SHORT}	50	100	150	kΩ	D
OUTPUTS						
CO Nch On Voltage (I_O = 50 µA, V_{DD} = 4.4V)	V_{ol1}	–	0.2	0.5	V	E
CO Pch On Voltage (I_O = –50 µA, V_{DD} = 3.9V)	V_{oh1}	3.4	3.8	–	V	F
DO Nch On Voltage (I_O = 50 µA, V_{DD} = 2.4V)	V_{ol2}	–	0.2	0.5	V	G
DO Pch On Voltage (I_O = –50 µA, V_{DD} = 3.9V)	V_{oh2}	3.4	3.7	–	V	H
TOTAL DEVICE						
Operating Input Voltage	V_{DD}	1.5	–	10	V	A
Supply Current	I_{cell}					
Operating (V_{DD} = 3.9 V, $V_{P–}$ = 0V)		–	3.0	6.0	µA	I
Standby (V_{DD} = 2.0 V)		–	0.3	0.6	µA	I
Minimum Operating Cell Voltage for Zero Volt Charging	V_{ST}	–	–	1.2	V	A

1. Indicates test circuits shown on next page.

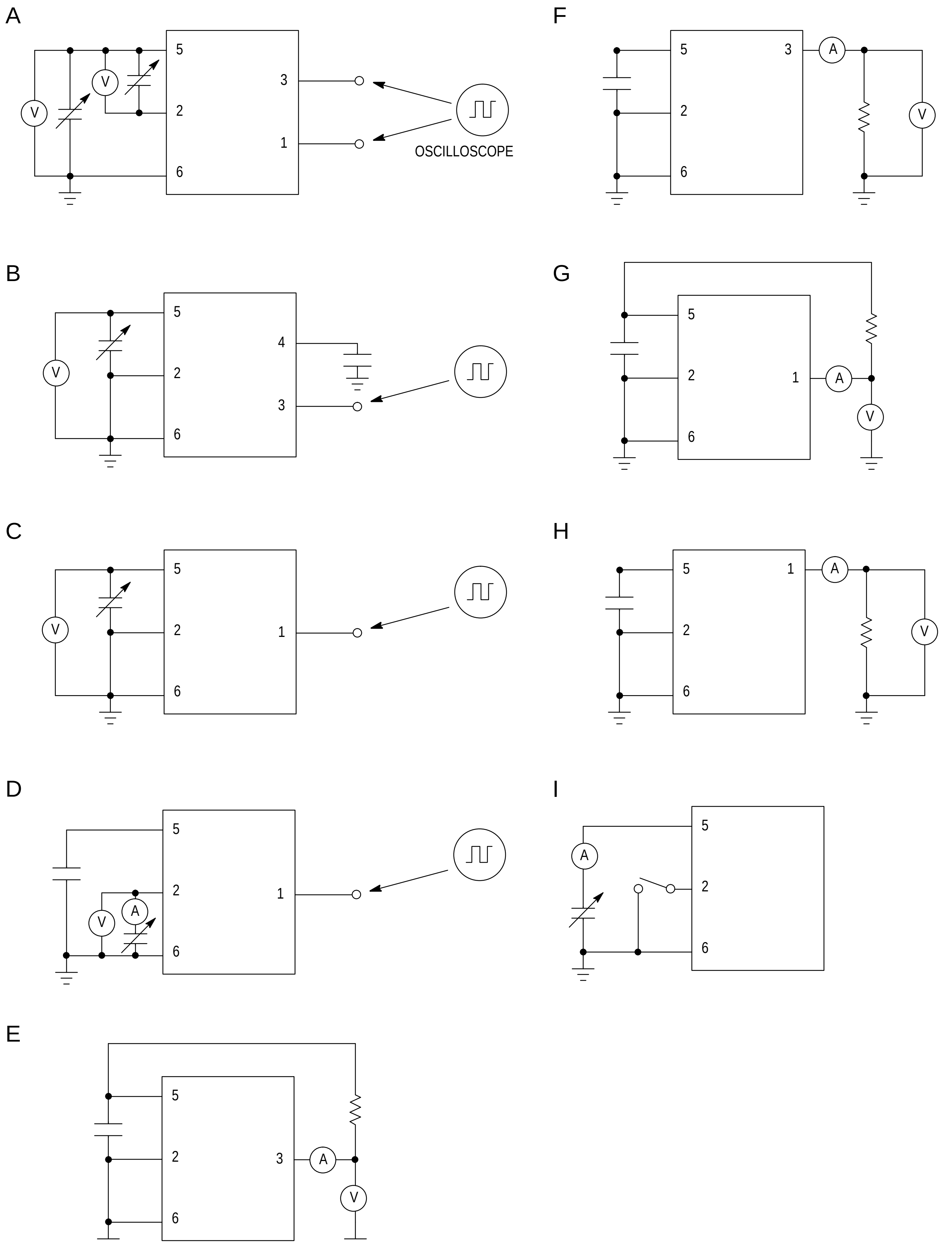


Figure 1. Test Circuit Schematics

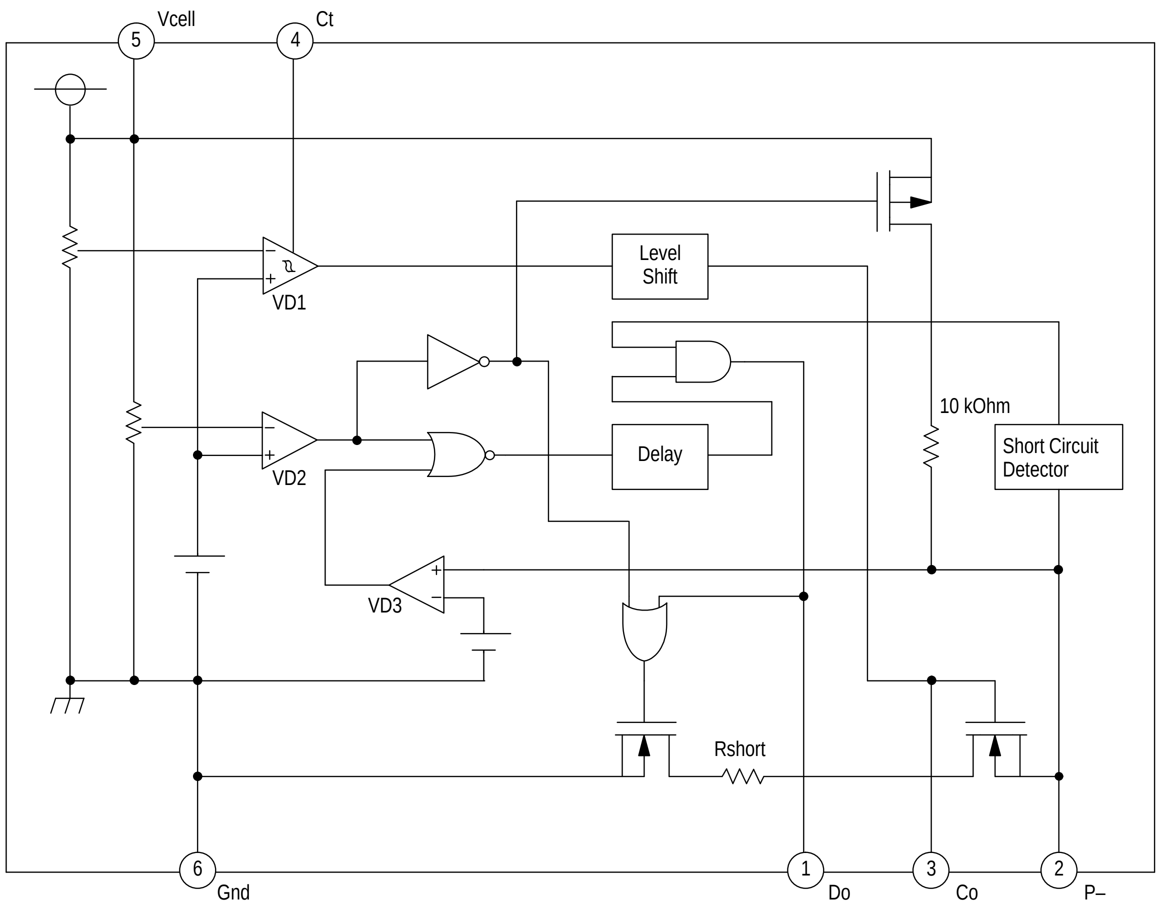


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	DO	This output connects to the gate of the discharge MOSFET allowing it to enable or disable battery pack discharging.
2	P–	This pin monitors cell discharge current. The excess current detector sets when the combined voltage drop of the charge MOSFET and the discharge MOSFET exceeds the discharge current limit threshold voltage, $V_{(DET3)}$. The short circuit detector activates when $V_{(P-)}$ is pulled within 0.8V of the cell voltage by a short circuit.
3	CO	This output connects to the gate of the charge MOSFET allowing it to enable or disable battery pack charging.
4	C_t	This pin connects to the external capacitor for setting the output delay of the overvoltage detector (VD1).
5	V_{cell}	This input connects to the positive terminal of the cell for voltage monitoring and provides operating bias for the integrated circuit.
6	Gnd	This is the ground pin of the IC.

TYPICAL CHARACTERISTICS

Figure 3. Overvoltage Threshold vs Temperature MC33349N–3X

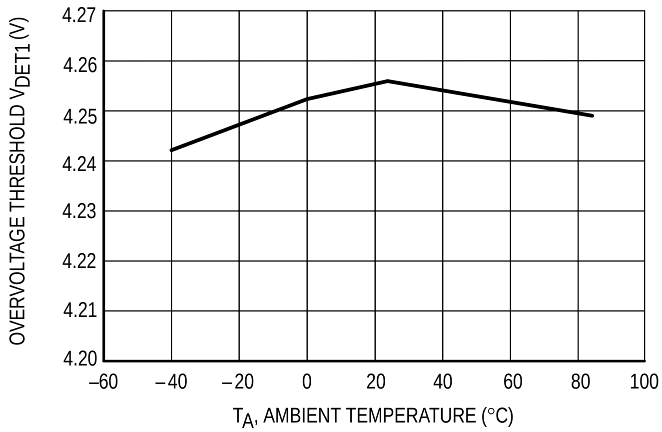


Figure 4. Undervoltage Threshold vs Temperature MC33349N–3X / MC33349N–7X

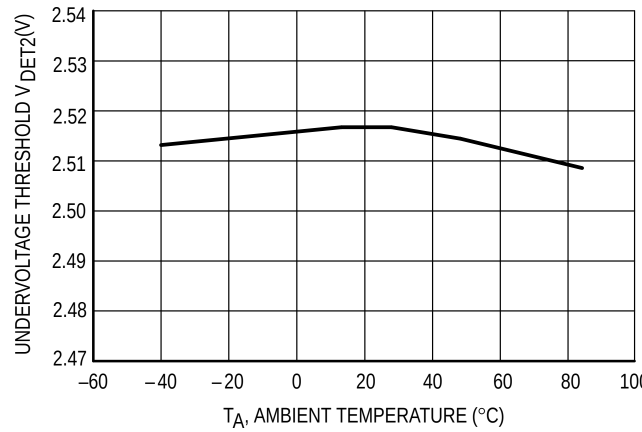


Figure 5. Excess Current Threshold vs Temperature MC33349N–3X / MC33349N–7X

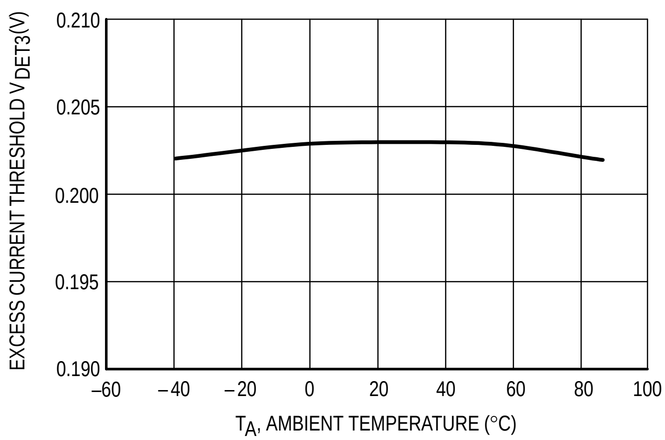


Figure 6. Short Protection Voltage vs Temperature MC33349N–3X

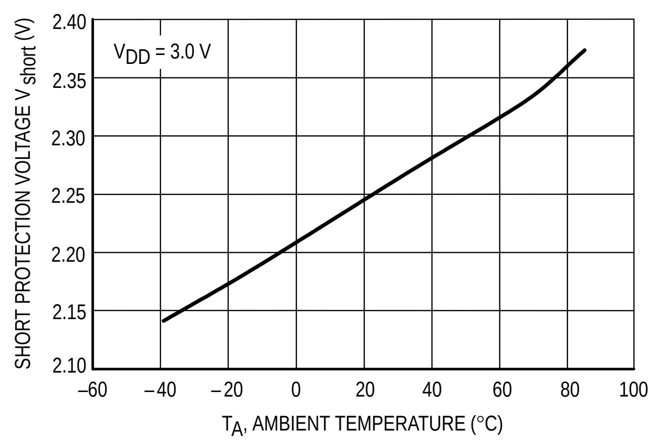


Figure 7. Output Delay of Overvoltage vs Temperature MC33349N–3X

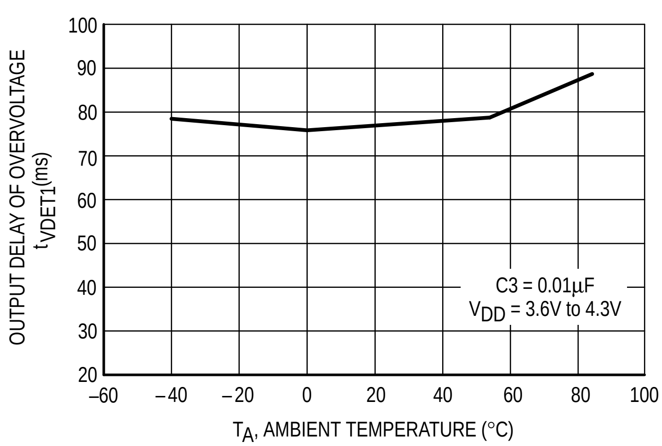


Figure 8. Output Delay of Undervoltage vs Temperature MC33349N–3X / MC33349N–7X

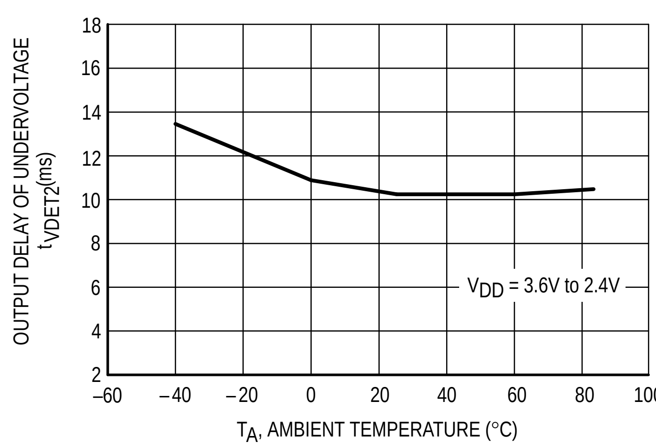


Figure 9. Output Delay of Excess Current vs Temperature MC33349N–3X

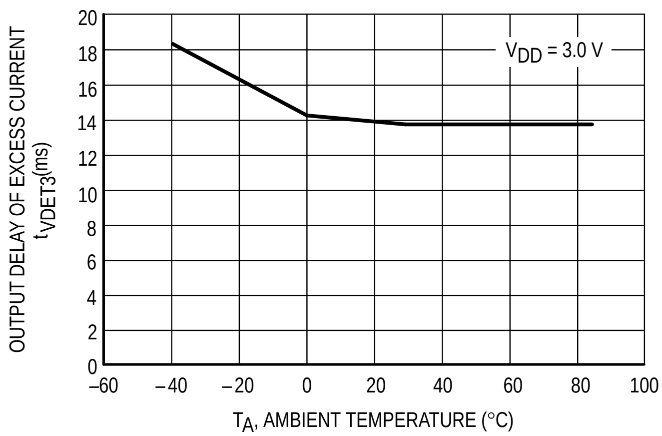


Figure 10. Output Delay of Short Circuit Detector vs Temperature MC33349N–3X

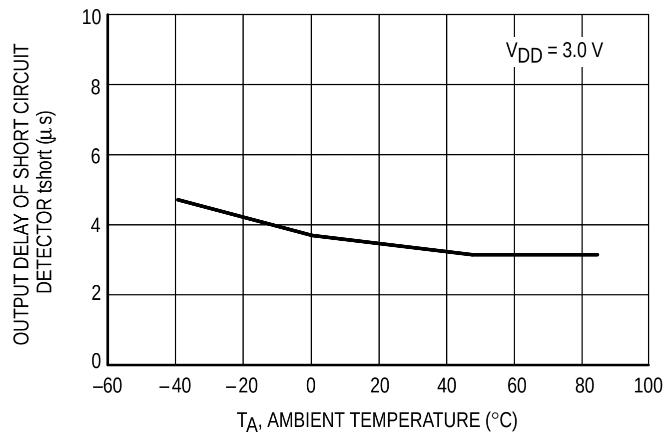


Figure 11. Overvoltage Threshold Hysteresis vs Temperature MC33349N–3X / MC33349N–7X

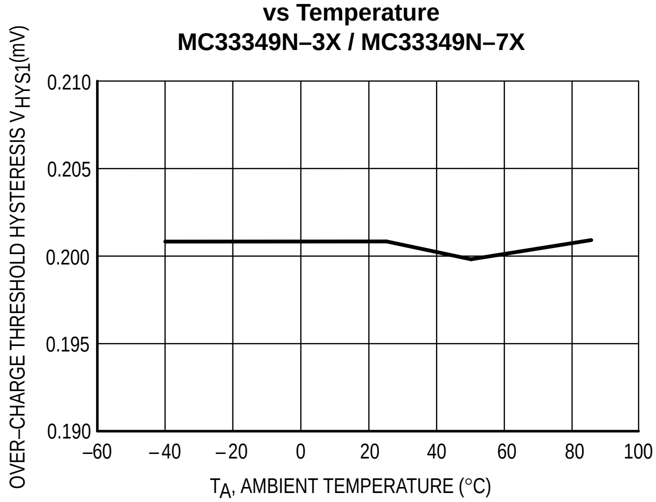


Figure 12. Operating Current vs Temperature MC33349N–3X

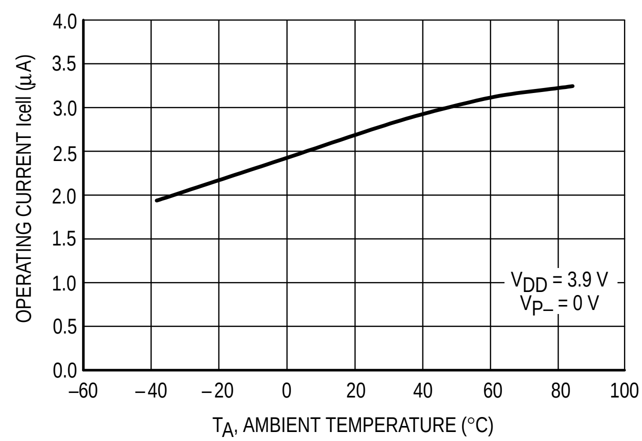


Figure 13. Standby Current vs Temperature MC33349N–3X

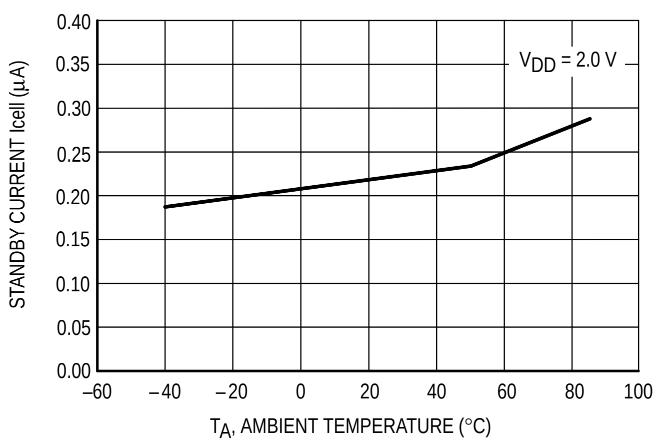


Figure 14. Cout Nch Driver On Voltage (Vol1) vs Temperature MC33349N–3X

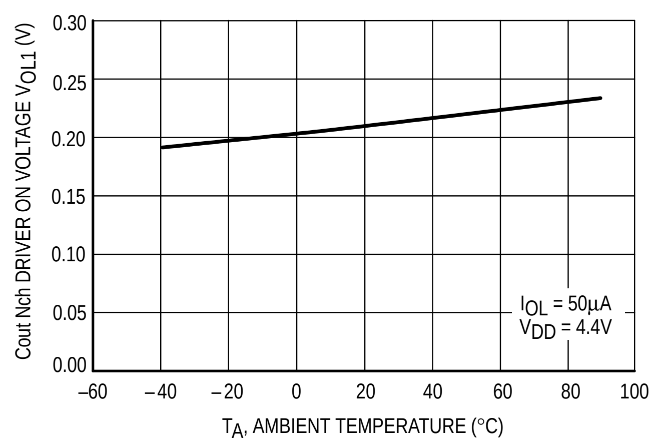


Figure 15. Cout Pch Driver On Voltage (Voh1) vs Temperature MC33349N–3X

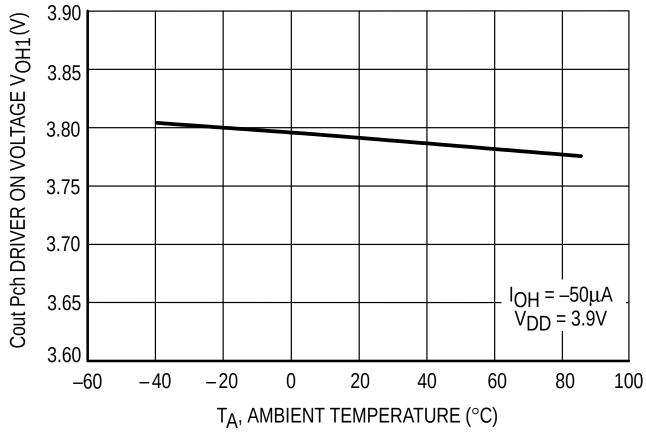


Figure 16. Dout Nch Driver On Voltage (Vol2) vs Temperature MC33349N–3X

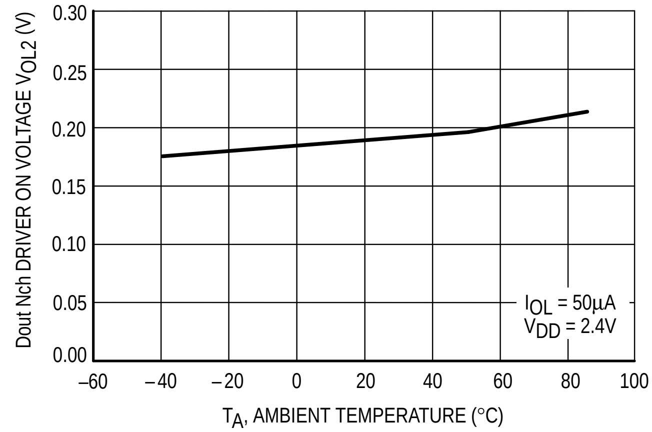


Figure 17. Dout Pch Driver On Voltage (Voh2) vs Temperature MC33349N–3X

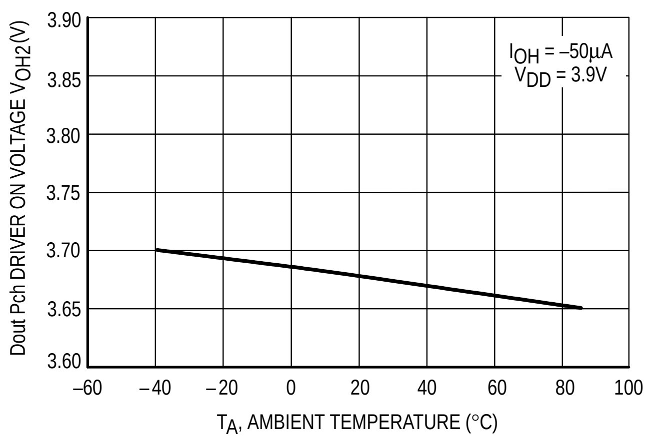


Figure 18. Short Protection Delay Time vs Capacitance C2 MC33349N–3X

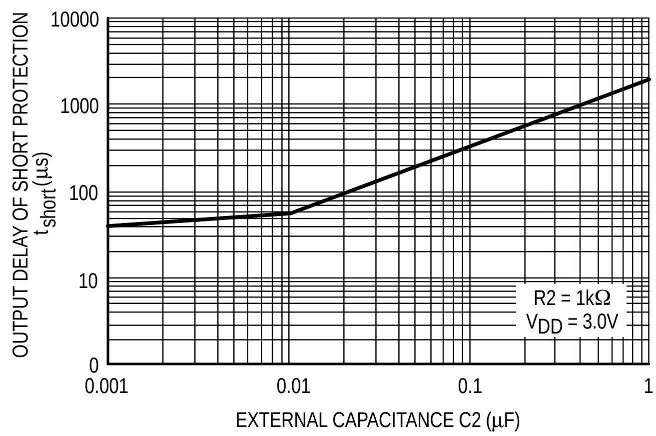


Figure 19. Excess Current Delay Time vs V_{DD} MC33349N–3X

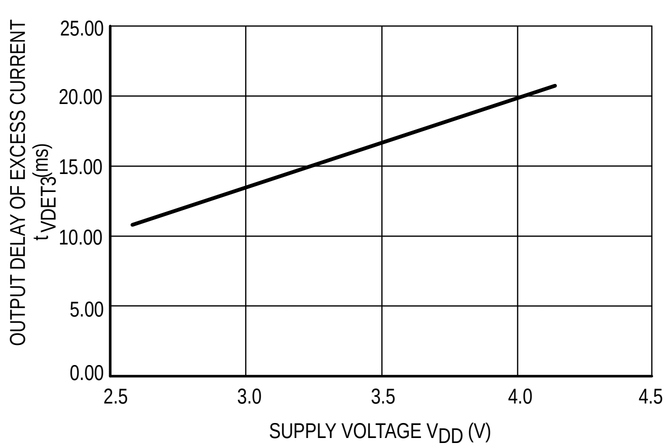


Figure 20. Excess Current Threshold vs External Resistance R2 MC33349N–3X / MC33349N–7X

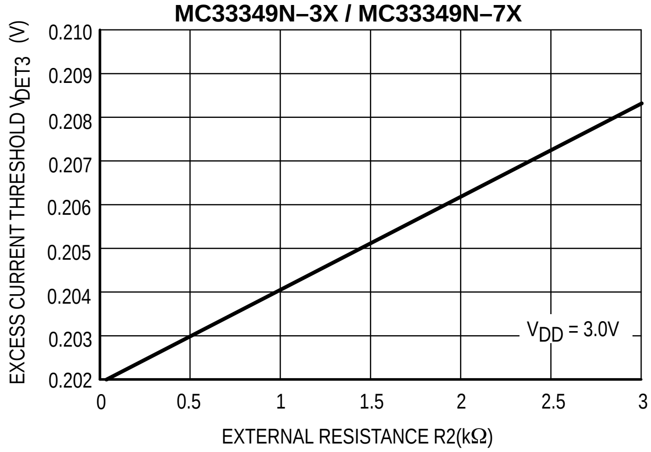
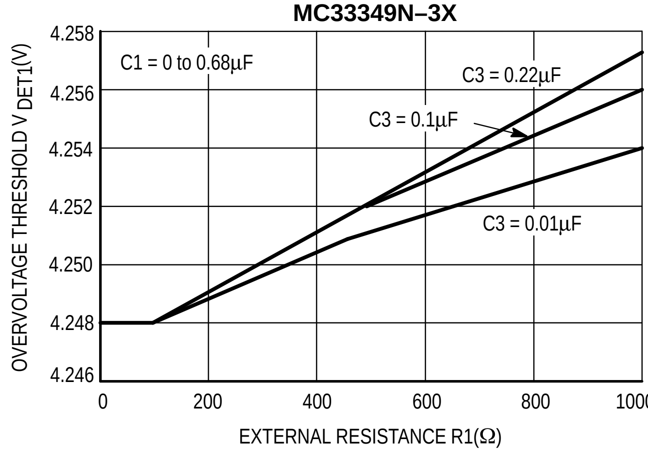


Figure 21. Overvoltage Threshold vs External Resistance R1 MC33349N–3X



OPERATING DESCRIPTION

VD1 / Over–Charge Detector

VD1 monitors the voltage at the V_{CELL} pin (V_{DD}). When it exceeds the over–charge detector threshold, V_{DET1}. VD1 senses an over–charging condition, the CO pin goes to a ”Low” level, and the external charge control, Nch–MOSFET turns off.

Resetting VD1 allows resumption of the charging process. VD1 resets under two conditions, thus, making the CO pin level ”High.” The first case occurs when the cell voltage drops below ”$V_{DET1} - V_{HYS1}$.” (V_{HYS1} is typically 200 mV). In the second case, disconnecting the charger from the battery pack can reset VD1 after V_{DD} drops between ”V_{DET1}” and ”$V_{DET1} - V_{HYS1}$”.

After detecting over–charge, connecting a load to the battery pack allows load current to flow through the parasitic diode of the external charge control FET. The CO level goes ”High” when the cell voltage drops below V_{DET1} due to load current draw through the parasitic diode.

An external capacitor connected between the Gnd pin and Ct pin sets the output delay time for over–charge detection. The external capacitor sets up a delay time from the moment of over–charge detection to the time CO outputs a signal, which enables the charge control FET to turn off. If the voltage fault occurs within the time delay window. CO will not turn off the charge control FET. The output delay time can be calculated as follows:

$$t_{VDET1}[sec] = (Ct[F] \times (VDD[V] - 0.7)/(0.48 \times 10^{-6})$$

A level shifter incorporated in a buffer driver for the CO pin drives the ”Low” level of CO pin to the P– pin voltage. A CMOS buffer sets the ”High” level of CO pin to V_{DD}.

VD2 / Over–Discharge Detector

VD2 monitors the voltage at the V_{CELL} pin (V_{DD}). When it drops below the over–discharge detector threshold, V_{DET2}, VD2 senses an over–discharge condition, the DO pin goes to a ”Low” level, and the external discharge control Nch MOSFET turns off. The IC enters a low current standby mode after detection of an over–discharged voltage by VD2. Supply current then reduces to approximately 0.3 µA. During standby mode, only the charger detector operates.

VD2 can only reset after connecting the pack to a charger. While V_{DD} remains under the over–discharge detector threshold, V_{DET2}, discharge current can flow through the parasitic diode of the external discharge control FET. The DO level goes ”High” when the cell voltage rises above V_{DET2} due to the charging current through the parasitic diode. Connecting a charger to the battery pack will instantly set DO ”High” if this causes V_{DD} to rise above V_{DET2}.

When cell voltage equals zero, one can charge the battery pack if the voltage is greater than the minimum charge voltage, V_{ST}.

Output delay time for the over–discharge detection (t_{VDET2}) is fixed internally. If the voltage fault occurs within the time delay window, DO will not turn off the discharge control FET.

A CMOS buffer sets the output of the DO pin to a ”High” level of V_{DD} and a ”Low” level of Gnd.

VD3 / Excess Current Detector, Short Circuit Detector

Both the excess current detector and the short circuit detector can work when the two control FET’s are on. When the voltage at the P– pin rises to a value between the short circuit protection voltage, V_{SHORT}, and the excess current threshold, V_{DET3}, the excess current detector operates. Increasing $V_{(P-)}$ higher than V_{SHORT} enables the short circuit detector. The DO pin then goes to a ”Low” level, and the external discharge control Nch MOSFET turns off.

Output delay time for excess current detection (t_{VDET3}) is fixed internally. If the excess current fault occurs within the time delay window, DO will not turn off the discharge control FET. However, when the short circuit protector is enabled, DO can turn off the discharge control FET. Its delay time would be approximately 5 µs.

The P– pin has a built–in pull down resistor, typically 100 kΩ, which connects to the Gnd pin. Once an excess current or short circuit fault is removed, the internal resistor pulls $V_{(P-)}$ to the Gnd pin potential. Therefore, the voltage from P– to Gnd drops below the current detection thresholds and DO turns the external MOSFET back on.

–NOTE–

If V_{DD} voltage is higher than the over–discharge voltage threshold, V_{DET2}, when excess current is detected the IC will not enter a standby mode. However, if V_{DD} is below V_{DET2} when excess current is detected, the IC will enter a standby mode. This will not occur when the short circuit detector activates.

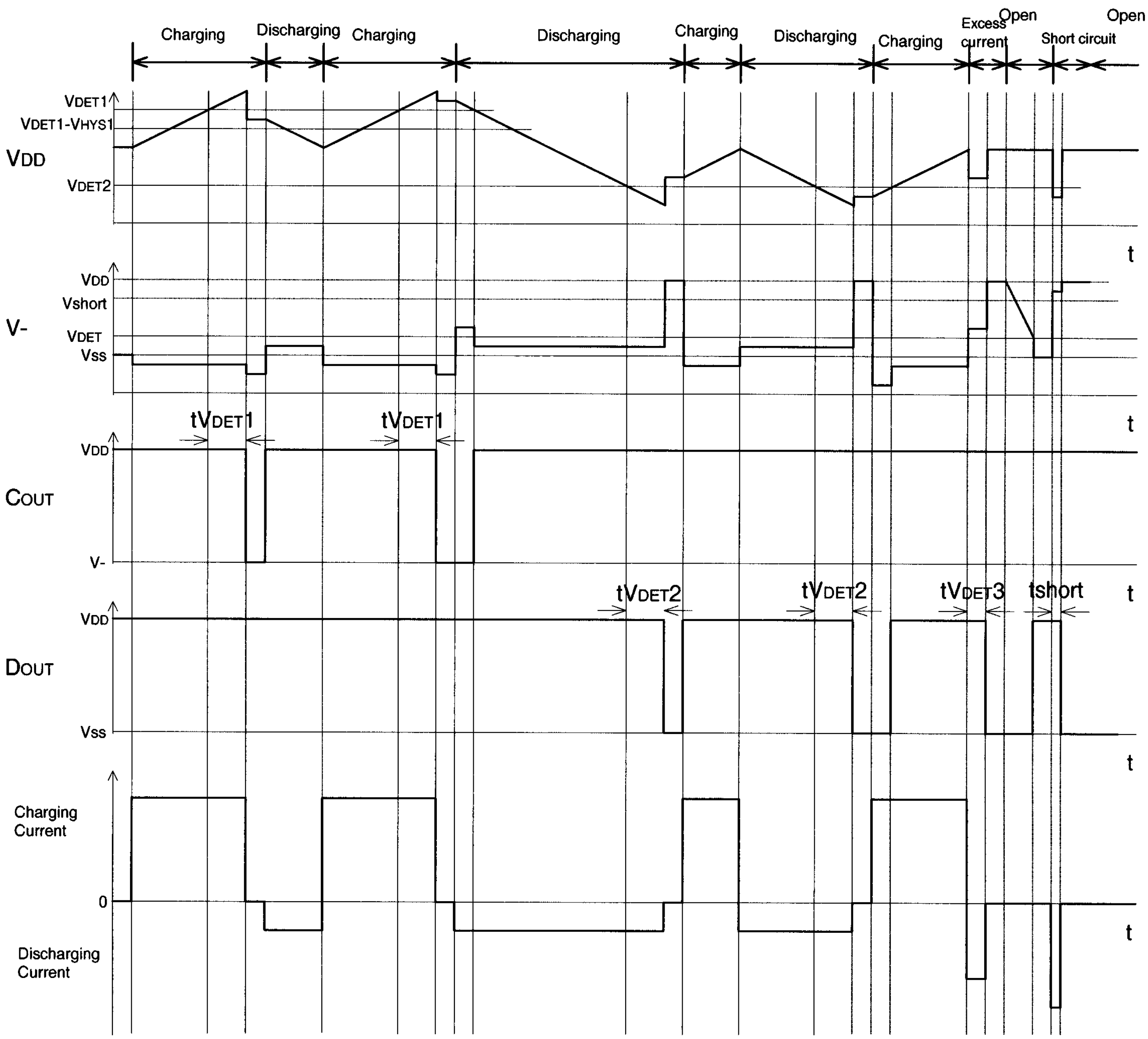


Figure 22. Timing Diagram / Operational Description

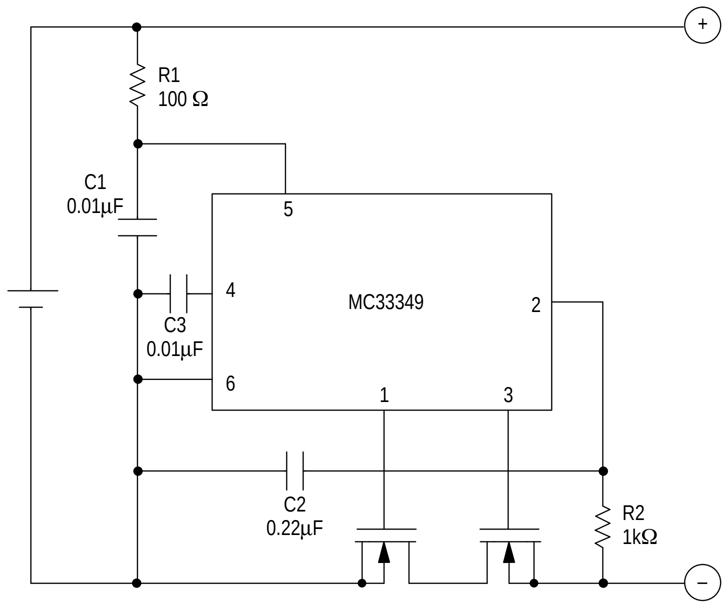


Figure 23. Typical Application Circuit

Technical Notes

R1 and C1 will stabilize a supply voltage to the MC33349. A recommended R1 value is less than 1 kΩ. A larger value of R1 leads to higher detection voltage because of shoot through current into the IC.

R2 and C2 stabilize P– pin voltage. Larger R2 values could possibly disable reset from over–discharge by connecting a charger. Recommended values are less than 1 kΩ. After an over–charge detection even connecting a battery pack to a system could probably not allow a system to draw load current if one uses a larger R2C2 time constant. The recommended C2 value is less than 1µF.

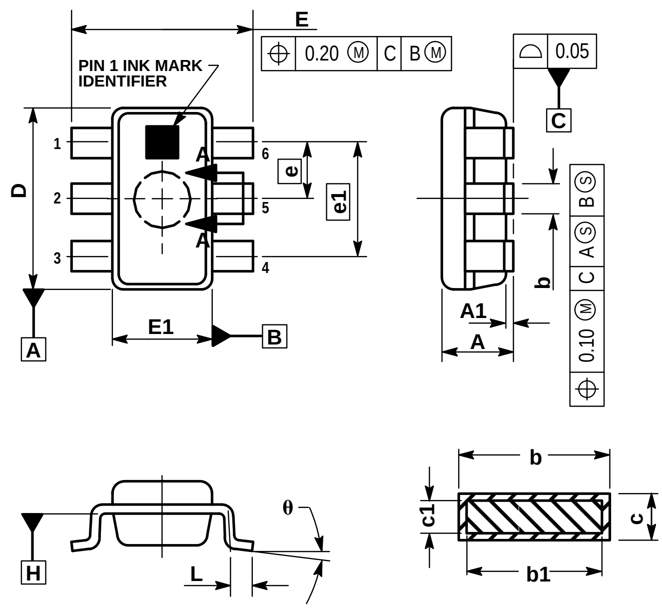
R1 and R2 can operate as a current limiter against setting cell reverse direction or for applying excess charging voltage to the IC and battery pack. Smaller R1 and R2 values may cause excessive power consumption over the specified power dissipation rating. Therefore R1+R2 should be more than 1 kΩ.

The time constants R1C1 and R2C2 must have a relation as follows:
R1C1 ≤ R2C2

If the R1C1 time constant for the Vcell pin is larger than the R2C2 time constant for the P– pin, the IC might enter a standby mode after detecting excess current. This was noted in the operating description of the current detectors.

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 1262–01
(SOT–23)
ISSUE O



SECTION A–A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION D DOES NOT INCLUDE FLASH OR PROTRUSIONS. FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.23 PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
b	0.35	0.50
b1	0.35	0.45
c	0.09	0.20
c1	0.09	0.15
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
e	0.95	
e1	1.90	
L	0.25	0.55
θ	0°	10°

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