

# MC10EP116, MC100EP116

## Hex Differential Line Receiver

The MC10EP116/100EP116 is a 6-bit differential line receiver based on the EP16 device. The 3.0GHz bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

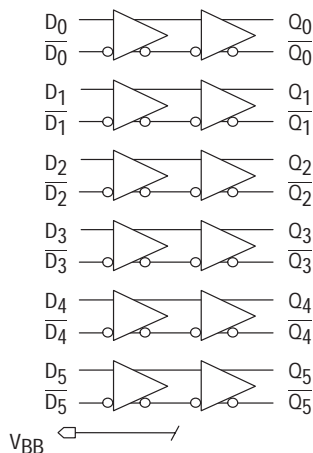
A  $V_{BB}$  pin is available to AC couple an input signal to the device. More information on AC coupling can be found in the design handbook interfacing with ECLinPS on our website.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5V below  $V_{CC}$ . All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to power supply to guarantee proper operation.

- 230ps Typical Propagation Delay
  - High Bandwidth to 3.0 GHz Typical
  - PECL mode: 3.0V to 5.5V  $V_{CC}$  with  $V_{EE} = 0V$
  - ECL mode: 0V  $V_{CC}$  with  $V_{EE} = -3.0V$  to  $-5.5V$
  - Internal Input Resistors: Pulldown on D, Pulldown and Pullup on  $\overline{D}$
  - Q Output will default LOW with inputs open or at  $V_{EE}$
  - ESD Protection: 2KV HBM, 100V MM
  - $V_{BB}$  Output
  - New Differential Input Common Mode Range
  - Moisture Sensitivity Level 2
- For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
  - Transistor Count: 729 devices

### LOGIC DIAGRAM



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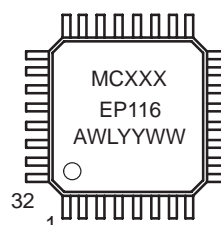


**32-LEAD TQFP**

**FA SUFFIX**

**CASE 873A**

### MARKING DIAGRAM\*



XXX = 10 or 100

A = Assembly Location

WL = Wafer Lot

YY = Year

WW = Work Week

\*For additional information, see Application Note AND8002/D

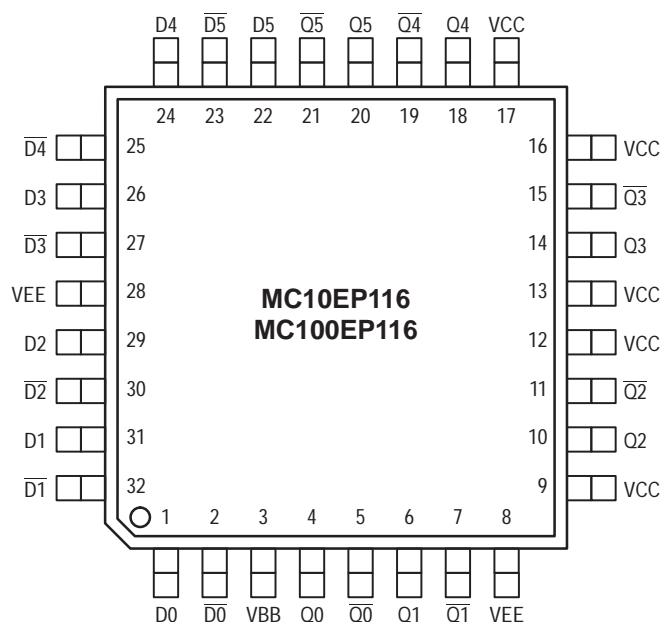
### PIN DESCRIPTION

PIN	FUNCTION
D[0:5], $\overline{D}$ [0:5]	ECL Differential Data Inputs
Q[0:5], $\overline{Q}$ [0:5]	ECL Differential Data Outputs
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

### ORDERING INFORMATION

Device	Package	Shipping
MC10EP116FA	TQFP	250 Units/Tray
MC10EP116FAR2	TQFP	2000 Tape & Reel
MC100EP116FA	TQFP	250 Units/Tray
MC100EP116FAR2	TQFP	2000 Tape & Reel

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**Figure 1. 32-Lead LQFP Pinout (Top View)**

Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>EE</sub>	Power Supply (V <sub>CC</sub> = 0V)	−6.0 to 0	VDC
V <sub>CC</sub>	Power Supply (V <sub>EE</sub> = 0V)	6.0 to 0	VDC
V <sub>I</sub>	Input Voltage (V <sub>CC</sub> = 0V, V <sub>I</sub> not more negative than V <sub>EE</sub> )	−6.0 to 0	VDC
V <sub>I</sub>	Input Voltage (V <sub>EE</sub> = 0V, V <sub>I</sub> not more positive than V <sub>CC</sub> )	6.0 to 0	VDC
I <sub>out</sub>	Output Current Continuous Surge	50 100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source Current†	± 0.5	mA
T <sub>A</sub>	Operating Temperature Range	−40 to +85	°C
T <sub>stg</sub>	Storage Temperature	−65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	80 55	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	12 to 17	°C/W
T <sub>sol</sub>	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

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## DC CHARACTERISTICS, ECL/LVECL ( $V_{CC} = 0V$ ; $V_{EE} = -5.5V$ to $-3.0V$ ) (Note 4.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 1.)	55		95	55	80	95	55		95	mA
VOH	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
VOL	Output LOW Voltage (Note 2.)	-1995	-1810	-1685	-1995	-1745	-1620	-1995	-1685	-1560	mV
VIH	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
VIL	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
VBB	Output Voltage Reference	-1575	-1475	-1375	-1540	-1440	-1340	-1515	-1415	-1315	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 3.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	$\frac{D}{\bar{D}}$	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1.  $V_{CC} = 0V$ ,  $V_{EE} = V_{EEmin}$  to  $V_{EEmax}$ , all other pins floating.
2. All loading with 50 ohms to  $V_{CC}-2.0$  volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .
4. Input and output parameters vary 1:1 with  $V_{CC}$ .

## DC CHARACTERISTICS, LVPECL ( $V_{CC} = 3.3V \pm 0.3V$ , $V_{EE} = 0V$ ) (Note 8.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)	55		95	55	80	95	55		95	mA
VOH	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 6.)	1305	1490	1615	1305	1555	1680	1305	1615	1740	mV
VIH	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
VIL	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
VBB	Output Voltage Reference	1725	1825	1925	1760	1860	1960	1785	1885	1985	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	$\frac{D}{\bar{D}}$	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5.  $V_{CC} = 3.0V$ ,  $V_{EE} = 0V$ , all other pins floating.
6. All loading with 50 ohms to  $V_{CC}-2.0$  volts.
7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .
8. Input and output parameters vary 1:1 with  $V_{CC}$ .

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## DC CHARACTERISTICS, PECL ( $V_{CC} = 5.0V \pm 0.5V$ , $V_{EE} = 0V$ ) (Note 12.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 9.)	55		95	55	80	95	55		95	mA
VOH	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
VOL	Output LOW Voltage (Note 10.)	3005	3190	3315	3005	3255	3380	3005	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
VIL	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
VBB	Output Voltage Reference	3425	3525	3625	3460	3560	3660	3485	3585	3685	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	D D	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

9.  $V_{CC} = 5.0V$ ,  $V_{EE} = 0V$ , all other pins floating.

10. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

11.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ .

12. Input and output parameters vary 1:1 with  $V_{CC}$ .

## AC CHARACTERISTICS ( $V_{CC} = 0V$ ; $V_{EE} = -3.0V$ to $-5.5V$ ) or ( $V_{CC} = 3.0V$ to $5.5V$ ; $V_{EE} = 0V$ )

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>max</sub>	Maximum Toggle Frequency (Note 13.)					3.0					GHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay to Output Differential	150	250	350	150	250	350	180	280	380	ps
t <sub>SKEW</sub>	Duty Cycle Skew (Note 14.)		5.0			5.0	20		5.0	20	ps
t <sub>JITTER</sub>	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V <sub>PP</sub>	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Times (20% – 80%)	Q	90 150	220	90 160	160	240	90 160	160	250	ps

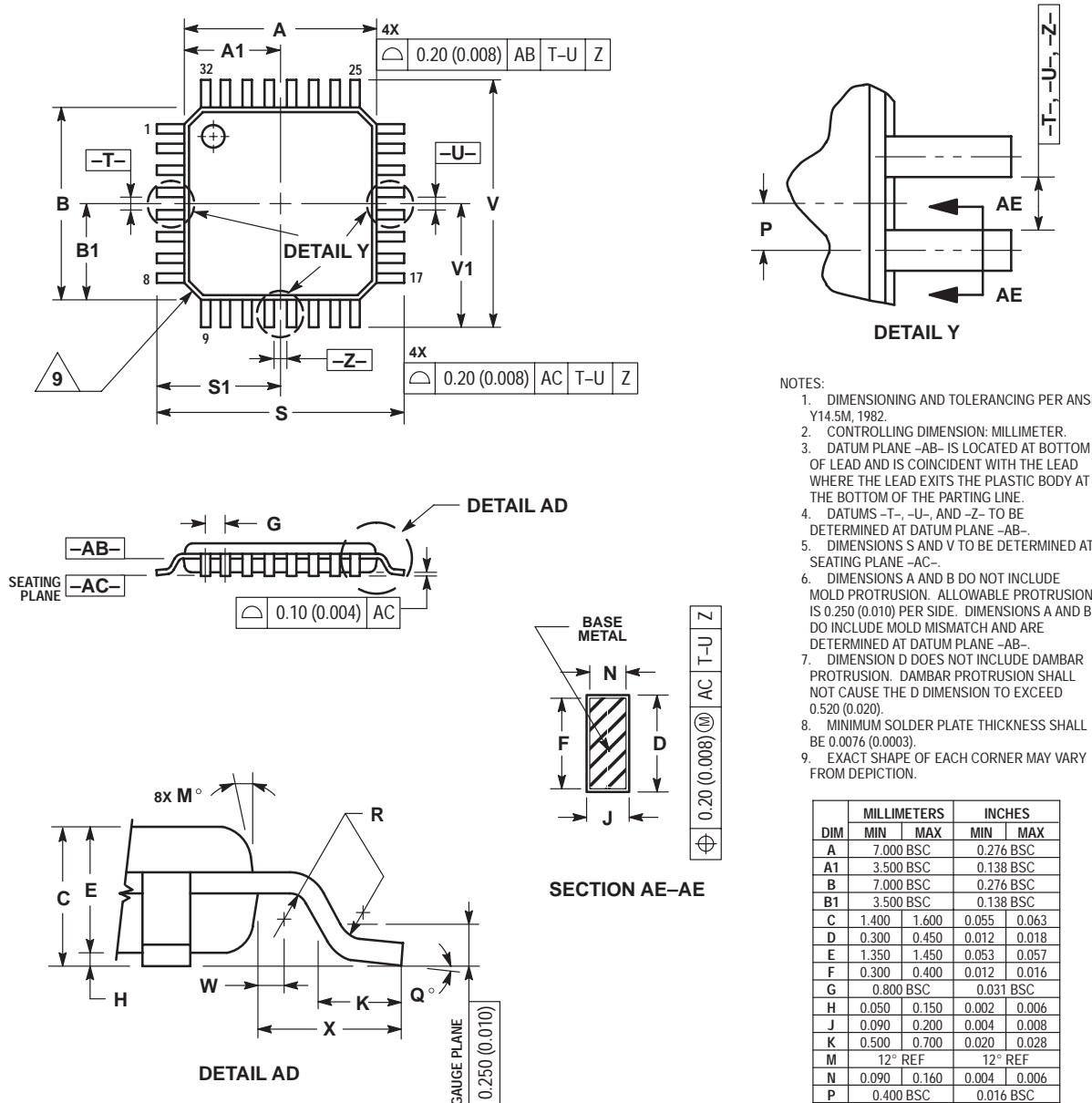
13. F<sub>max</sub> guaranteed for functionality only.

14. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

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## PACKAGE DIMENSIONS

TQFP  
FA SUFFIX  
32-LEAD PLASTIC PACKAGE  
CASE 873A-02  
ISSUE A



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

## **Notes**

## **Notes**

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