MC10EP016

Product Preview

8-Bit Synchronous Binary Up Counter

The MC10EP016 is a high–speed synchronous, presettable, cascadeable 8–bit binary counter. Architecture and operation are the same as the MC10E016 in the ECLinPS™ family.

The counter features internal feedback to $\overline{TC}$ gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all–one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated. COUT and $\overline{COUT}$ have been added so cascading can now be done without adding external components. A differential clock input has also been added to improve signal to noise ratio.

- 1.3GHz Typical Count Frequency
- PECL mode: 3.0V to 5.5V V_{CC} with V_{EE} = 0V
- ECL mode: 0V V_{CC} with V_{EE} = –3.0V to –5.5V
- 550ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- Addition of COUT and $\overline{COUT}$
- 8–Bit
- Differential Clock Input
- VBB Output
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Q Output will default LOW with inputs open or at V_{EE}
- 75kΩ Pulldown Resistors
- ESD Protection: >4KV HBM, >200V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 897 devices

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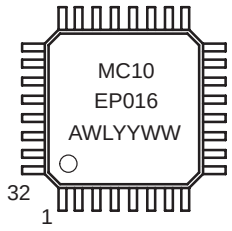
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP016FA	TQFP	250 Units/Tray
MC10EP016FAR2	TQFP	2000 Tape & Reel

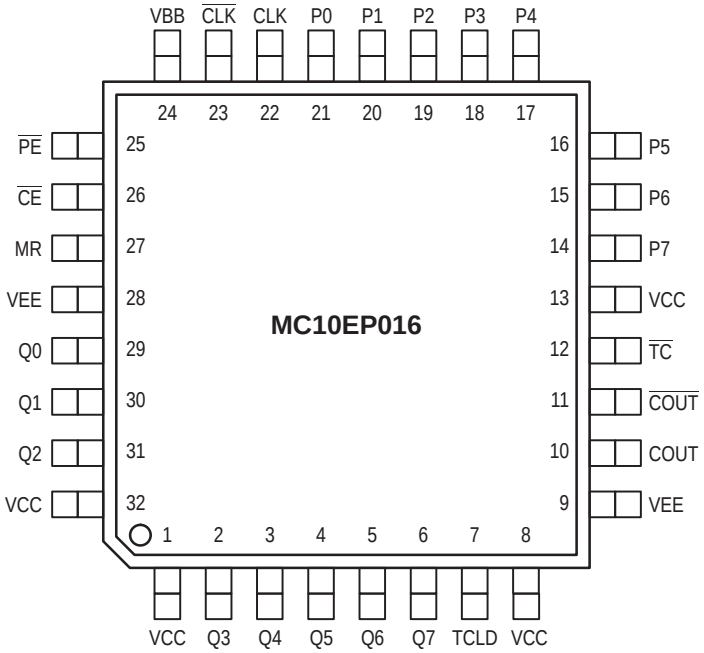


Figure 1. 32–Lead TQFP Pinout
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION	
PIN	**FUNCTION**
P0–P7	ECL Parallel Data (Preset) Inputs
Q0–Q7	ECL Data Outputs
$\overline{CE}$	ECL Count Enable Control Input
$\overline{PE}$	ECL Parallel Load Enable Control Input
MR	ECL Master Reset
CLK, $\overline{CLK}$	ECL Differential Clock
$\overline{TC}$	ECL Terminal Count Output
TCLD	ECL TC–Load Control Input
COUT, $\overline{COUT}$	ECL Carry–Out Output
VCC	Positive Supply
VEE	Negative, 0 Supply
VBB	Reference Voltage Output

FUNCTION TABLES

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	FUNCTION
X	L	X	L	Z	Load Parallel (Pn to Qn)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Qn : = LOW, $\overline{TC}$: = HIGH)

ZZ = Clock Pulse (High–to–Low)
Z = Clock Pulse (Low–to–High)

FUNCTION TABLE

Function	$\overline{PE}$	$\overline{CE}$	MR	TCLD	CLK	P7–P4	P3	P2	P1	P0	Q7–Q4	Q3	Q2	Q1	Q0	TC	$\overline{COUT}$	COUT
Load Count	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L	L	H
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H	H	L
Load Hold	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
Load on Terminal Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H	H	L
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V; V_{EE} = –5.5V to –3.0V) (Note 3.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
IEE	Power Supply Current (Note 1.)					150(4)					mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1135	–1060	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1935	–1810	–1685	–1870	–1745	–1620	–1810	–1685	–1560	mV
V_{IH}	Input HIGH Voltage Single Ended	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage Single Ended	–1935		–1610	–1870		–1545	–1810		–1485	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Input and output parameters vary 1:1 with V_{CC}.
4. Recommend 500 lfpm air flow when using –5.2V power supply.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.3V, V_{EE} = 0V) (Note 7.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 5.)					150					mA
V_{OH}	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

5. V_{CC} = 3.3V, V_{EE} = 0V, all other pins floating.
6. All loading with 50 ohms to V_{CC}–2.0 volts.
7. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL (V_{CC} = 5.0V ± 0.5V, V_{EE} = 0V) (Note 10.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IEE	Power Supply Current (Note 8.)					150(11)					mA
V_{OH}	Output HIGH Voltage (Note 9.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 9.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

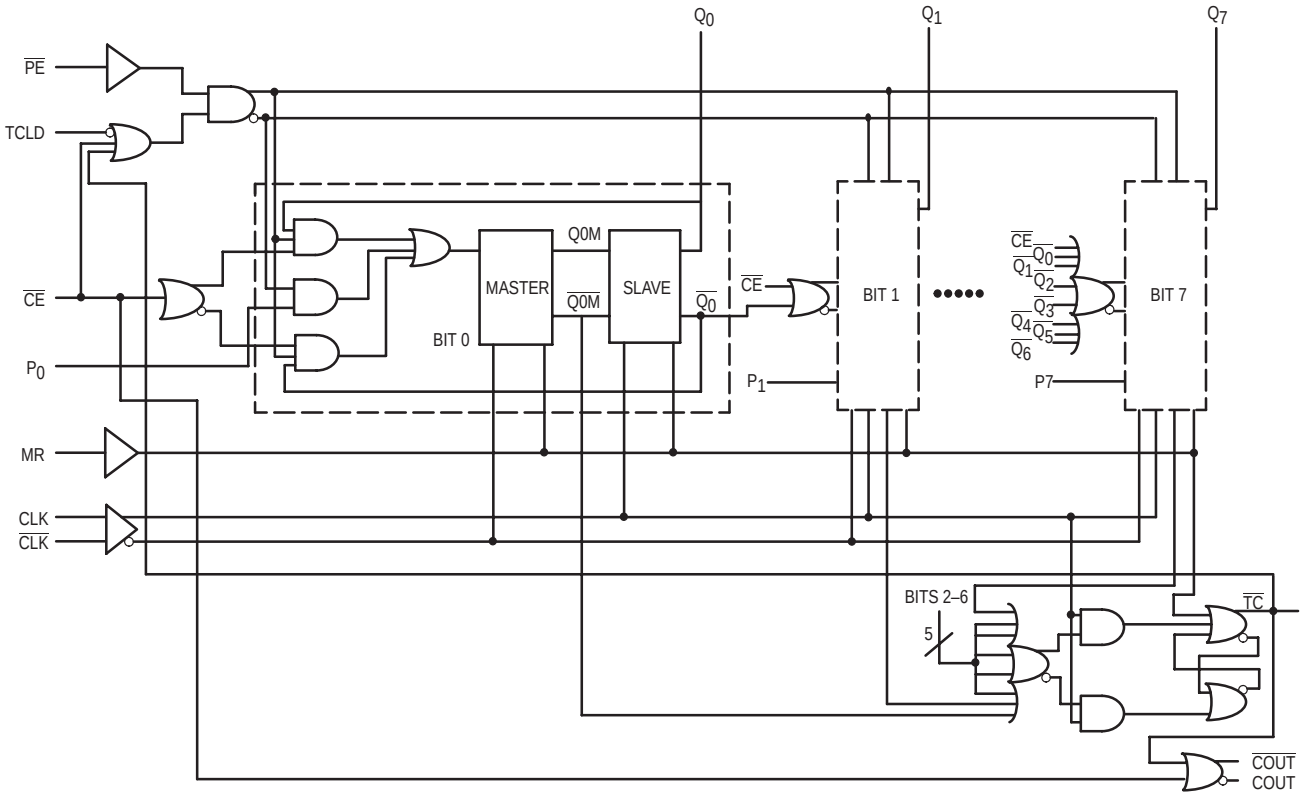
8. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating.
9. All loading with 50 ohms to V_{CC}–2.0 volts.
10. Input and output parameters vary 1:1 with V_{CC}.
11. Recommend 500 lfpm air flow when using +5V power supply.

AC CHARACTERISTICS (V_{EE} = –3.6V to –3.0; V_{CC} = GND)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Count Frequency (Note 12.)					1.3					GHz
t_{PLH} t_{PHL}	Propagation Delay CLK –> Q MR –> Q CLK –> $\overline{TC}$ MR –> $\overline{TC}$					500 550 550 550					ps
t_S	Setup Time Pn $\overline{CE}$ $\overline{PE}$ TCLD										ps
t_H	Hold Time Pn $\overline{CE}$ $\overline{PE}$ TCLD										ps
t_{RR}	Reset Recovery Time										ps
t_{PW}	Minimum Pulse Width CLK, MR					300					ps
t_r t_f	Output Rise/Fall Times (20% – 80%)					165					ps

12. f_{max} specified to 1.3GHz with reduced output swing.

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

Applications Information

Cascading Multiple EP016 Devices

For applications which call for larger than 8-bit counters multiple EP016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of EP016 devices. Two EP016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 1 below pictorially illustrates the cascading of 4 EP016s to build a 32-bit high frequency counter. Note the EP01 gates used to OR the terminal count outputs of the lower order EP016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant EP016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an EP016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting EP016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary setup time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 1 shows EP01 gates used to control the count enable inputs, however, if the frequency of operation is lower a slower, LVECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is TBD and that for a 16-bit counter is TBD. Figure 2 shows cascade approach using $\overline{COUT}$ output with no external gates. This may cause a reduced frequency due to internal gate delays.

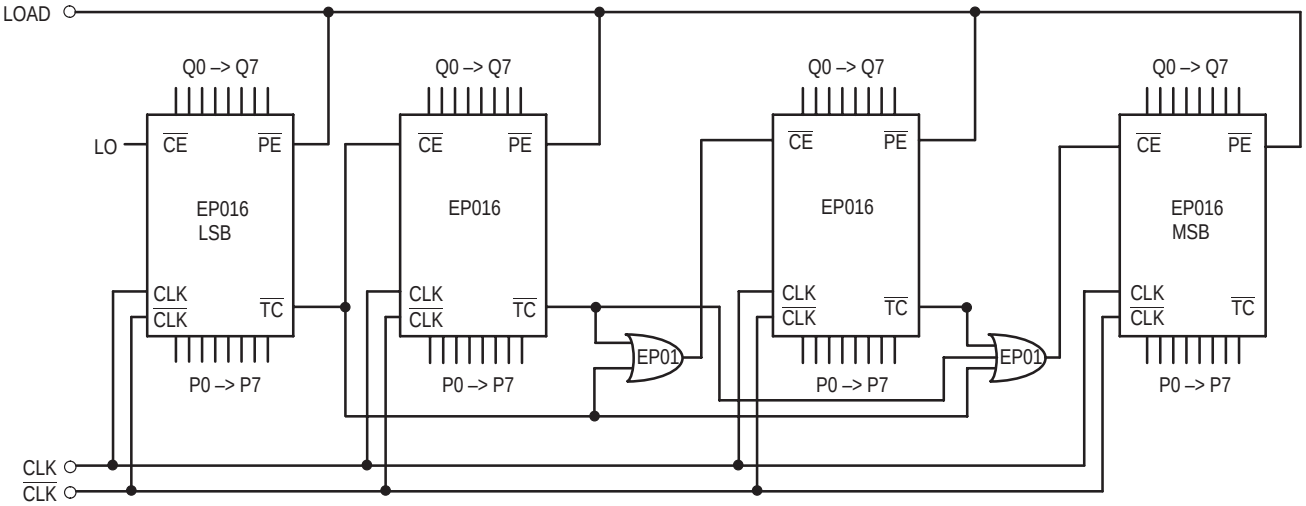


Figure 1. 32-Bit Cascaded EP016 Counter

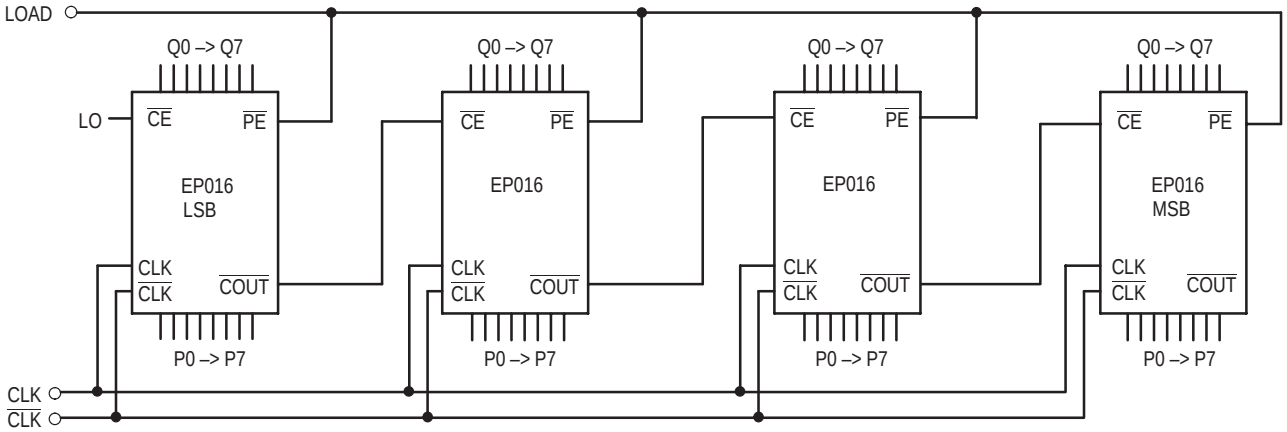


Figure 2. 32-Bit Cascaded EP016 Counter without external gates

Applications Information (continued)

Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

The EP016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 3 below illustrates the input conditions necessary for utilizing the EP016 as a programmable divider set up to divide by 113.

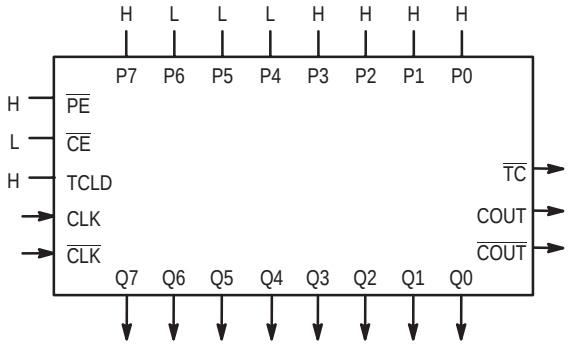


Figure 3. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = 256 – 113 = $8F_{16}$ = 1000 1111

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 3 will result in the waveforms of Figure 4. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 1. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single EP016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple EP016s can be cascaded in a manner similar to that already discussed. When EP016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple EP016 divider chains.

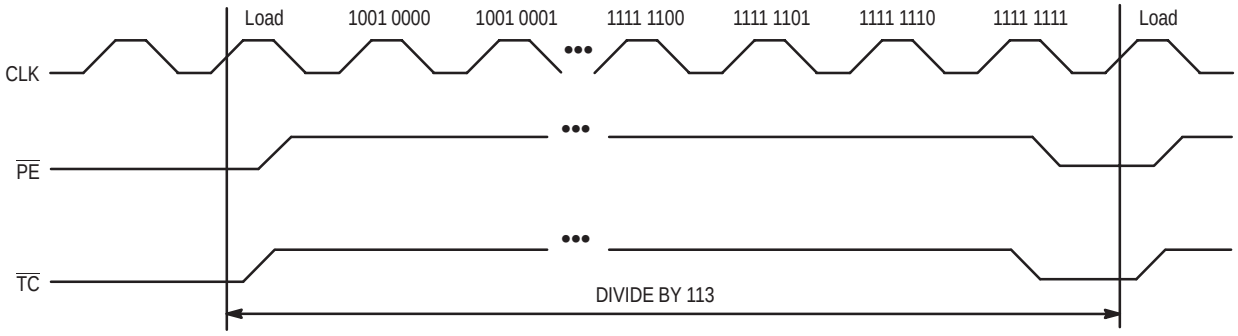


Figure 4. Divide by 113 EP016 Programmable Divider Waveforms

Applications Information (continued)

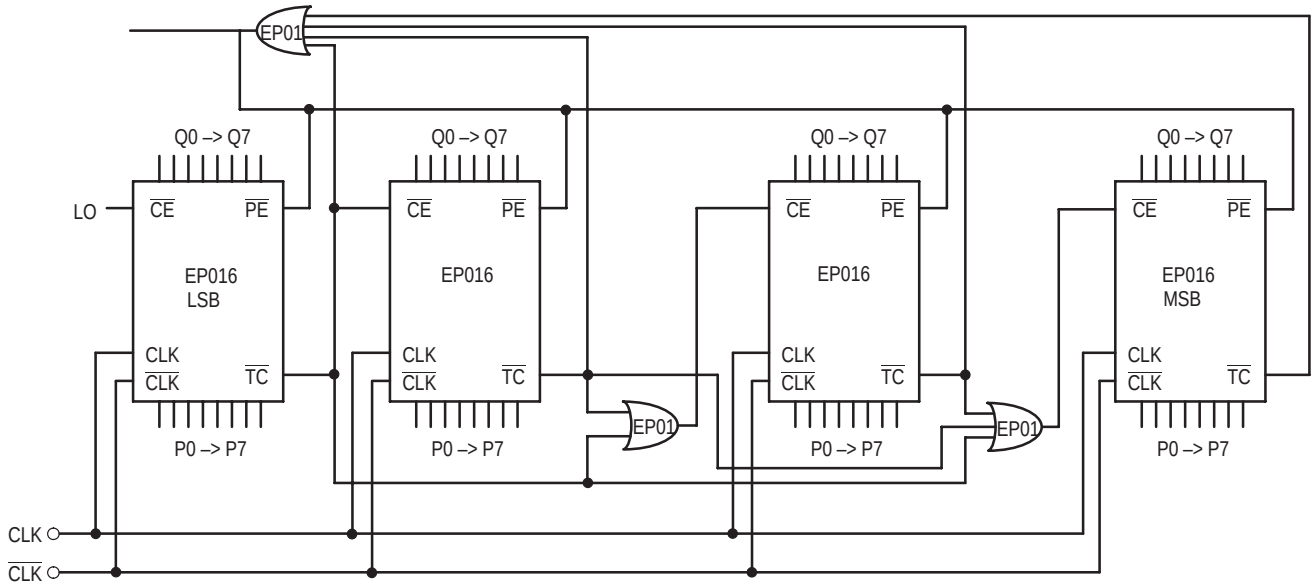


Figure 5. 32-Bit Cascaded EP016 Programmable Divider

Figure 5 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EP01 OR gates were used. For lower frequency applications a slower OR gate could replace the EP01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant EP016 must also feed the $\overline{CE}$ input of the most significant EP016. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Figure 6 shows a typical block diagram of a 32–bit divider chain using $\overline{COUT}$ and no external components. This may cause a reduced maximum frequency due to internal gate delays.

Maximizing EP016 Count Frequency

The EP016 device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

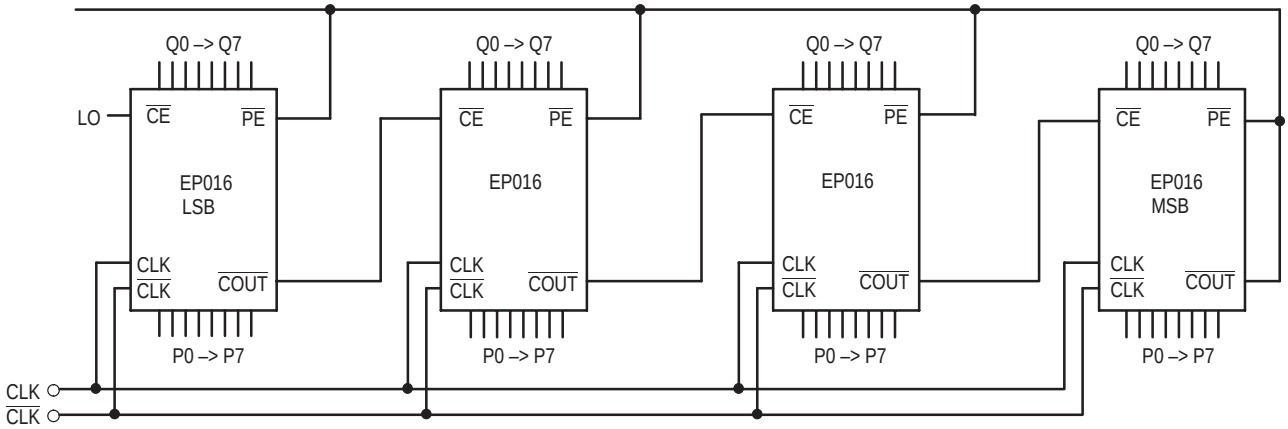
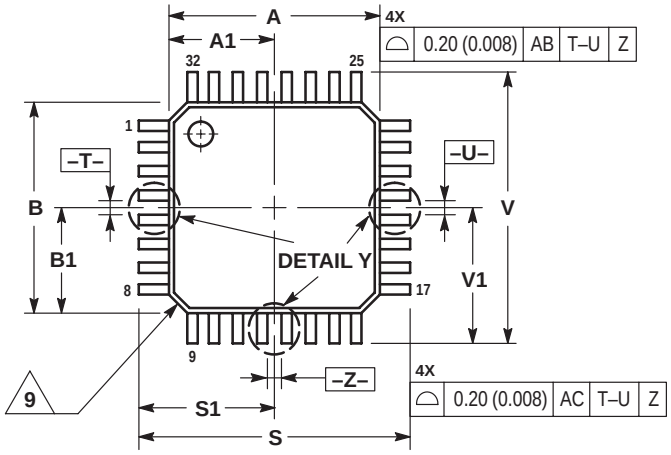
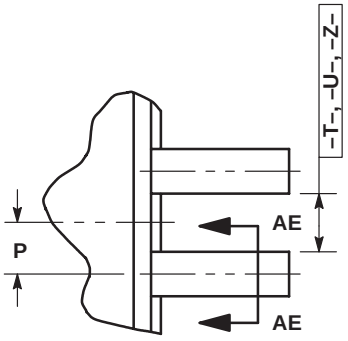


Figure 6. 32-Bit Cascaded EP016 Programmable Divider without external gates

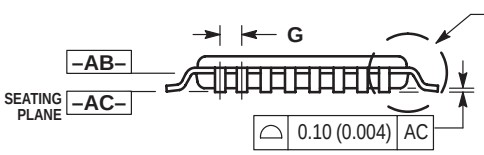
PACKAGE DIMENSIONS

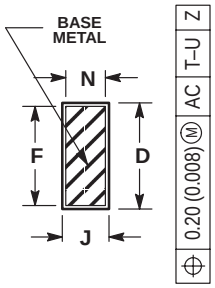
TQFP
FA SUFFIX
32–LEAD PLASTIC PACKAGE
CASE 873A–02
ISSUE A



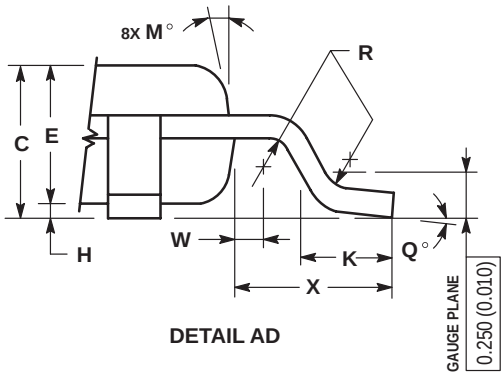


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

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