

**MNLM6161-X REV 2A1**

Original Creation Date: 08/03/95

Last Update Date: 11/23/98

Last Major Revision Date: 10/28/98

## HIGH SPEED OPERATIONAL AMPLIFIER

### General Description

The LM6161 high-speed amplifier exhibits an excellent speed-power product in delivering 300 V/uS and 50 MHz unity gain stability with only 5 mA of supply current. Further, power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

This amplifier is built with National's VIP[™] (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

### Industry Part Number

LM6161

### Prime Die

LM6161B

### NS Part Numbers

LM6161E/883\*  
 LM6161J-QMLV \*\*  
 LM6161J/883 \*\*\*  
 LM6161W-SMD \*\*\*\*  
 LM6161W/883  
 LM6161WG-QMLV \*\*\*\*\*  
 LM6161WG/883 \*\*\*\*\*

### Controlling Document

See Features Page

### Processing

MIL-STD-883, Method 5004

### Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

**Features**

- High slew rate 300V/uS
- High unity gain freq 50MHz
- Low supply current 5mA
- Fast settling 120nS to 0.1%
- Low differential gain <0.1%
- Low differential phase 0.1 degrees
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply
- SMD : 5962-89621012A\*,VPA\*\*,PA\*\*\*,HA\*\*\*\*,VXA\*\*\*\*\*,XA\*\*\*\*\*

**Applications**

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

**(Absolute Maximum Ratings)**

(Note 1)

Supply Voltage (V+ - V-)	36V
Differential Input Voltage Range (Note 4)	±8V
Common-Mode Voltage Range (Note 6)	(V+ - 0.7V) to (V- - 7V)
Output Short Circuit to Gnd (Note 3)	Continuous
Power Dissipation (Note 2)	400mW
Soldering Information (Soldering, 10 seconds)	260 C
Storage Temperature Range	-65 C to +150 C
Maximum Junction Temperature	150 C
Thermal Resistance	
ThetaJA	
LCC	90 C/W
(500LF/Min Air flow)	61 C/W
CERDIP	113 C/W
(500LF/Min Air flow)	51 C/W
CERPAK	228 C/W
(500LF/Min Air flow)	140 C/W
CERAMIC SOIC	228 C/W
(500LF/Min Air flow)	140 C/W
ThetaJC	
LCC	20 C/W
CERDIP	21 C/W
CERPAK	21 C/W
CERAMIC SOIC	21 C/W
ESD Tolerance (Note 4, 5)	±500V
<p>Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.</p> <p>Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.</p> <p>Note 3: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 C.</p> <p>Note 4: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vio, Iio and Noise).</p> <p>Note 5: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100pF in series with 1500 Ohms.</p> <p>Note 6: The voltage between V+ and either input pin must not exceed 36V.</p>	

## Recommended Operating Conditions

(Note 1)

Temperature Range

$-55\text{ }^{\circ}\text{C} \leq T_A \leq +125\text{ }^{\circ}\text{C}$

Supply Voltage Range

4.75V to 32V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

## Electrical Characteristics

### DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)  
 DC:  $V_{cc} = \pm 15V$ ,  $V_{cm} = 0V$ ,  $R_l \geq 100K$  Ohms,  $R_s = 10K$  Ohms.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-7	7	mV	1
					-10	10	mV	2, 3
Iib	Input Bias Current				-3	3	uA	1
					-6	6	uA	2, 3
Iio	Input Offset Current				-350	350	nA	1
					-800	800	nA	2, 3
+Vcmr	Positive Common-Mode Voltage Range	$V_{cc} = \pm 15V$			13.9		V	1
		$V_{cc} = \pm 15V$			13.8		V	2, 3
		$V_{cc} = +5V$	2		3.9		V	1
			2		3.8		V	2, 3
-Vcmr	Negative Common-Mode Voltage Range	$V_{cc} = \pm 15V$				-12.9	V	1
		$V_{cc} = \pm 15V$				-12.7	V	2, 3
		$V_{cc} = +5V$	2			2.0	V	1
			2			2.2	V	2, 3
CMRR	Common-Mode Rejection Ratio	$-12.9V \leq V_{cm} \leq 13.9V$			80		dB	1
		$-12.7V \leq V_{cm} \leq 13.8V$			74		dB	2, 3
PSRR	Power Supply Rejection Ratio	$\pm 10V \leq V_{cc} \leq \pm 16V$			80		dB	1
		$\pm 10V \leq V_{cc} \leq \pm 16V$			74		dB	2, 3
Ios	Output Short Circuit Current	Source				-30	mA	1
						-20	mA	2, 3
		Sink			30		mA	1
					20		mA	2, 3
Icc	Supply Current					6.5	mA	1
						6.8	mA	2, 3
Avs	Large Signal Voltage Gain	$V_{out} = \pm 10V$ , $R_l = 2K$ Ohms	1		550		V/V	1
		$V_{out} = \pm 10V$ , $R_l = 2K$ Ohms	1		300		V/V	2, 3
+Vop	Positive Voltage Swing	$V_{cc} = \pm 15V$ , $R_l = 2K$ Ohms			13.5		V	1
		$V_{cc} = \pm 15V$ , $R_l = 2K$ Ohms			13.3		V	2, 3
		$V_{cc} = +5V$ , $R_l = 2K$ Ohms			3.5		V	1
					3.3		V	2, 3

## Electrical Characteristics

### DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_L \geq 100K \text{ Ohms}$ ,  $R_S = 10K \text{ Ohms}$ .

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Vop	Negative Voltage Swing	$V_{CC} = \pm 15V$ , $R_L = 2K \text{ Ohms}$				-13.0	V	1
		$V_{CC} = \pm 15V$ , $R_L = 2K \text{ Ohms}$				-12.7	V	2, 3
		$V_{CC} = +5V$ , $R_L = 2K \text{ Ohms}$				1.7	V	1
						2.0	V	2, 3

### AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_L \geq 100K \text{ Ohms}$ ,  $R_S = 10K \text{ Ohms}$ .

Gbw	Gain Bandwidth Product	$f = 20Mhz$			40		Mhz	4
					30		Mhz	5, 6
+Sr	Slew Rate	Output step = -4V to +4V, $A_v = +1$ , $V_{in} = 8V \text{ step}$			200		V/uS	4
					180		V/uS	5, 6
-Sr	Slew Rate	Output step = +4V to -4V, $A_v = +1$ , $V_{in} = 8V \text{ step}$			200		V/uS	4
					180		V/uS	5, 6
ts	Setting Time	10V step to 0.1% , $A_v = 1$ , $R_L = 2K \text{ Ohms}$				300	nS	9
						325	nS	10, 11

### DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC:  $V_{CC} = \pm 15V$ ,  $V_{CM} = 0V$ ,  $R_L \geq 100K \text{ Ohms}$ ,  $R_S = 10K \text{ Ohms}$ . Delta Calculations Performed on QMLV Devices at Group B, Subgroup 5 ONLY.

Vio	Input Offset Voltage				-0.7	+0.7	mV	1
Iib	Input Bias Current				-0.5	+0.5	uA	1
Iio	Input Offset Current				-35	+35	nA	1
CMRR	Common Mode Rejection Ratio	$-12.9V \leq +V_{CM} \leq 13.9V$			-5	+5	dB	1

Note 1: Voltage gain is the total output swing (20V) divided by the signal required to produce that swing.

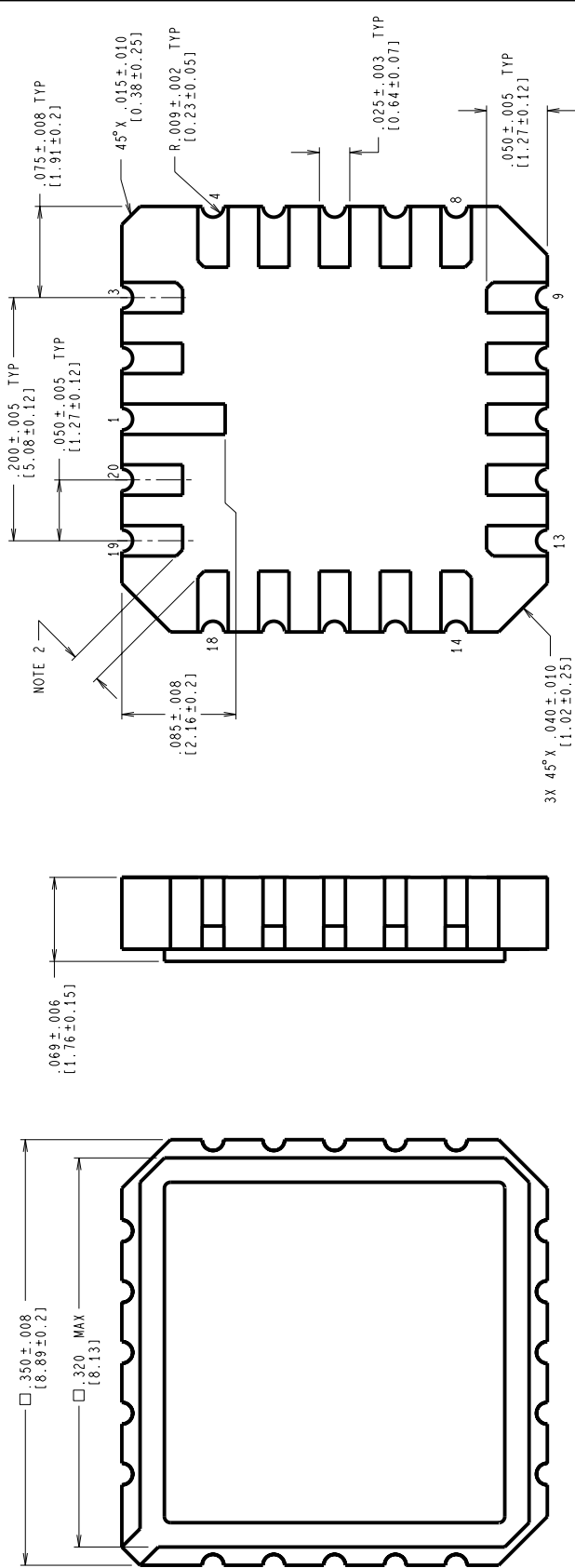
Note 2: For single supply operation, the following conditions apply:  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $V_{out} = 2.5V$ . Vio adjust pins are each connected to  $V_-$  to realize maximum output swing. This connection will degrade Vio.

## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05885HRA4	CERDIP (J), 8 LEAD (B/I CKT)
06190HRA3	CERPACK (W, WG), 10LD (B/I CKT)
06191HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000167A	CERPACK (W), 10 LEAD (PINOUT)
P000168B	LCC (E), 20 LEAD, TYPE C (PINOUT)
P000169A	CERDIP (J), 8 LEAD (PINOUT)
P000259A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

- NOTES: UNLESS OTHERWISE SPECIFIED.
- LEAD FINISH TO BE ONE OF THE FOLLOWING:
    - 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
    - SOLDER DIP.
  - CORNER PADS MAY HAVE A  $45^\circ \times .020 \text{ IN}/0.51 \text{ mm}$  MAXIMUM CHAMFER TO ACCOMPLISH THE  $.015 \text{ IN}/0.38 \text{ mm}$  DIMENSION.
  - REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

# MIL/AERO CONFIGURATION CONTROL

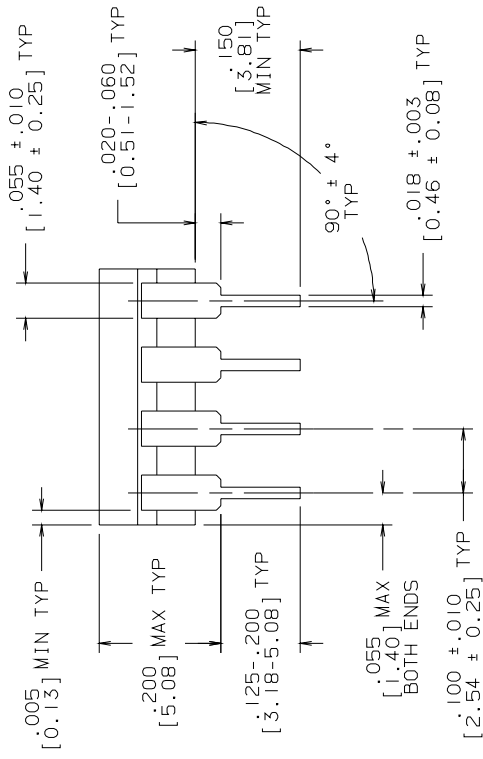
APPROVALS		DATE	SCALE		SIZE	DRAWING NUMBER	REV
DESIGN	Design Grady	02/10/94	N/A	C	MKT-E20A	E	E
ESTD	CHK						
ENGR	CHK						
APPROVAL							
PROJECTION							
DO NOT SCALE DRAWING							
SHEET 1 of 1							

**NATIONAL SEMICONDUCTOR CORPORATION**  
2000 Semiconductor Drive, Santa Clara, CA 95052-8000


**LEADLESS CHIP CARRIER,  
TYPE C,  
20 TERMINAL**

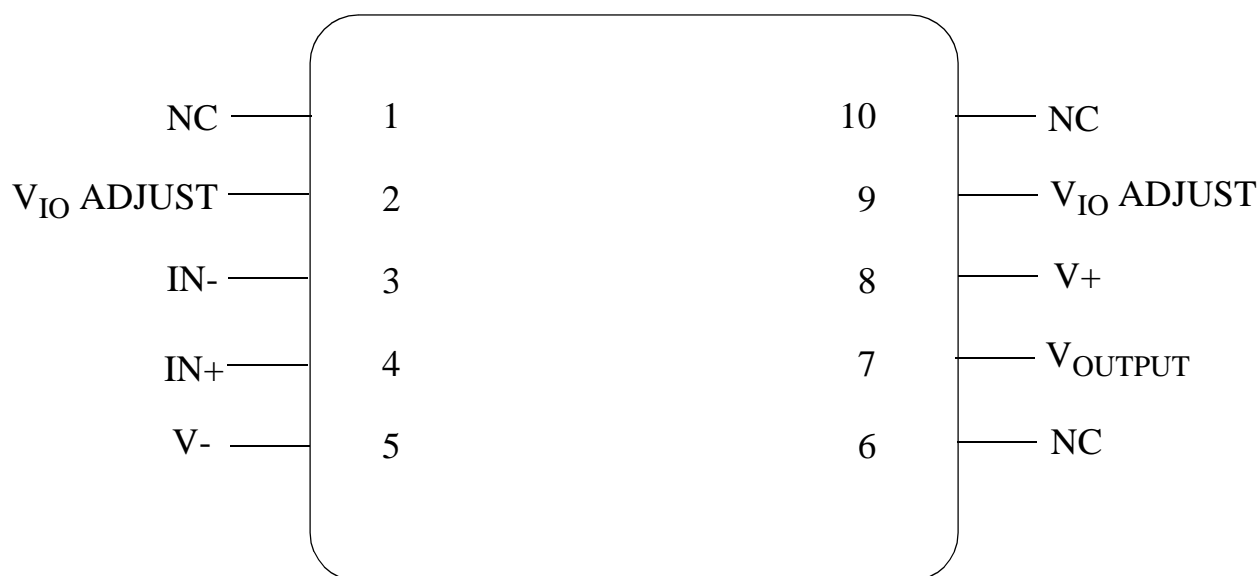


LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/



2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

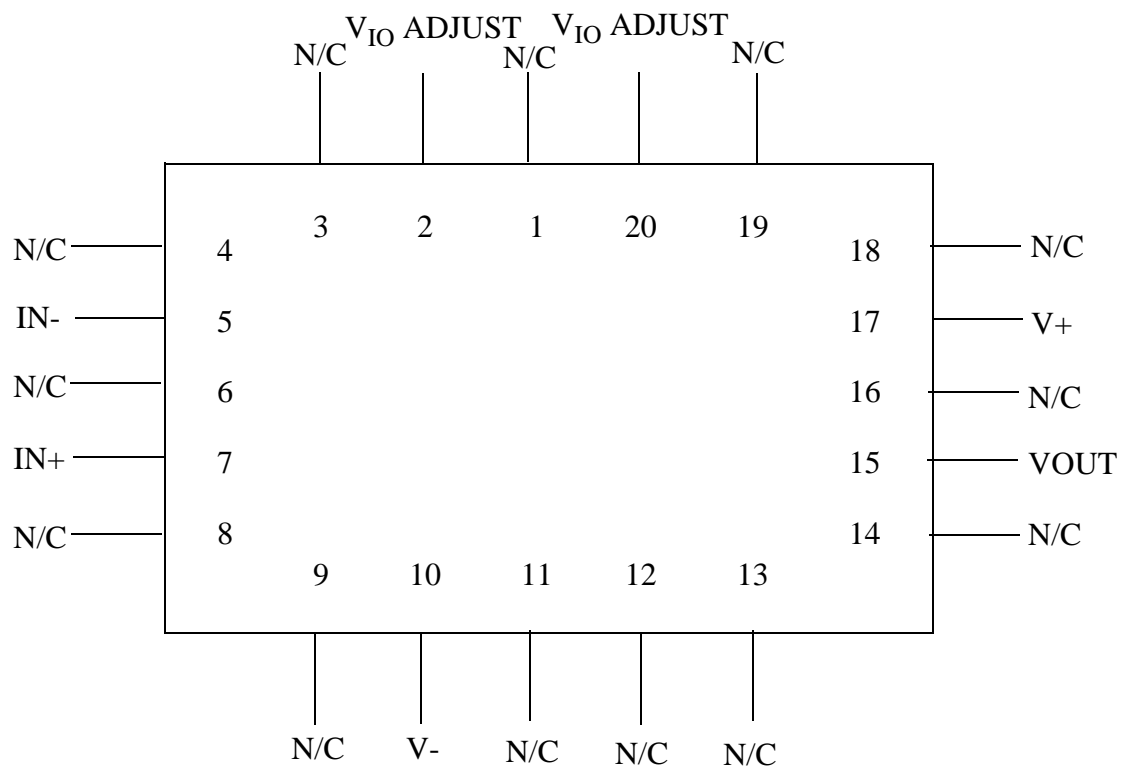
	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J08A	L
	DO NOT SCALE	DRAWING	SHEET	OF



**LM6161W**  
**10 - LEAD CERPACK**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000167A**



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 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050



# LM6161E

## 20 - LEAD LCC

### CONNECTION DIAGRAM

### TOP VIEW

### P000168B



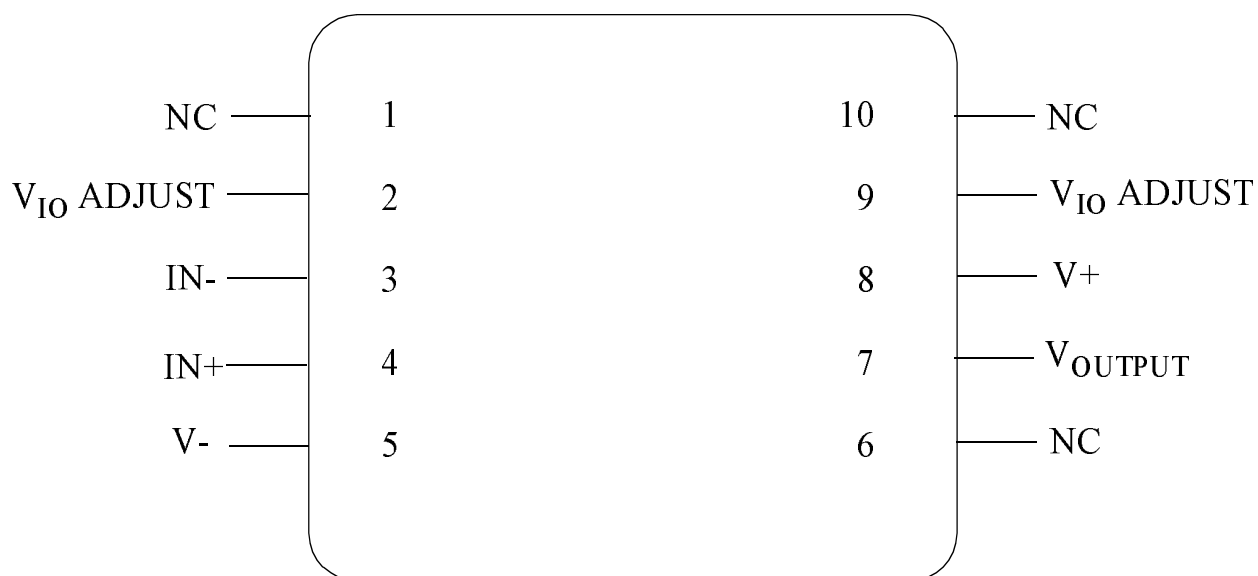
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LM6161J  
8 - LEAD DIP  
CONNECTION DIAGRAM  
TOP VIEW  
P000169A



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2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050

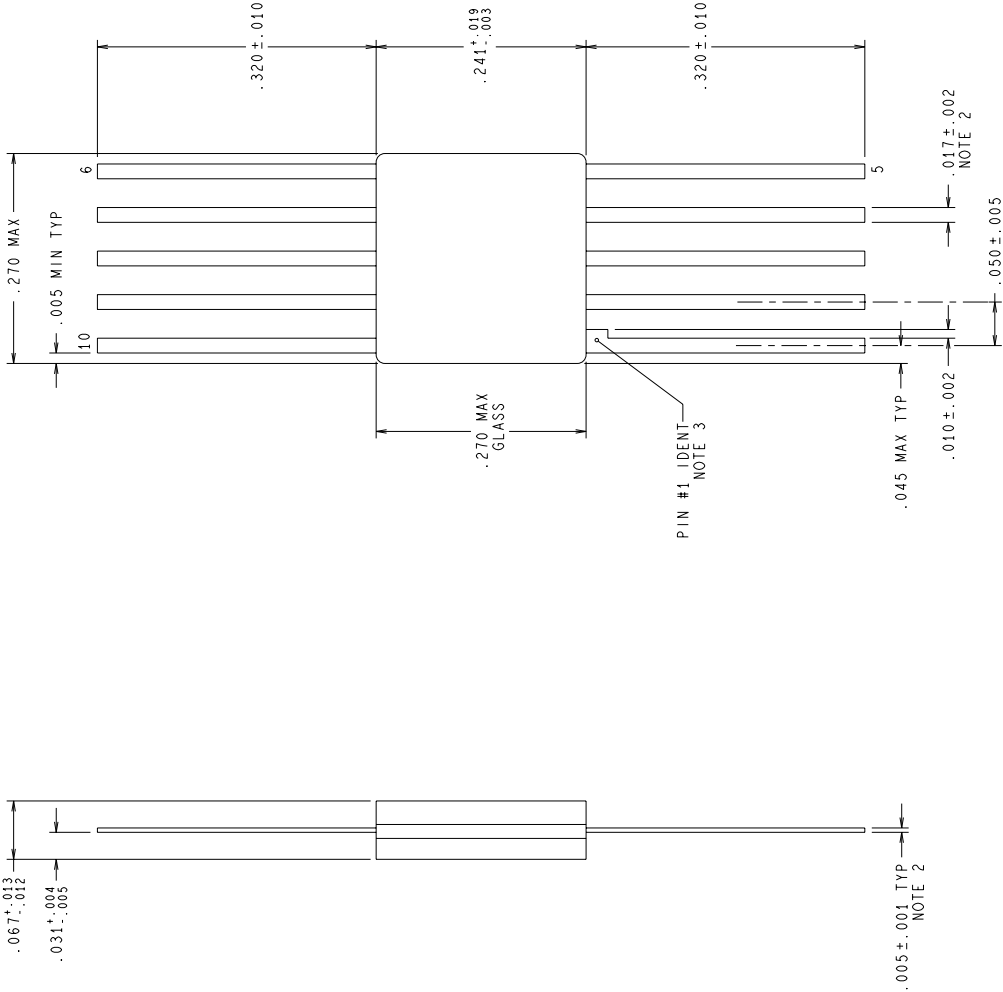


**LM6161WG**  
**10 - LEAD CERAMIC SOIC**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000259A**



National Semiconductor™  
 MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94 DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94 DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:  
a) A NOTCH OR OTHER MARK WITHIN THIS AREA  
b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-003, VARIATION AG, DATED 06/01/76.

MIL/AERO  
CONFIGURATION CONTROL

MIL-M-38510  
CONFIGURATION CONTROL

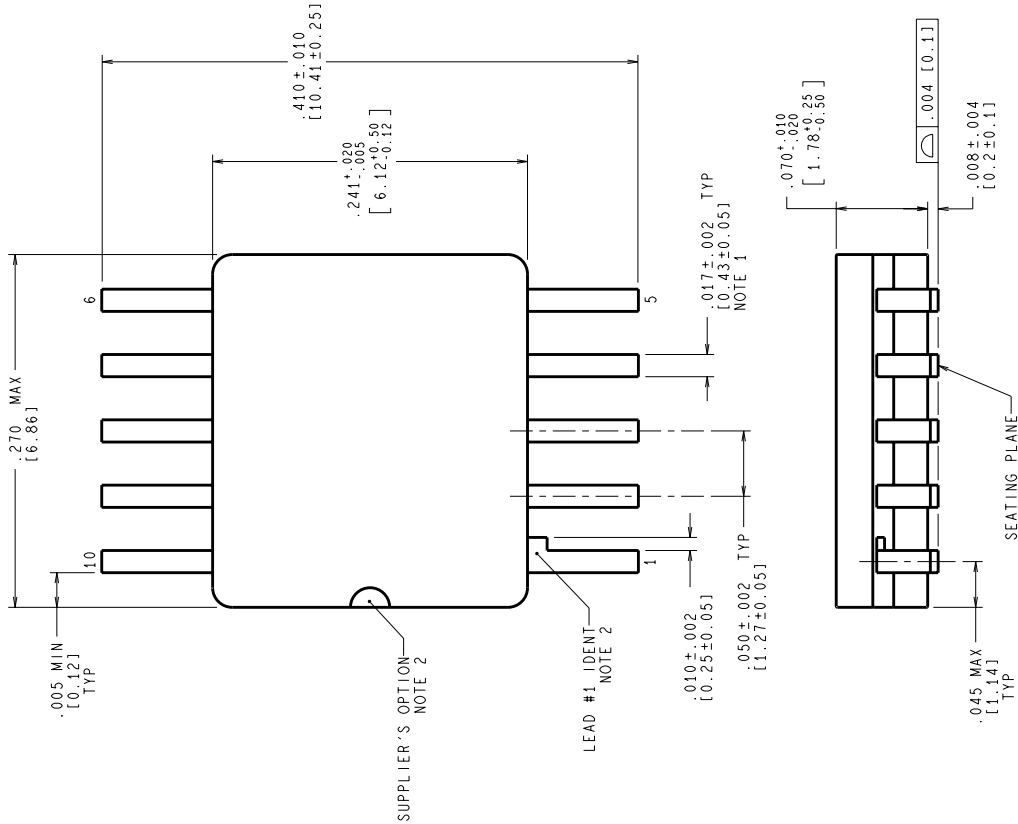
APPROVALS		DATE	
DESIGN	<i>D. F. Grady</i>	07/28/94	
DFTG. CHK.			
EMER. CHK.			
PROJECTION			
SCALE	N/A	SIZE	C
DRAWING NUMBER	MKT-W10A		
REV	G		
DO NOT SCALE DRAWING		SHEET 1 of 1	

**National Semiconductor**  
2000 Semiconductor dr., Santa Clara, CA 95052-8090

CERPACK, 10 LEAD

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996
B	LD PITCH TOL WAS $\pm .005$ ; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R .006 $\pm .002$ DIM .040 $\pm .003$ WAS .037 $\pm .003$	11441	04/19/1996
C	R .015(0.38) WAS R .006(0.15)	11838	10/08/1997

BY/APP'D	DATE	MS/KH



CONTROLLING DIMENSION IS INCH  
VALUES IN | | ARE MILLIMETERS

# MIL-PRF-38535 CONFIGURATION CONTROL

APPROVALS	DATE	DATE	DATE
DESIGN	MARYA SUCHY	02/29/96	
ENGINEER	CHK.		
TESTER	CHK.		
PROJECTION			
SCALE	N/A	SIZE	C
DRAWING NUMBER	(SC) MKT-WG10A	REV	C
DO NOT SCALE DRAWING			

**National Semiconductor**  
2000 Semiconductor Dr., Santa Clara, CA 95052-8000

**CERPACK,  
10 LEAD,  
GULL WING**

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICRONS. SOLDER MAY BE APPLIED OVER LEAD BASE METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
  - A NOTCH OR OTHER MARK WITHIN THIS AREA
  - A TAB ON LEAD 1, EITHER SIDE
- NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
1A1	M0002843	11/23/98	Barbara Lopez	Update MDS: MNL6161-X Rev. 0B0 to MNL6161-X Rev. 1A1. Updated NSID, deleted W-SMD and added WG ID. Added SMD number for WG package. Added WG package to thermal resistance, updated note 6, deleted note 7, added power dissipation limit in Absolute section. Updated Subgroups to match SMD, added note 2 to Electrical section. Added MKT graphic for WG package. Added Pinouts for all packages. Added Burn-In CKT for W and E packages.
2A1	M0003073	11/23/98	Rose Malone	Update MDS: MNL6161-X, Rev. 1A1 to MNL6161-X, Rev. 2A1.