National Semiconductor

MICROCIRCUIT DATA SHEET

MJLM148-X REV 0C1

Original Creation Date: 08/08/95
Last Update Date: 04/12/99
Last Major Revision Date: 08/08/95

QUAD OPERATIONAL, MEDIUM POWER, INTERNALLY COMPENSATED AMPLIFIER

General Description

The LM148 series is a true quad LM741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a LM741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple LM741 or LM1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Industry Part Number

LM148

Prime Die

LM148

Controlling Document

38510/11001, AMEND. 3 REV B

NS Part Numbers

JL148BCA
JL148BDA
JL148BZA
JL148SCA
JL148SDA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 741 op amp operating characteristics
- Low supply current drain 0.6mA/Amplifier
- Class AB output stage-no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 1mV
- Low input offset current 4nA
- Low input bias current 30nA
- Gain bandwidth product (Unity Gain) 1.0Mhz
- High degree of isolation between amplifiers 120dB
- Overload protection for input and outputs

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage		± 22V
Input Voltage Range		± 20V
Input Current Range		-0.1mA to 10mA
Differential Input Voltage Range (Note 2)		± 30V
Output Short Circuit Duration (Note 3)		Continuous
Power Dissipation (Note 4)		
(Pd at 25 C)		
CERDIP		400mW
CERPACK		350mW
Maximum Junction Temperature (TjMAX)		175 C
Operating Temperature Range		-55 C ≤ TA ≤ +125 C
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		300 C
Thermal Resistance		
ThetaJA		
CERDIP	(Still Air)	103 C/W
	(500LF/Min Air Flow)	52 C/W
CERPACK	(Still Air)	140 C/W
	(500LF/Min Air Flow)	100 C/W
CERAMIC SOIC	(Still Air)	176 C/W
	(500LF/Min Air Flow)	116 C/W
ThetaJC		
CERDIP		19 C/W
CERPACK		25 C/W
CERAMIC SOIC		25 C/W
Package Weight (Typcial)		
CERDIP		TBD
CERPACK		465mg
CERAMIC SOIC		415mg
ESD Tolerance (Note 5)		500V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: The differential input voltage range shall not exceed the supply voltage range.
Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shrted as the maximum junction temperature will be exceeded.
Note 4: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by TjMAX, ThetaJA, and the ambient temperature, TA. The maximum available power dissipation at any temperature is Pd=(TjMAX - TA)/ThetaJA or the 25 C PdMAX, whichever is less.
Note 5: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±20V, Vcm = 0V, measure each amplifier.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-5	5	mV	1
					-6	6	mV	2, 3
		+Vcc = 5V, -Vcc = -35V, Vcm = +15V			-5	5	mV	1
					-6	6	mV	2, 3
					-5	5	mV	1
					-6	6	mV	2, 3
		+Vcc = 5V, -Vcc = -5V			-5	5	mV	1
					-6	6	mV	2, 3
Delta Vio/Delta T	Input Offset Voltage Temperature Stability	25 C ≤ TA ≤ 125 C	1		-25	25	uV/C	2
		-55 C ≤ TA ≤ 25 C	1		-25	25	uV/C	3
Iio	Input Offset Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-25	25	nA	1, 2
					-75	75	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = +15V			-25	25	nA	1, 2
					-75	75	nA	3
					-25	25	nA	1, 2
					-75	75	nA	3
		+Vcc = 5V, -Vcc = -5V			-25	25	nA	1, 2
					-75	75	nA	3
Delta Iio/Delta T	Input Offset Current Temperature Stability	25 C ≤ TA ≤ 125 C	1		-200	200	pA/C	2
		-55 C ≤ TA ≤ 25 C	1		-400	400	pA/C	3
+Iib	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-0.1	100	nA	1, 2
					-0.1	325	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = +15V			-0.1	100	nA	1, 2
					-0.1	325	nA	3
					-0.1	100	nA	1, 2
					-0.1	325	nA	3
		+Vcc = 5V, -Vcc = -5V			-0.1	100	nA	1, 2
					-0.1	325	nA	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±20V, Vcm = 0V, measure each amplifier.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Iib	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-0.1	100	nA	1, 2
					-0.1	325	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = +15V			-0.1	100	nA	1, 2
					-0.1	325	nA	3
					-0.1	100	nA	1, 2
					-0.1	325	nA	3
		+Vcc = 5V, -Vcc = -5V			-0.1	100	nA	1, 2
					-0.1	325	nA	3
+PSRR	Power Supply Rejection Ratio	-Vcc = -20V, +Vcc = 20 to 10V	2		-100	100	uV/V	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+Vcc = 20V, -Vcc = -20 to -10V	2		-100	100	uV/V	1, 2, 3
CMR	Common Mode Rejection	±5V ≤ ±Vcc ≤ ±35V, Vcm = ±15V			76		dB	1, 2, 3

Electrical Characteristics

DC/AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±20V, Vcm = 0V, measure each amplifier.
AC: ±Vcc = ±20V, Vcm = 0V, measure each amplifier.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios+	Short Circuit Current	+Vcc = 15V, -Vcc = -15V, Vcm = -10V			-55		mA	1, 2
					-75		mA	3
Ios-	Short Circuit Current	+Vcc = 15V, -Vcc = -15V, Vcm = 10V				55	mA	1, 2
						75	mA	3
Icc	Power Supply Current	+Vcc = 15V, -Vcc = -15V				3.6	mA	1, 2
						4.5	mA	3
+Vop	Output Voltage Swing	Rl = 10K ohms			16		V	4, 5, 6
		Rl = 2K ohms			15		V	4, 5, 6
-Vop	Output Voltage Swing	Rl = 10K ohms				-16	V	4, 5, 6
		Rl = 2K ohms				-15	V	4, 5, 6
Avs-	Open Loop Voltage Gain	Vout = -15V, Rl = 10K Ohms			50		V/mV	4
					25		V/mV	5, 6
		Vout = -15V, Rl = 2K Ohms			50		V/mV	4
					25		V/mV	5, 6
Avs+	Open Loop Voltage Gain	Vout = +15V, Rl = 10K Ohms			50		V/mV	4
					25		V/mV	5, 6
		Vout = +15V, Rl = 2K Ohms			50		V/mV	4
					25		V/mV	5, 6
Avs	Open Loop Voltage Gain	±Vcc = ±5V, Vout = ±2V, Rl = 10K Ohms			10		V/mV	4, 5, 6
		±Vcc = ±5V, Vout = ±2V, Rl = 2K Ohms			10		V/mV	4, 5, 6
TR(tr)	Transient Response Time	Vin = 50mV, Av = 1				1	uS	7, 8A, 8B
TR(os)	Transient Response Time	Vin = 50mV, Av = 1				25	%	7, 8A, 8B
Sr+	Slew Rate	Vin = -5V to +5V, Av = 1			.2		V/uS	7, 8A, 8B
Sr-	Slew Rate	Vin = +5V to -5V, Av = 1			.2		V/uS	7, 8A, 8B

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: ±Vcc = ±20V, Vcm = 0V, measure each amplifier.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
NI(BB)	Noise (Broadband)	Bw = 10Hz to 5KHz				15	uVrms	7
NI(PC)	Noise (Popcorn)	Rs = 20K Ohms				40	uVpk	7
Cs	Channel Separation	Vin = ±10V, A to B, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, A to C, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, A to D, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, B to A, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, B to C, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, B to D, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, C to A, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, C to B, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, C to D, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, D to A, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, D to B, Rl = 2K Ohms			80		dB	7
		Vin = ±10V, D to C, Rl = 2K Ohms			80		dB	7

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±20V, Vcm = 0V, measure each amplifier. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

Vio	Input Offset Voltage				-1	1	mV	1
+Iib	Input Bias Current				-15	15	nA	1
-Iib	Input Bias Current				-15	15	nA	1

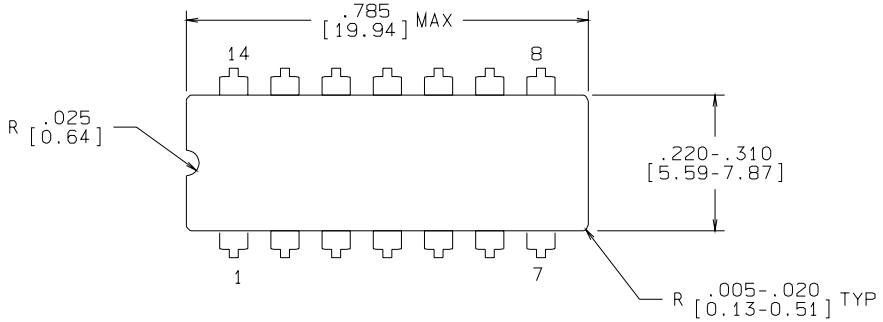
Note 1: Calculated Parameter.
Note 2: Datalogs as uV.

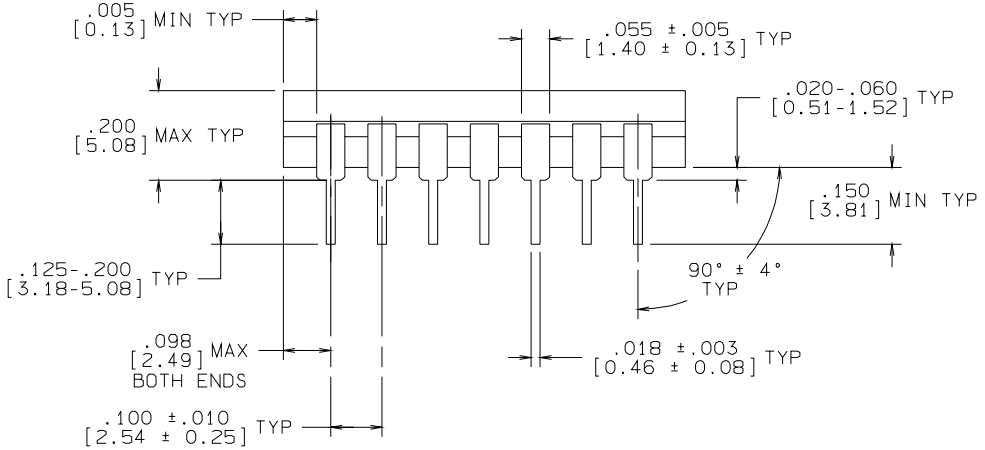
Graphics and Diagrams

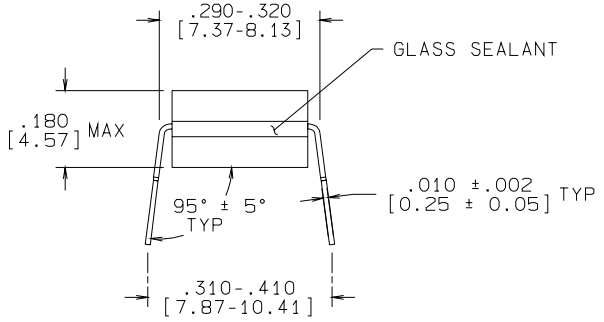
GRAPHICS#	DESCRIPTION
05324HRA2	CERDIP (J), 14LD (B/I CKT)
06203HRA2	CERPACK (W), 14LD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000229A	CERDIP (J), 14 LEAD (PINOUT)
P000367A	CERPACK (W), 14 LEAD (PINOUT)
P000370A	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)
WG14ARB	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

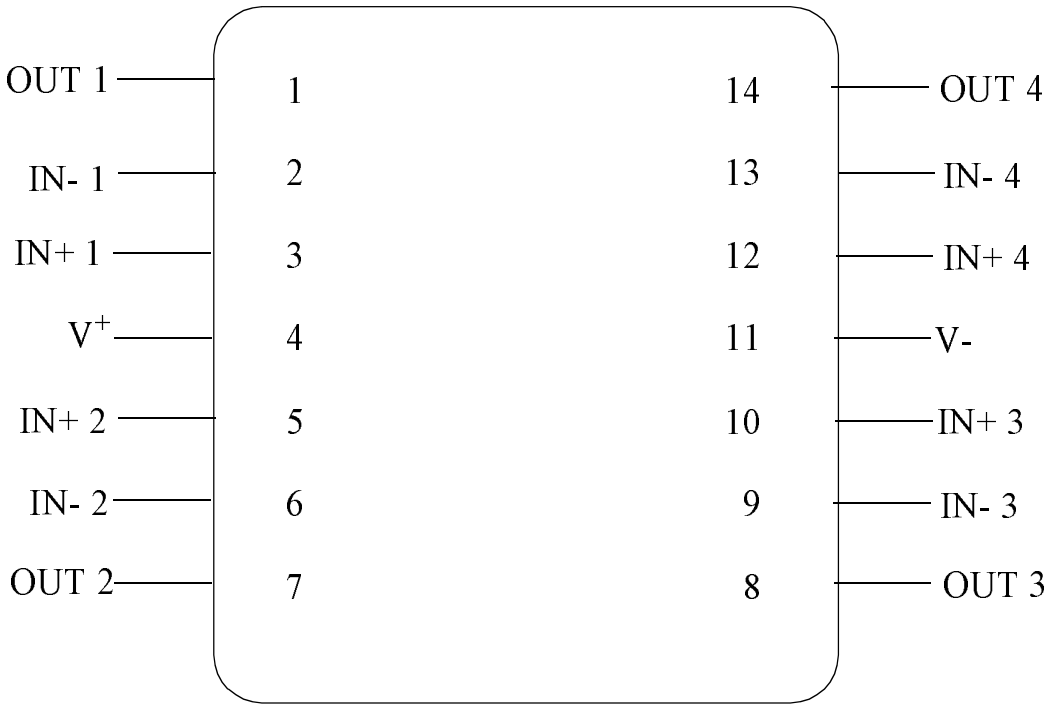
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

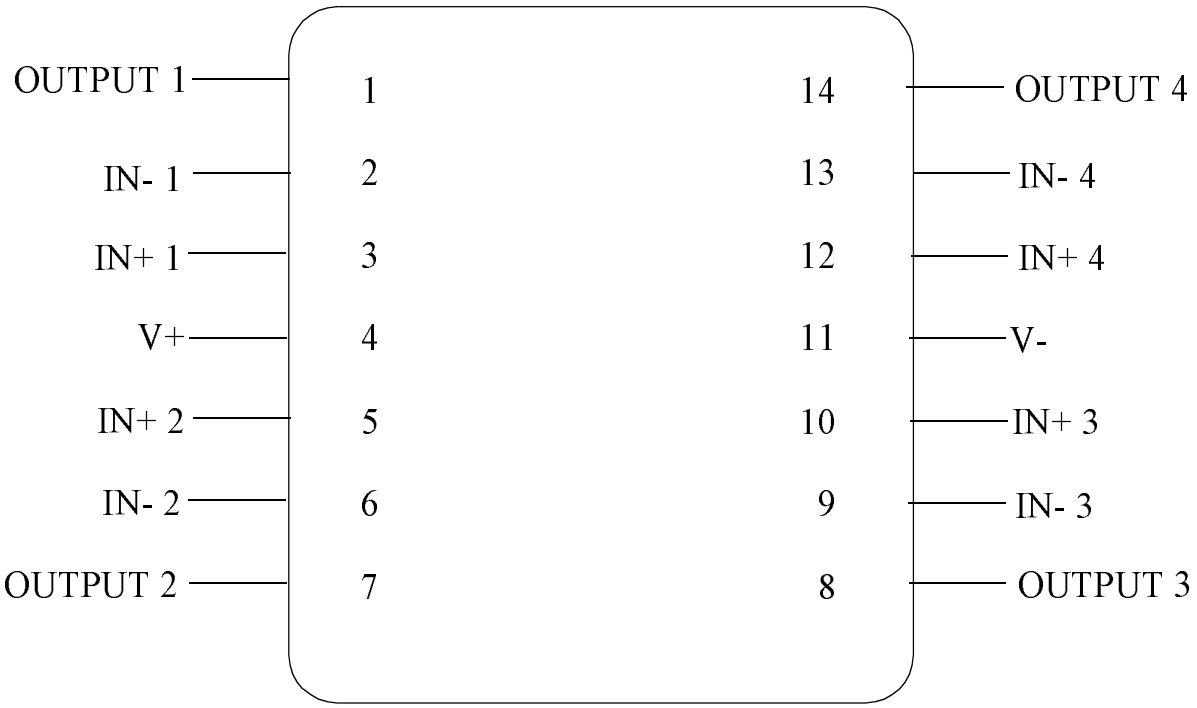
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM148J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000229A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM148W

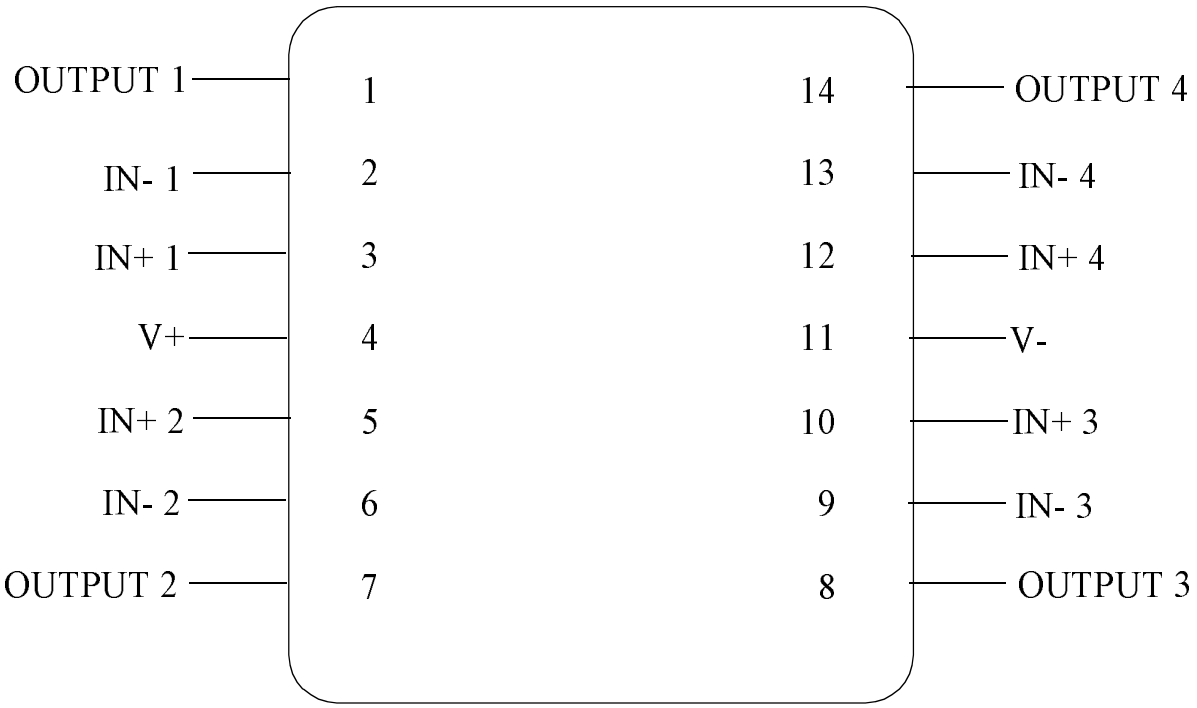
14 - LEAD CERPACK

CONNECTION DIAGRAM

TOP VIEW

P000367A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM148WG

14 - LEAD CERAMIC SOIC

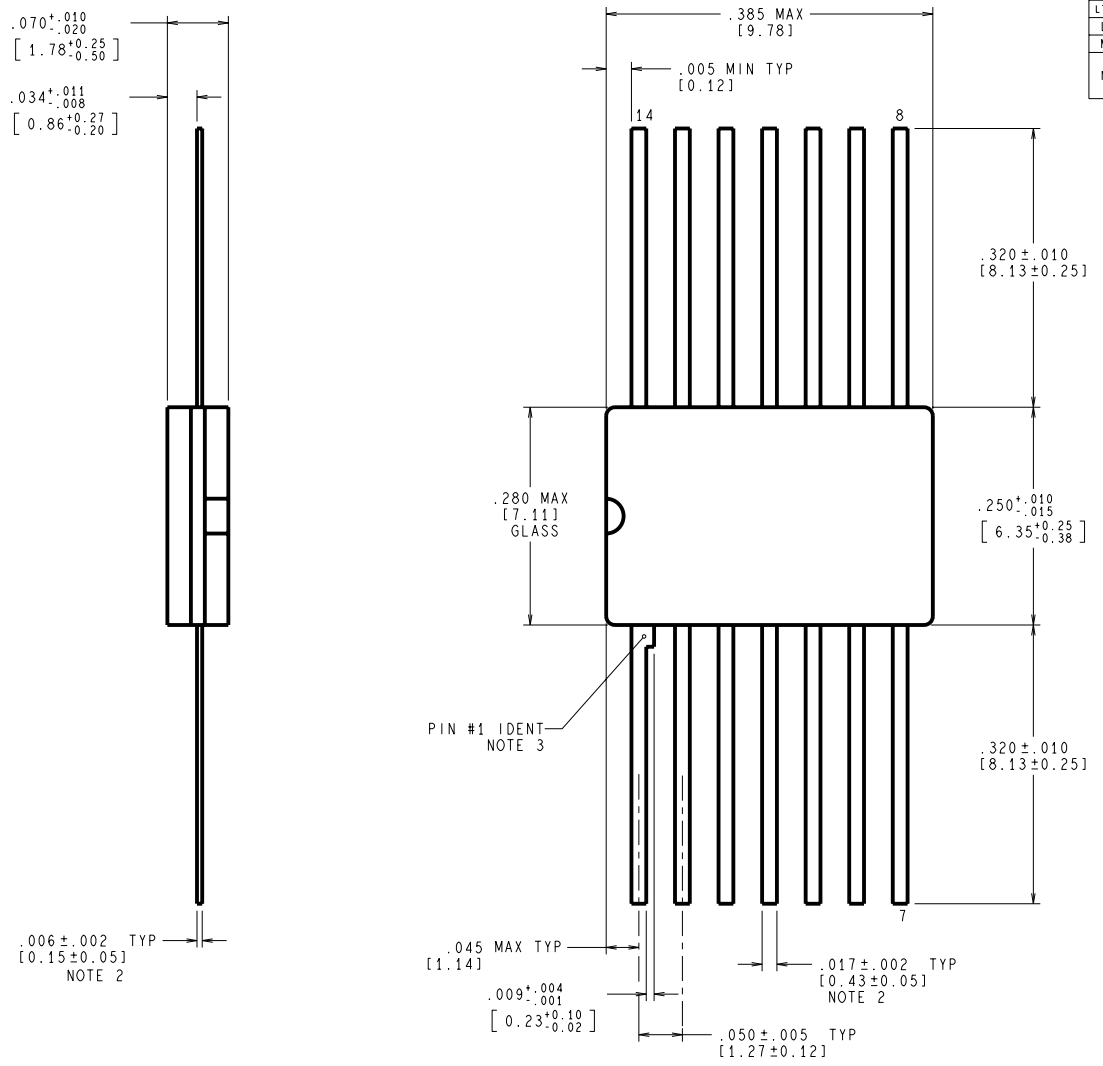
CONNECTION DIAGRAM

TOP VIEW

P000370A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

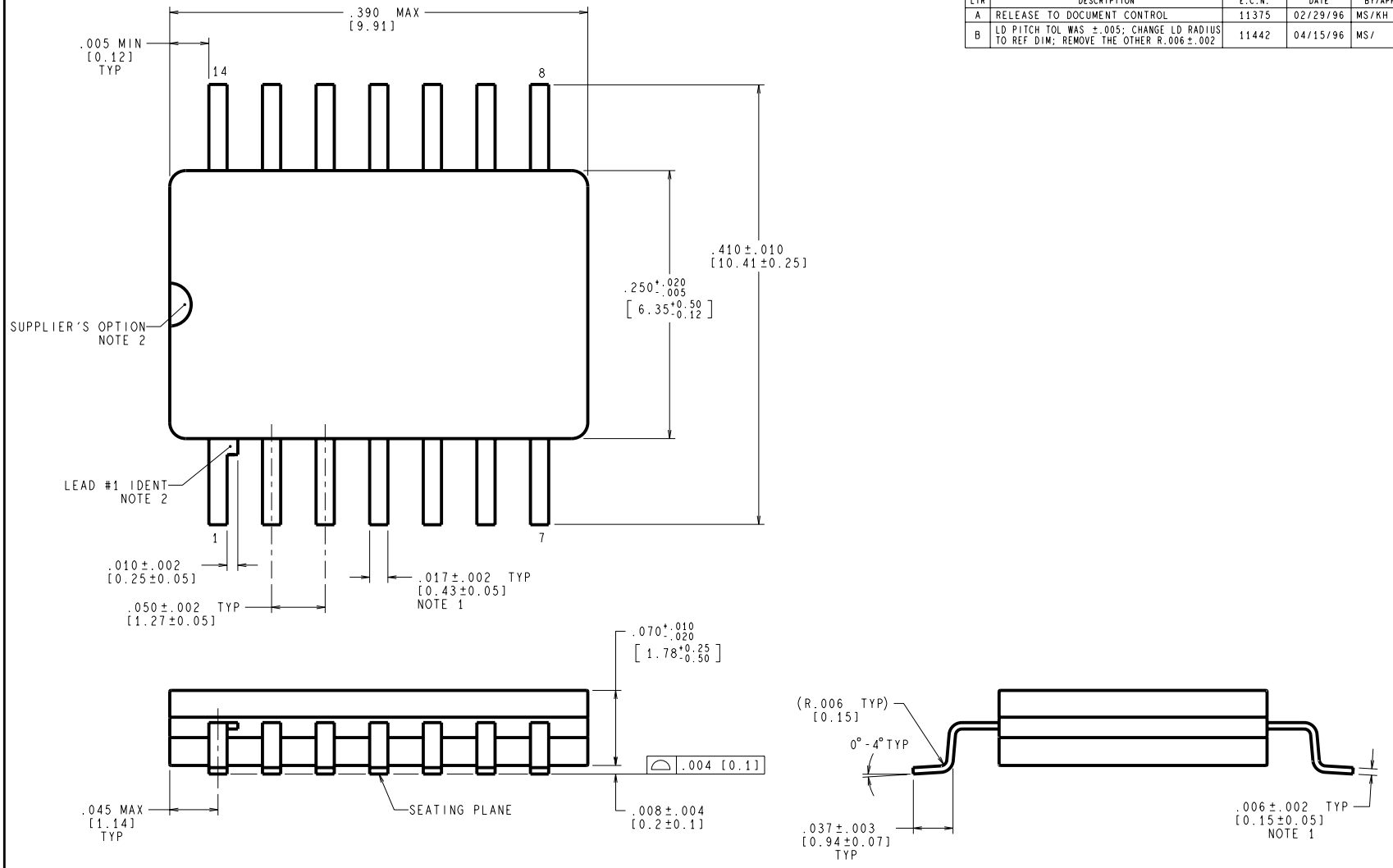
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/96	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002	11442	04/15/96	MS/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
14 LEAD,
GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-WG14A	B

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0C1	M0003344	04/12/99	Rose Malone	Update MDS: MJLM148-X, Rev. 0B0 to MJLM148-X, Rev. 0C1. Added reference to JL148BZA to Main Table, Absolute Section and graphics.