National Semiconductor

MICROCIRCUIT DATA SHEET

MJLM111-X REV 0C1

Original Creation Date: 08/18/95
Last Update Date: 08/24/98
Last Major Revision Date: 09/05/96

VOLTAGE COMPARATOR

General Description

The LM111, is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 and LM710. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111, can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

Industry Part Number

LM111

Prime Die

LM111

Controlling Document

38510/10304, AMEND.1 REV E

NS Part Numbers

JL111BCA
JL111BGA
JL111BHA
JL111BPA
JL111SGA
JL111SHA
JL111SPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Low Input Bias Current.
- Low Input Offset Current.
- Wide Differential Input Voltage.
- Power Supply Voltage, Single 5V to ±15V.
- Offset Voltage Null Capability.
- Strobe Capability.

(Absolute Maximum Ratings)
(Note 1)

Positive Supply Voltage		+30.0V
Negative Supply Voltage		-30.0V
Total Supply Voltage		36V
Output to Negative Supply Voltage		50V
GND to Negative Supply Voltage		30V
Differential Input Voltage		±30V
Sink Current		50mA
Input Voltage (Note 2)		±15V
Power Dissipation (Note 3)		
14 Ld DIP-Package		400mW at 25 C
8 Ld Metal Can-Package		330mW at 25 C
10 Ld Flatpack-Package		330mW at 25 C
8 Ld DIP-Package		400mW at 25 C
Output Short Circuit Duration		10 sec.
Maximum Strobe Current		10mA
Operating Temperature Range		-55 C to 125 C
Thermal Resistance		
ThetaJA		
14 Ld DIP	(Still Air @ 0.5W)	TBD
	(500LF/Min Air flow @ 0.5W)	TBD
8 Ld Metal Can Pkg	(Still Air @ 0.5W)	162 C/W
	(500LF/Min Air flow @ 0.5W)	92 C/W
10 Ld Flatpack	(Still Air @ 0.5W)	231 C/W
	(500LF/Min Air flow @ 0.5W)	153 C/W
8 Ld DIP	(Still Air @ 0.5W)	TBD
	(500LF/Min Air flow @ 0.5W)	TBD
ThetaJC		
14 Ld DIP		TBD
8 Ld Metal Can Pkg		50 C/W
10 Ld Flatpack		24 C/W
8 Ld DIP		TBD
Storage Temperature Range		-65 C to 150 C
Maximum Junction Temperature		175 C
Lead Temperature (Soldering, 60 seconds)		300 C
Voltage at Strobe Pin		V+ -5V
ESD Rating (Note 4)		300V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
Note 2: This rating applies for ±15V supplies. The positive input voltage limits is 30V above the negative supply. The negative input voltage limits is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.
Note 4: Human body model, 1.5k Ohms in series with 100pF.

Recommended Operating Conditions

Supply Voltage	Vcc = ±15Vdc
Amp Operating Temperature Range	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = +2.5V, -Vcc = -2.5V, Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
Vio(R)	Raised Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
Iio	Input Offset Current	Vin = 0V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
Iio(R)	Raised Input Offset Current	Vin = 0V, Rs = 50K Ohms			-25	+25	nA	1, 2
					-50	+50	nA	3
Iib+	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-100	0.1	nA	1, 2
					-150	0.1	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib-	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-100	0.1	nA	1, 2
					-150	0.1	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
Vo(STB)	Collector Output Voltage (ST)	Vin+ = Gnd, Vin- = 15V, Istb = -3mA, Rs = 50 Ohms	1		14		V	1, 2, 3
CMR	Common Mode Rejection	-28V≤-Vcc≤-0.5V, Rs=50 Ohms, 2V≤+Vcc≤29.5V, Rs=50 Ohms, -14.5V≤Vcm≤13V,Rs=50 Ohms			80		dB	1, 2, 3
Vol	Low Level Output Voltage	+Vcc = 4.5V, -Vcc = Gnd, Iout = 8mA, ±Vin = 0.5V, Vid = -6mV				0.4	V	1, 2, 3
		+Vcc = 4.5V, -Vcc = Gnd, Iout = 8mA, ±Vin = 3V, Vid = -6mV				0.4	V	1, 2, 3
		Iout = 50mA, ±Vin = 13V, Vid = -5mV				1.5	V	1, 2, 3
		Iout = 50mA, ±Vin = -14V, Vid = -5mV				1.5	V	1, 2, 3
Icex	Output Leakage Current	+Vcc = 18V, -Vcc = -18V, Vout = 32V			-1	10	nA	1
					-1	500	nA	2
Ii	Input Leakage Current	+Vcc = 18V, -Vcc = -18V, +Vin = +12V, -Vin = -17V	7		-5	500	nA	1, 2, 3
		+Vcc = 18V, -Vcc = -18V, +Vin = -17V, -Vin = +12V	7		-5	500	nA	1, 2, 3
Icc+	Power Supply Current					6	mA	1, 2
						7	mA	3
Icc-	Power Supply Current				-5		mA	1, 2
					-6		mA	3
Delta Vio/Delta T	Temperature Coefficient Input Offset Voltage	25 C ≤ T ≤ 125 C			-25	25	uV/ C	2
		-55 C ≤ T ≤ 25 C			-25	25	uV/ C	3
Delta Iio/Delta T	Temperature Coefficient Input Offset Current	25 C ≤ T ≤ 125 C			-100	100	pA/ C	2
		-55 C ≤ T ≤ 25 C			-200	200	pA/ C	3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios	Short Circuit Current	Vout = 5V, t ≤ 10mS, Vin- = 0.1V, Vin+ = 0V	3, 5			200	mA	1
		Vout = 5V, t ≤ 10mS, Vin- = 0.1V, Vin+ = 0V	3, 5			150	mA	2
		Vout = 5V, t ≤ 10mS, Vin- = 0.1V, Vin+ = 0V	3, 5			250	mA	3
Vio(adj)+	Input Offset Voltage (Adjustment)	Vout = 0V, Vin = 0V, Rs = 50 Ohms	3		5		mV	1
Vio(adj)-	Input Offset Voltage (Adjustment)	Vout = 0V, Vin = 0V, Rs = 50 Ohms	3			-5	mV	1
Ave+	Voltage Gain (Emitter)	Rl = 600 Ohms	3, 6		10		V/mV	4
			3, 6		8		V/mV	5, 6
Ave-	Voltage Gain (Emitter)	Rl = 600 Ohms	3, 6		10		V/mV	4
			3, 6		8		V/mV	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: ±Vcc = ±15V, Vcm = 0

trLHC	Response Time (Collector Output)	Vod(Overdrive) = -5mV, Cl = 50pF, Vin = -100mV	4			300	nS	7, 8B
			4			640	nS	8A
trHLC	Response Time (Collector Output)	Vod(Overdrive) = 5mV, Cl = 50pF, Vin = 100mV	4			300	nS	7, 8B
			4			500	nS	8A

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-0.5	0.5	mV	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-0.5	0.5	mV	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-0.5	0.5	mV	1
Iib+	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-12.5	12.5	nA	1
Iib-	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-12.5	12.5	nA	1
Icex	Output Leakage Current	+Vcc = 18V, -Vcc = -18V, Vout = 32V			-5	5	nA	1

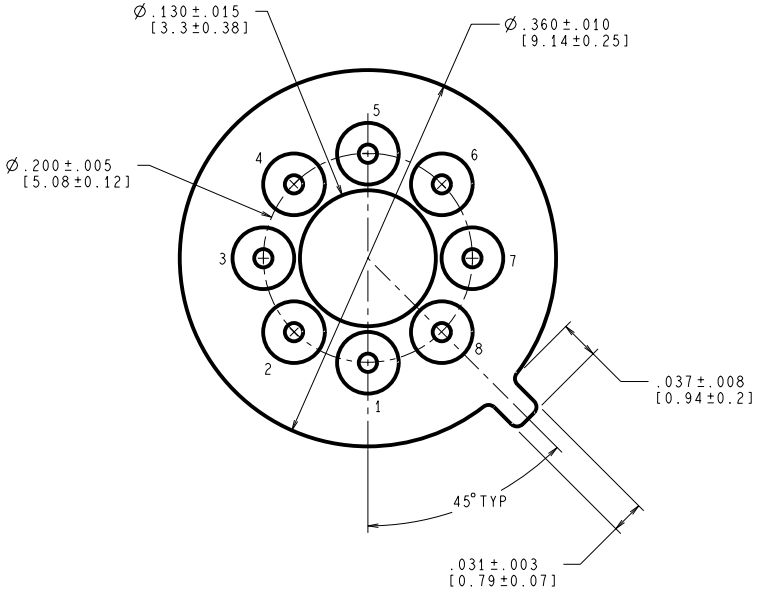
Note 1: Istb = -2mA at -55 C.
Note 2: Calculated parameter.
Note 3: Use DC tape for Ios and Vio(adj), Ave+ and Ave- as indicated in TAPE NAME section of this JRETS.
Note 4: Uses AC tape and hardware.
Note 5: Actual min. limit used is 5mA due to test setup.
Note 6: Datalog reading in K = V/mV.
Note 7: Vid is voltage difference between inputs.

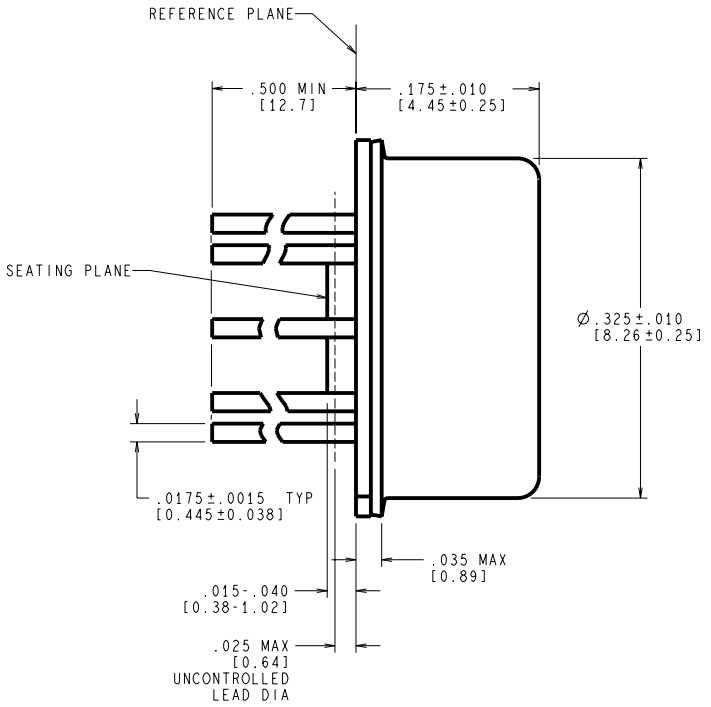
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05172HRB2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
05174HRC2	CERPACK (W), 10 LEAD (B/I CKT)
05284HRC2	METAL CAN (H), TO-39, 3LD .200 DIA P.C. (B/I CKT)
05349HRE2	CERDIP (J), 14 LEAD (B/I CKT)
05445HRC	CERDIP (J), 8 LEAD (B/I CKT)
05652HRA2	CERDIP (J), 8 LEAD (B/I CKT)
09569HRC2	CERPACK (W), 10 LEAD (B/I CKT)
09570HRC2	CERDIP (J), 14 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000151A	METAL CAN (H), TO-99, 8LD .200 DIA P.C.(PIN OUT)
P000152A	CERPACK (W), 10 LEAD (PIN OUT)
P000153A	CERDIP (J), 8 LEAD (PIN OUT)
P000387A	CERDIP (J), 14 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
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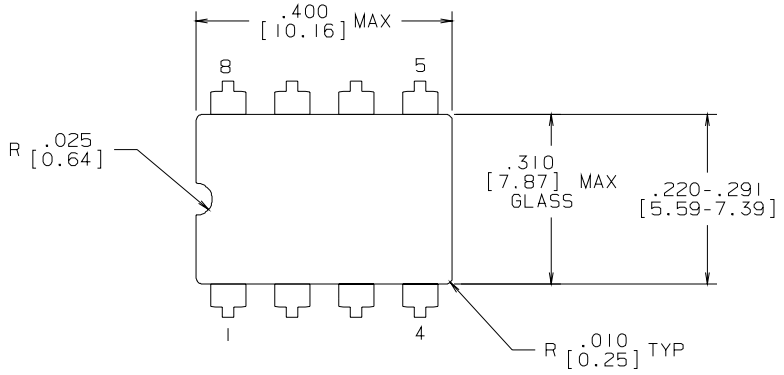

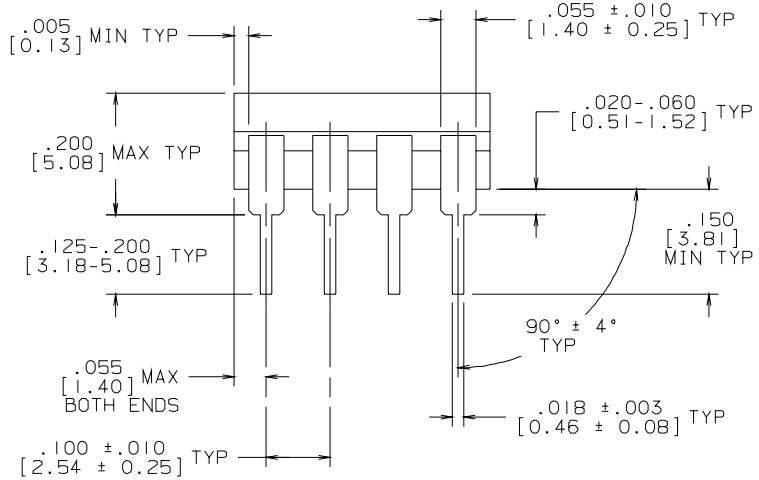

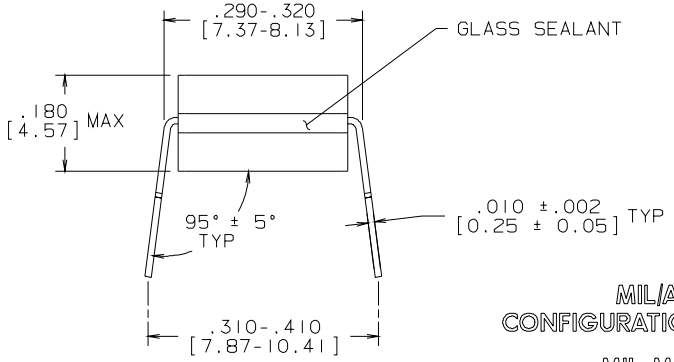

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
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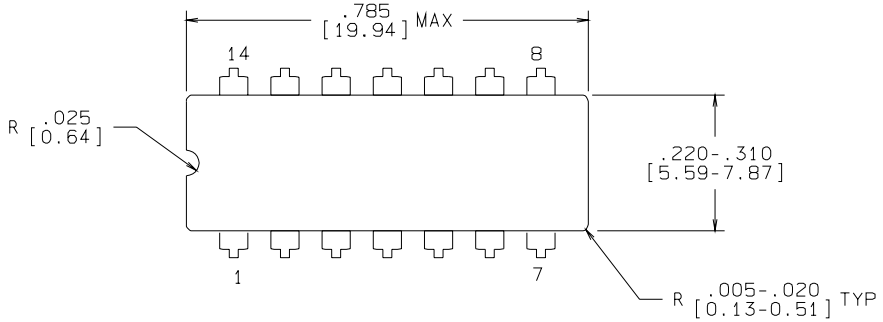
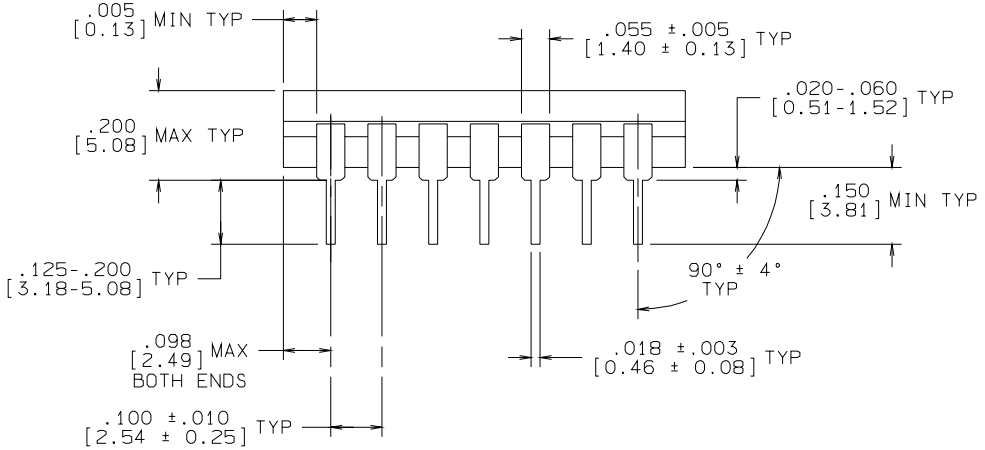
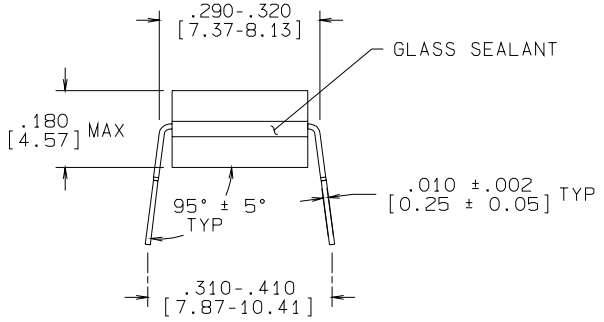






CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

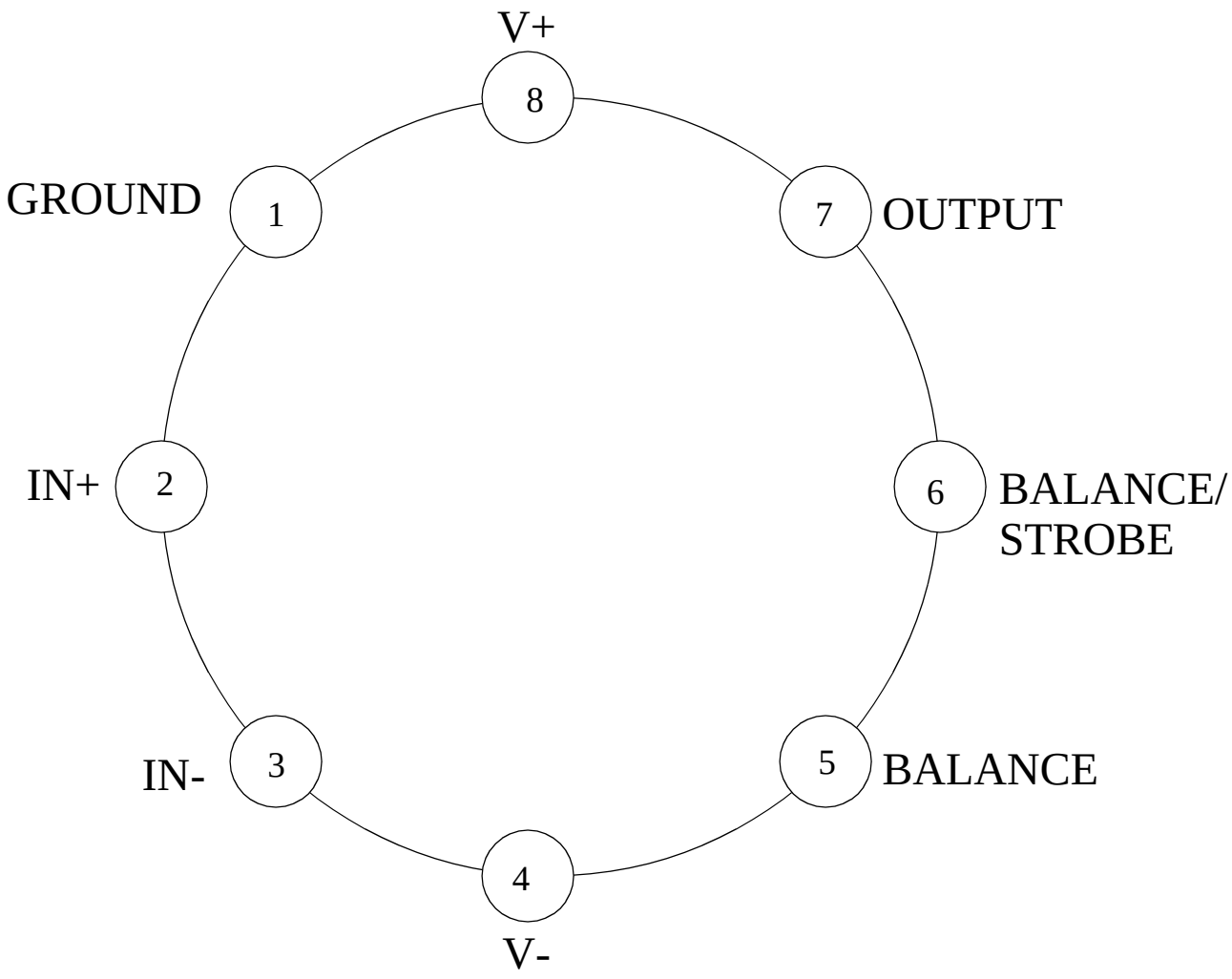
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

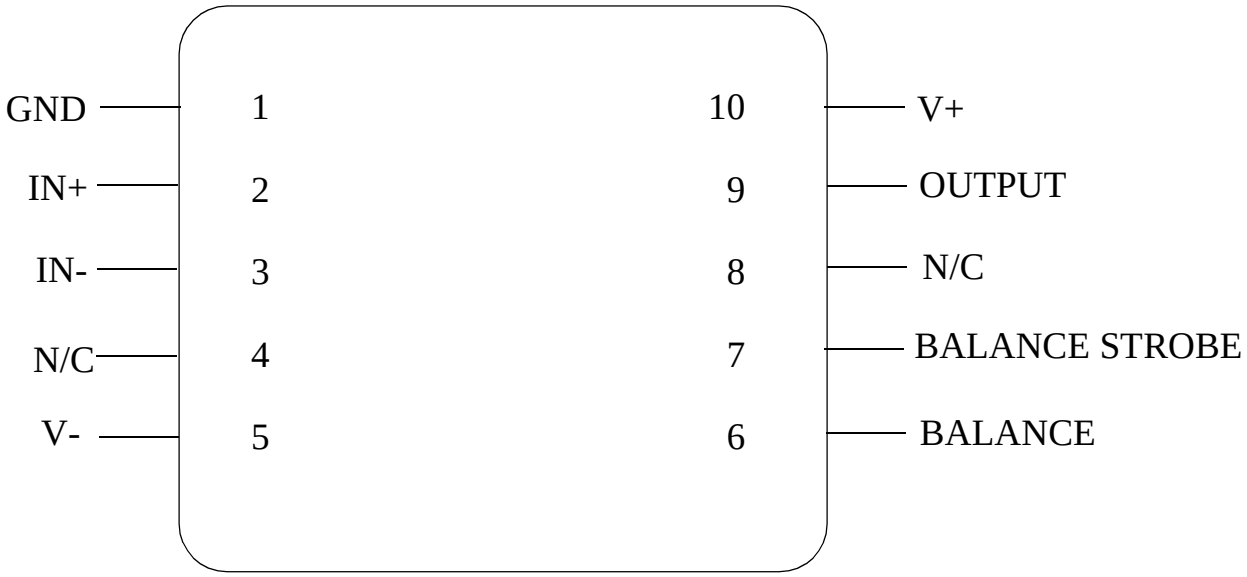
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



JL111H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000151A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



JL111W

10 - LEAD CERPACK

CONNECTION DIAGRAM
TOP VIEW

P000152A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

JL111J-8

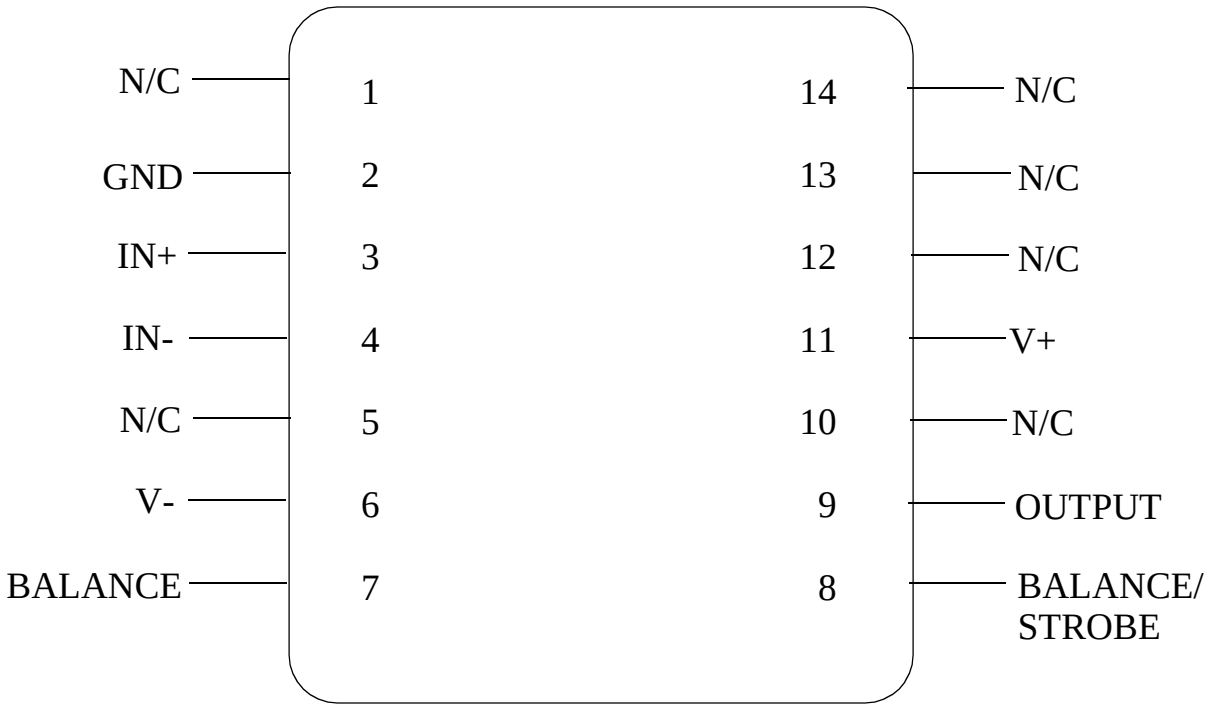
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000153A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



JL111J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000387A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
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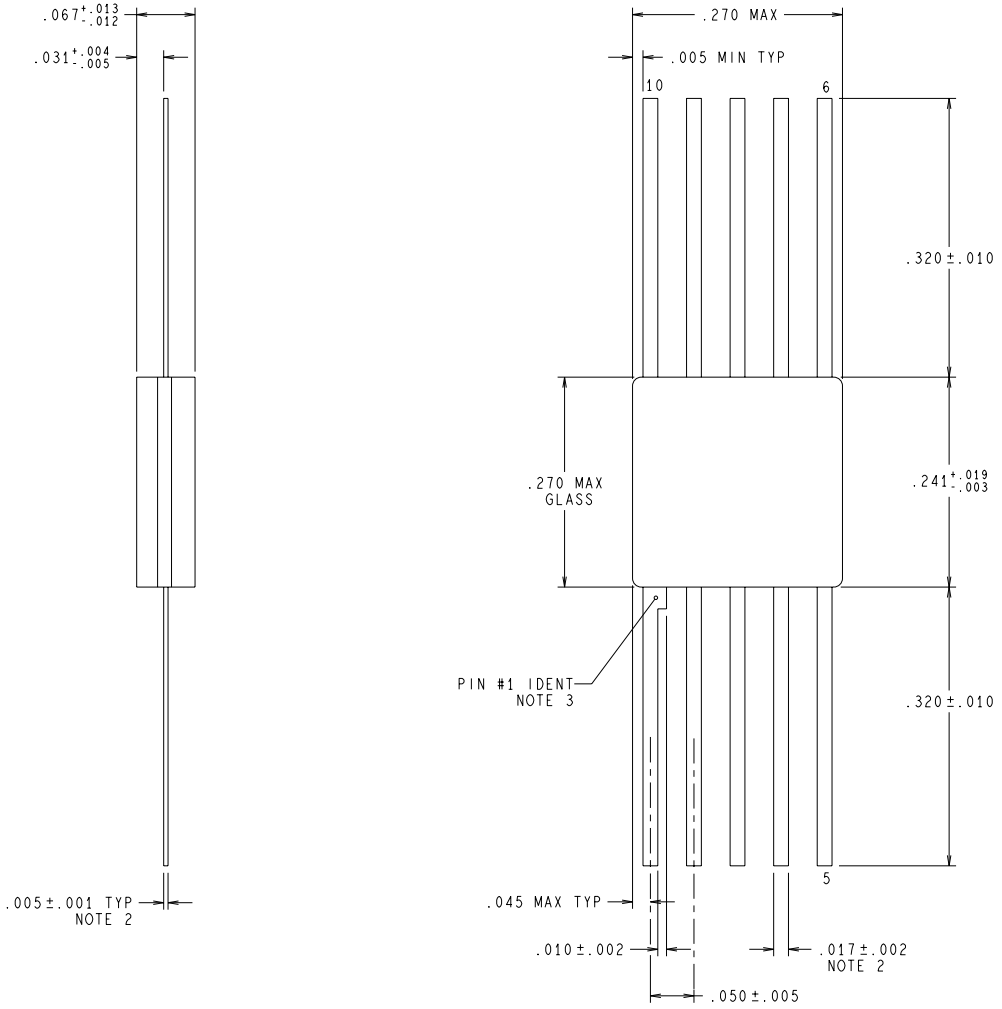

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION — INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0C1	M0003013	08/24/98	Rose Malone	Update MDS: MJLM111-X Rev. 0B0 to MJLM111-X Rev. 0C1. Updated Power Dissipation Condition, Added Thermal Data and Burn-In Ckts for all packages. Changed Pinout P000150A to P000387A to match Data Base.