National Semiconductor

MICROCIRCUIT DATA SHEET

MDLM139A-X REV 0B1

Original Creation Date: 07/14/95
Last Update Date: 03/27/98
Last Major Revision Date: 07/14/95

LOWER POWER LOW OFFSET VOLTAGE QUAD COMPARATOR

General Description

The LM139A consists of four independent precision voltage comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139A was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic- where the low power drain of the LM139A is a distinct advantage over standard comparators.

Industry Part Number

LM139A

NS Part Numbers

LM139AE-SMD *
LM139AJ-SMD **
LM139AW-SMD ***
LM139AWG-SMD ****

Prime Die

LM139

Controlling Document

See Features Page

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply voltage range
  LM139A series, 2 Vdc to 28 Vdc
- Very low supply current drain (0.8 mA) - independent of supply voltage.
- Low input biasing current 25 nA
- Low input offset current $\pm$5 nA
  and offset voltage $\pm$1 mV
- Input common-mode voltage range includes ground.
- Differential input voltage range equal to the power supply voltage.
- Low output saturation voltage. 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.
- SMD : 5962-87739012A*, 01CA**, 01DA***, 01XA****

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage, V+	36 Vdc or ±18 Vdc
Differential Input Voltage (Note 5)	36 Vdc
Input Voltage	-0.3 Vdc to +36 Vdc
Input Current (Vin<-0.3 Vdc) (Note 6)	50mA
Power Dissipation (Note 2, 3)	
LCC	1250mW
CERDIP	1200mW
CERPACK	680mW
SOIC	680mW
Sink Current (approx.)	20mA
Output Short Circuit to GND (Note 4)	Continuous
Storage Temperature Range	-65 C to +150 C
Maximum Junction Temperature	150 C
Lead Temperature (Soldering, 10 seconds)	300 C
Operating Temperature Range	-55 C to +125 C
Thermal Resistance	
ThetaJA	
LCC (Still Air)	100 C/W
LCC (500LF/Min Air flow)	73 C/W
CERDIP (Still Air)	103 C/W
CERDIP (500LF/Min Air flow)	65 C/W
CERPACK (Still Air)	183 C/W
CERPACK (500LF/Min Air flow)	120 C/W
SOIC (Still Air)	183 C/W
SOIC (500LF/Min Air flow)	120 C/W
ThetaJC	
LCC	28 C/W
CERDIP	23 C/W
CERPACK	23 C/W
SOIC	23 C/W
ESD Tolerance (Note 7)	600V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guaranteed specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The low bias dissipation and the ON-OFF characteristics of the outputs keeps the chip dissipation very small (Pd $\leq$ 100mW), provided the output transistors are allowed to saturate.

Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20mA independent of the magnitude of V+.

Note 5: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 Vdc(or 0.3 Vdc below the magnitude of the negative power supply, if used) (at 25 C).

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward baised and thereby acting as input diode clamps. In addition to the diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 Vdc (at 25 C).

Note 7: Human body model, 1.5K Ohms in series with 100pF.

Recommended Operating Conditions

Supply Voltage	5Vdc to 30Vdc
Ambient Operating Temperature Range	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+ = 5V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Supply Current	V+ = 30V, Rl = Infinity				3	mA	1, 2, 3
		Rl = Infinity				3	mA	1, 2, 3
Icex	Output Leakage Current	V+ = 30V, Vin(-) = 0V, Vin(+) ≥ 1V, Vo = 30V				0.5	uA	1
		V+ = 30V, Vin(-) = 0V, Vin(+) ≥ 1V, Vo = 30V				1	uA	2, 3
Vsat	Saturation Voltage	Isink ≤ 4mA, Vin(-) = 1V, Vin(+) = 0V				400	mV	1
		Isink ≤ 4mA, Vin(-) = 1V, Vin(+) = 0V				700	mV	2, 3
Isink	Output Sink Current	Vo ≥ 1.5V, Vin(-) = 1V, Vin(+) = 0V			6		mA	1
Vio	Input Offset Voltage	Rs = 0 Ohm			-2	2	mV	1
					-4	4	mV	2, 3
		V+ = 30V, Rs = 0 Ohm			-2	2	mV	1
					-4	4	mV	2, 3
		V+ = 30V, Vcm = 28V, Vo = 1.4V, Rs = 0 Ohm			-2	2	mV	1
					-4	4	mV	2, 3
+Iib	Input Bias Current	Vo = 1.5V			-100	-1	nA	1
					-300	-1	nA	2, 3
-Iib	Input Bias Current	Vo = 1.5V			-100	-1	nA	1
					-300	-1	nA	2, 3
Iio	Input Offset Current	Vo = 1.5V			-25	25	nA	1
					-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	V+ = 5V to 30V			70		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	V+ = 30V, Vcm = 0V to 28V, Rl ≥ 15K Ohms			70		dB	1, 2, 3
Av	Voltage Gain	V+ = 15V, Rl ≥ 15K Ohms, Vo = 1V to 11V			50		V/mV	4
		V+ = 15V, Rl ≥ 15K Ohms, Vo = 1V to 11V			25		V/mV	5, 6
Vcm	Common Mode Voltage Range	V+ = 30V	1		0	V+-2	V	1, 2, 3
		V+ = 5V	1		0	V+-2	V	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+ =5V, 100mV Input Step

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tRLH	Response Time	Vod = 5mV, Rl = 5.1K Ohms				5	uS	9
tRHL	Response Time	Vod = 5mV, Rl = 5.1K Ohms				2.5	uS	9

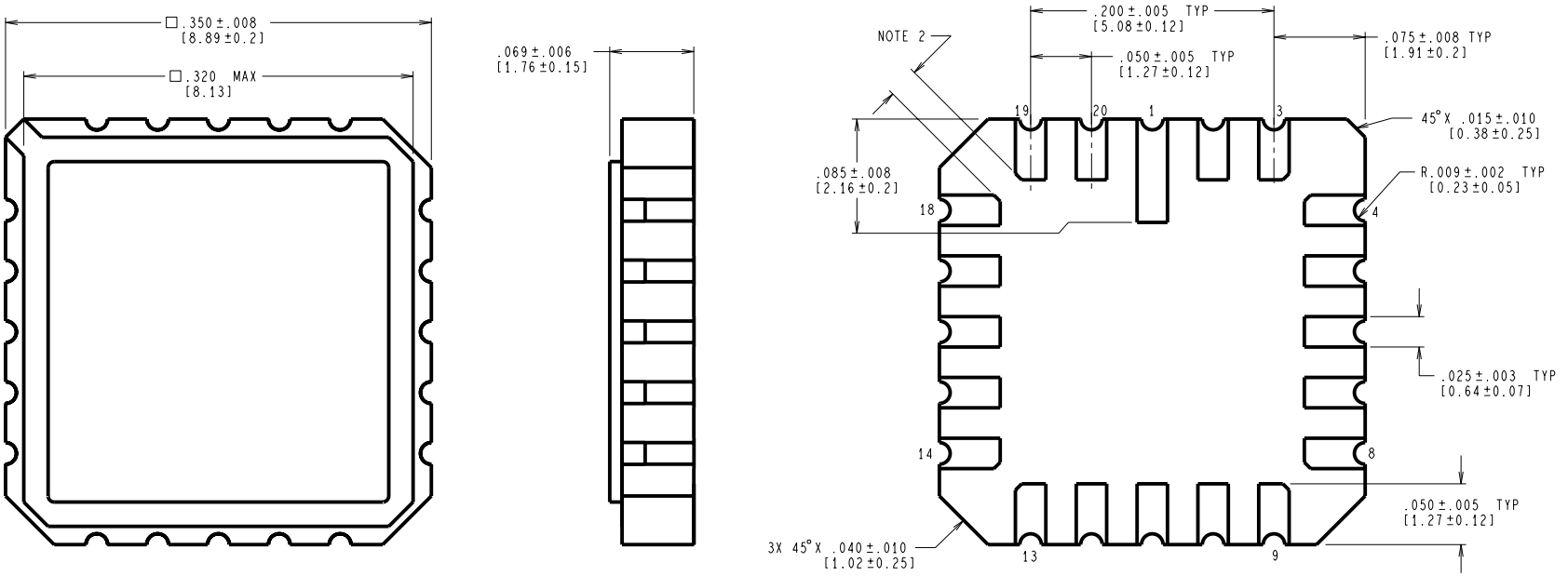
Note 1: Parameter guaranteed by Vio tests.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
5542HRA2	(blank)
5715HRA2	CERPACK (W), 14 LEAD (B/I CKT)
5816HRA3	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000184A	CERPACK (W), 14 LEAD (PINOUT)
P000201A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)
P000238A	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
P000271A	CERDIP (J), 14 LEAD (PINOUT)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

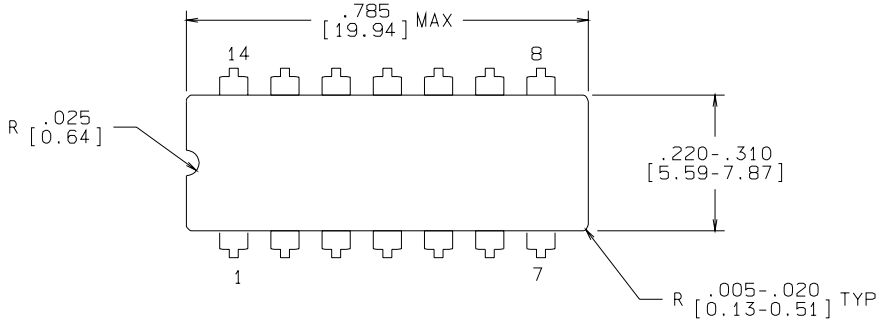
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

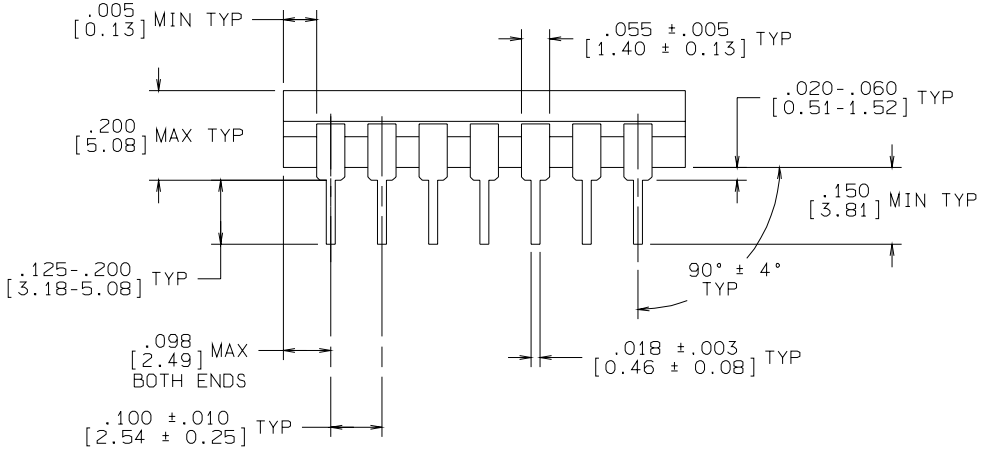
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

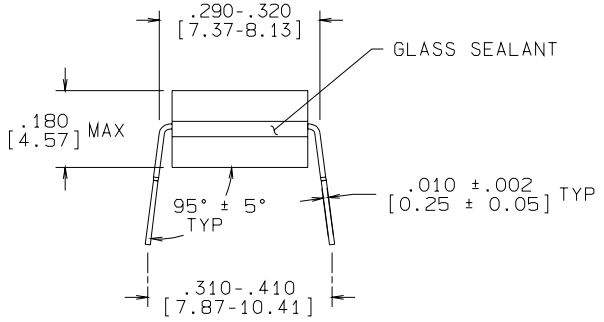
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

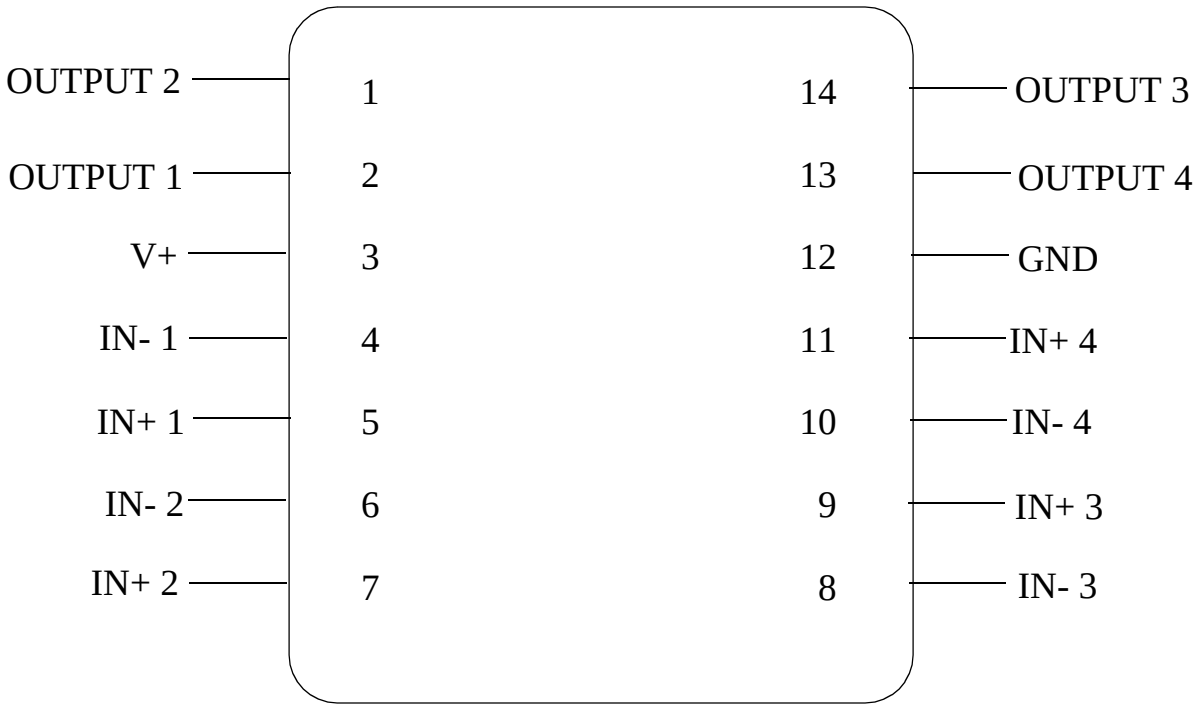
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

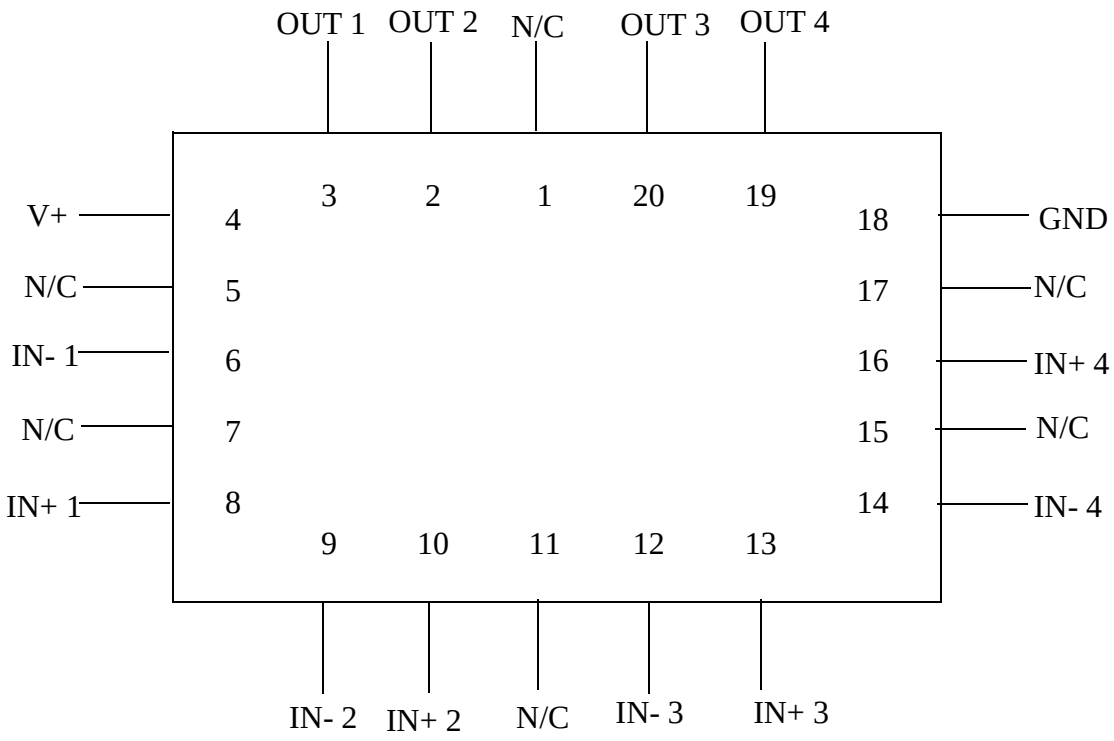
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM139AW, LM139W
14 - LEAD CERPACK
CONNECTION DIAGRAM
TOP VIEW
P000184A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM139AE, LM139E

20 - LEAD LCC

CONNECTION DIAGRAM

TOP VIEW

P000201A

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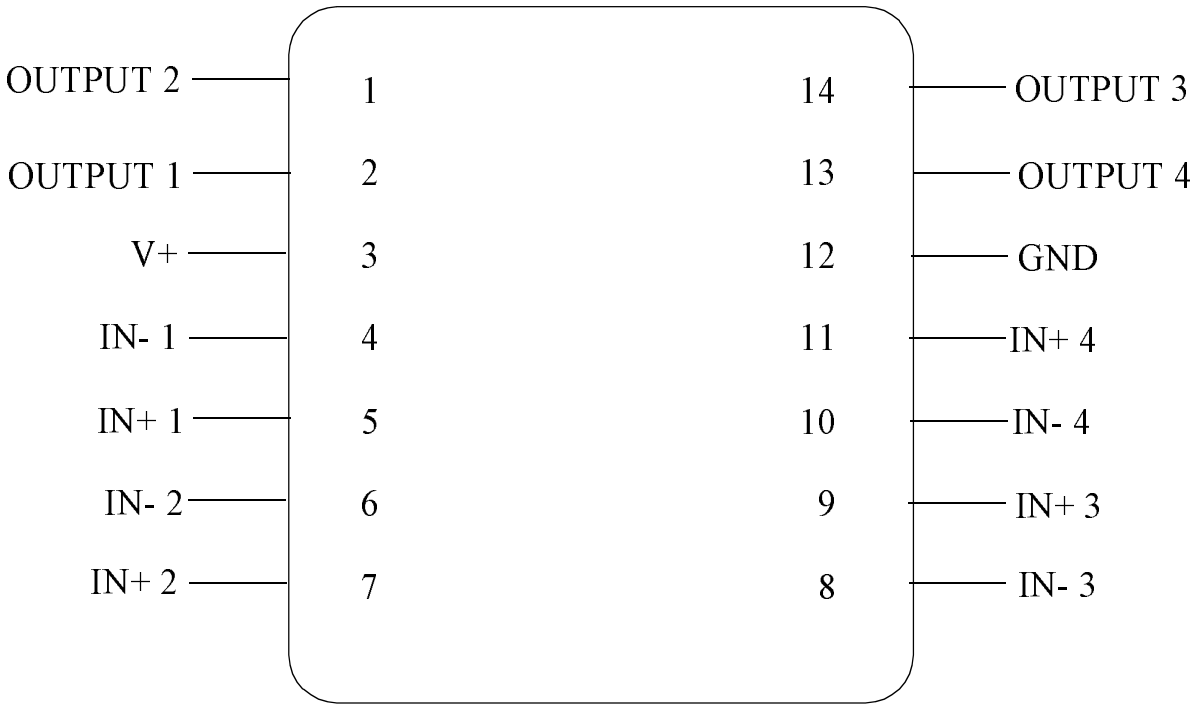
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM139AWG, LM139WG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM

TOP VIEW
P000238A

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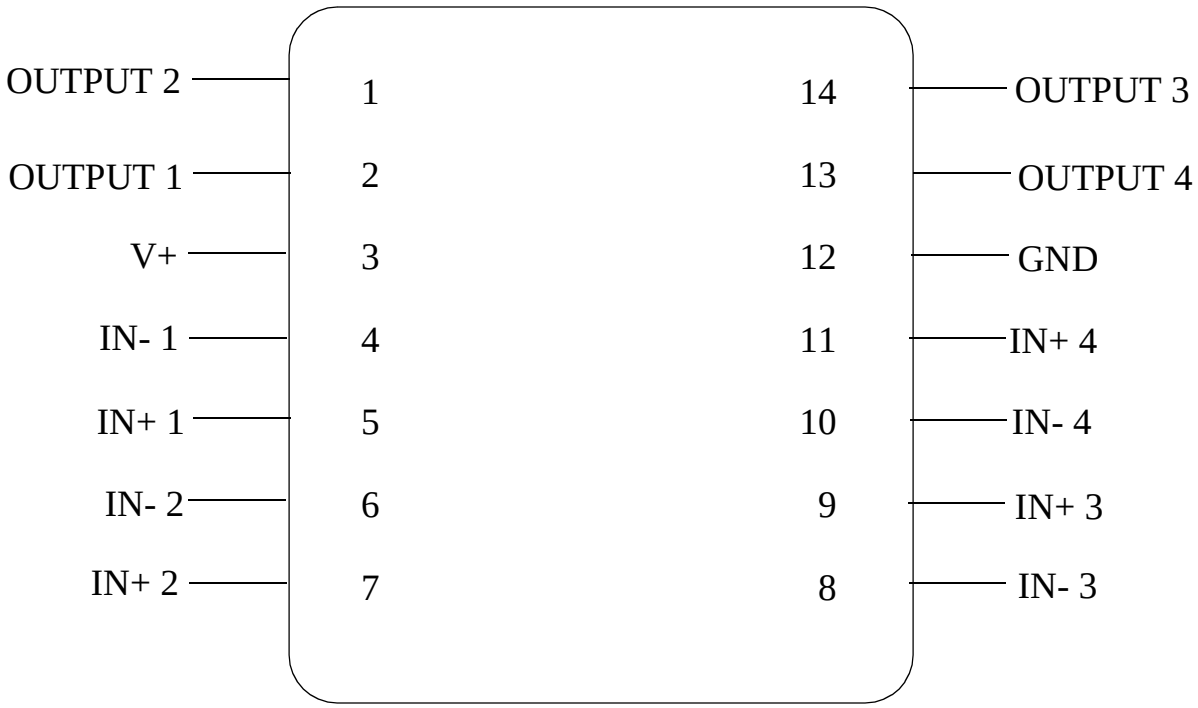
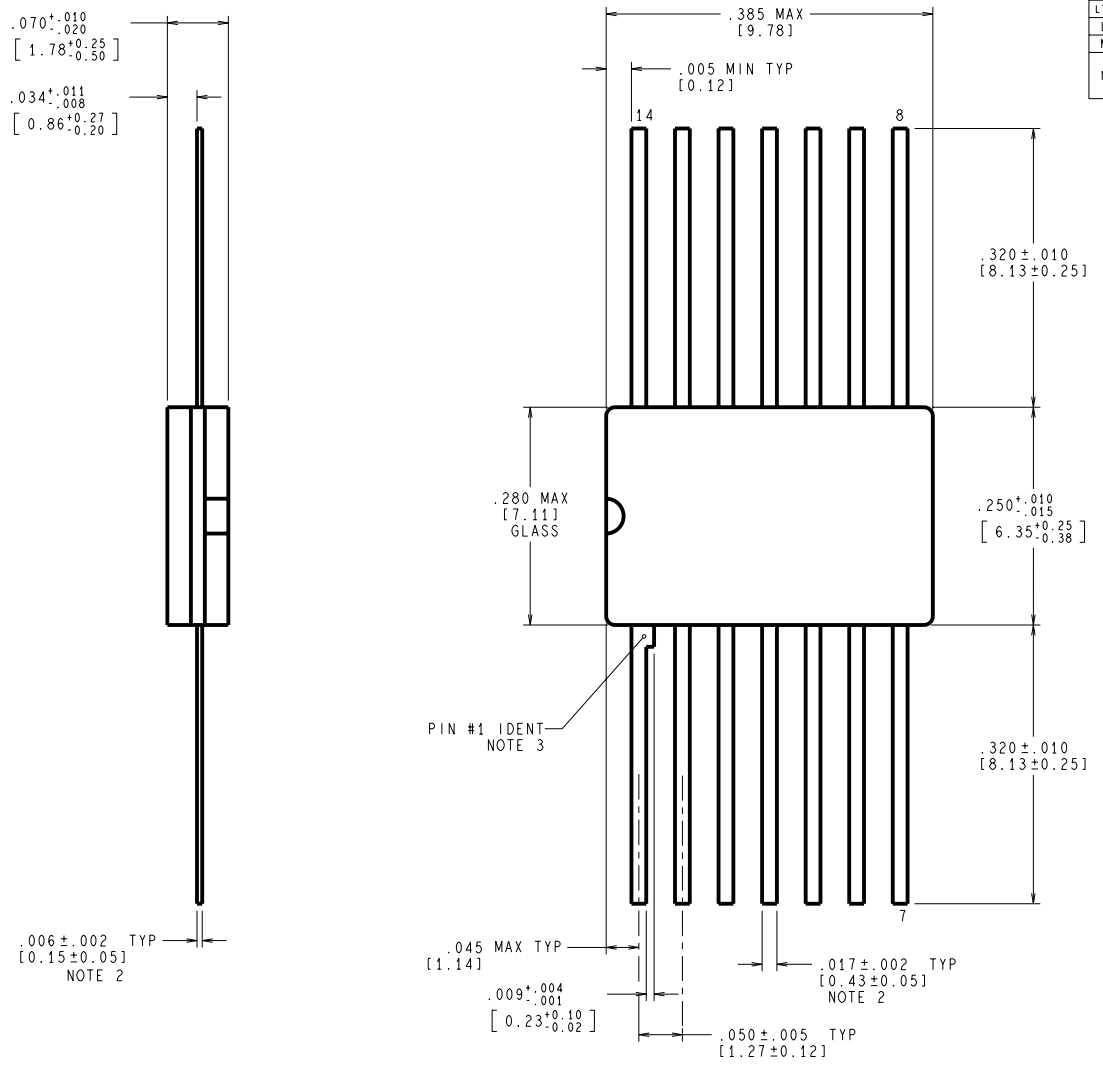
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM139AJ, LM139J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000271A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

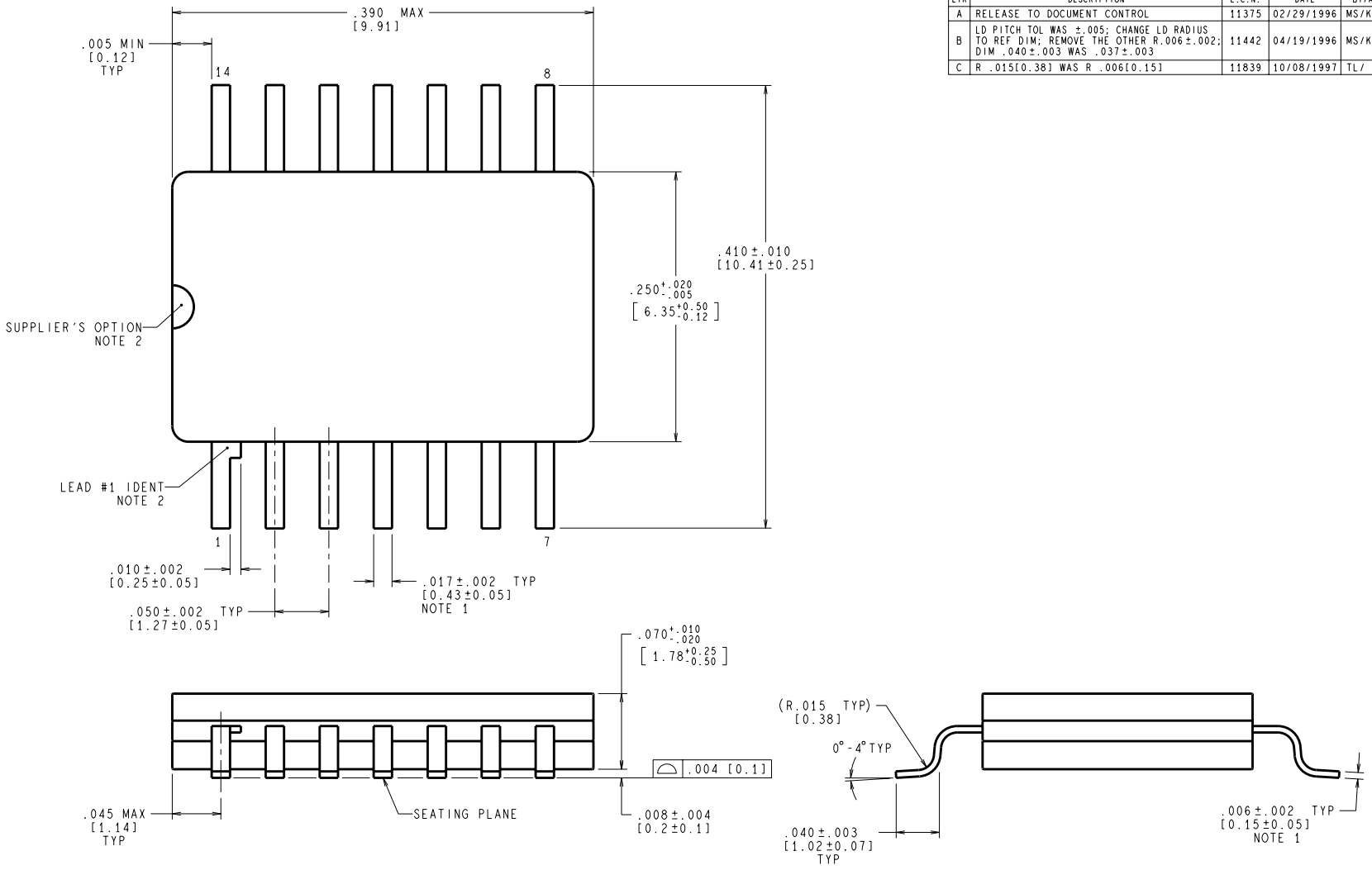
National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11442	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11839	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG14A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0000441	03/27/98	Barbara Lopez	Changed: MDLM139A-X Rev. 0AL to MDLM139A-X Rev. 0A0. Changed NSID to reflect SMD part number.
0B1	M0002749	03/27/98	Barbara Lopez	Update MDS: MDLM39A-X Rev. 0A0 to MDLM139A-X Rev. 0B1. Added WG package. Updated subgroups for Av parameter from: (1, 2 and 3) to (4, 5 and 6), to meet SMD. Added Graphics for Burn-In and Pinout.