

MNDS26F32M-X REV 0B0

Original Creation Date: 08/24/98
Last Update Date: 10/05/98
Last Major Revision Date:

QUAD DIFFERENTIAL LINE RECEIVERS

General Description

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times.

The device features an input sensitivity of 200mV over the input common mode range of $\pm 7.0V$. The DS26F32 provides an enable function common to all four receivers and TRI-STATE outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

Industry Part Number

DS26F32

Prime Die

M632

NS Part Numbers

DS26F32ME/883 *
DS26F32MJ-QMLV****
DS26F32MJ/883 **
DS26F32MW-QMLV*****
DS26F32MW/883 ***

Controlling Document

5962-78020

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Military temperature range
- Input voltage range of $\pm 7.0\text{V}$ (differential or common mode) $\pm 0.2\text{V}$ sensitivity over the input voltage range.
- High input impedance
- Operation from single $+5.0\text{V}$ supply
- Input pull-down resistor prevents output oscillation on unused channels
- TRI-STATE outputs, with choice of complementary enables, for receiving directly on a data bus
- SMD (Standard Military Drawing) 5962-7802005M2A*, MEA**, MFA***, VEA****, VFA*****

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature Range	-65 C to +150 C
Operating Temperature Range	-55 C to +125 C
Lead Temperature Soldering, 60 seconds	300 C
Supply Voltage	7.0V
Common Mode Voltage Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Maximum Power Dissipation (Pd) @ +25C (Note 2)	500mW
Thermal Resistance (JA)	
J package	100 C/W
W package	142 C/W
E package	87 C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Derate J package 10.0mW/C above +25C, Derate W package 7.1mW/C above +25C, Derate E package 11.5mW/C above +25C

Recommended Operating Conditions

Temperature	-55 C to +125 C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_{CC} = 5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _{in}	Input Current	$V_{CC}=4.5V$, $V_{in}=15V$ (Pin under test), other inputs $-15V \leq V_{in} \leq +15V$				2.3	mA	1, 2, 3
		$V_{CC}=5.5V$, $V_{in}=-15V$ (Pin under test), other inputs $-15V \leq V_{in} \leq +15V$				-2.8	mA	1, 2, 3
I _{il}	Logical "0" Enable Current	$V_{CC} = 5.5V$, $V_{en} = .4V$				-360	uA	1, 2, 3
I _{ih}	Logical "1" Enable Current	$V_{CC} = 5.5V$, $V_{in} = 2.7V$				10	uA	1, 2, 3
I _i	Logical "1" Enable Current	$V_{CC} = 5.5V$, $V_{in} = 5.5V$				50	uA	1, 2, 3
V _{ik}	Input Clamp Voltage (Enable)	$V_{CC} = 4.5V$, $I_{in} = -18mA$				-1.5	V	1, 2, 3
V _{oh}	Logical "1" Output Voltage	$V_{CC} = 4.5V$, $I_{oh} = -440uA$, $\Delta V_{in} = 1V$, $\overline{V_{en}} = .8 = V_{en}$			2.5		V	1, 2, 3
V _{ol}	Logical "0" Output Voltage	$V_{CC} = 4.5V$, $\overline{V_{en}} = .8V = V_{en}$, $I_{ol} = 4mA$, $\Delta V_{in} = -1V$				.4	V	1, 2, 3
		$V_{CC} = 4.5V$, $\overline{V_{en}} = .8V = V_{en}$, $I_{ol} = 8mA$, $\Delta V_{in} = -1V$				.45	V	1, 2, 3
I _{cc}	Supply Current	$V_{CC} = 5.5V$, All $V_{in} = Gnd$, $V_{en} = 0V$, $\overline{V_{en}} = 2V$				50	mA	1, 2, 3
I _{oz}	Off-State Output Current	$V_{CC} = 5.5V$, $V_o = .4V$, $V_{en} = .8V$, $\overline{V_{en}} = 2V$				-20	uA	1, 2, 3
		$V_{CC} = 5.5V$, $V_o = 2.4V$, $V_{en} = .8V$, $\overline{V_{en}} = 2V$				20	uA	1, 2, 3
R _{in}	Input Resistance	$-15 \leq V_{cm} \leq 15V$			14		KOhm	1, 2, 3
V _{th}	Differential Input Voltage	$V_{CC} = 4.5V$, $-7V \leq V_{cm} \leq 7V$, $V_{en} = \overline{V_{en}} = 2.5V$, $V_o = 0.45/2.5V$	2		-.2	.2	V	1, 2, 3
		$V_{CC} = 5.5V$, $-7V \leq V_{cm} \leq 7V$, $V_{en} = \overline{V_{en}} = 2.5V$, $V_o = 0.45/2.5V$	2		-.2	.2	V	1, 2, 3
V _{il}	Logical "0" Input Voltage (Enable)	$V_{CC} = 5.5V$	2			.8	V	1, 2, 3
V _{ih}	Logical "1" Input Voltage (Enable)	$V_{CC} = 4.5V$	2		2		V	1, 2, 3
I _{sc (min)}	Output Short Circuit Current	$V_{CC} = 4.5V$, $V_o = 0V$, $\Delta V_{in} = 1V$			-15		mA	1, 2, 3
I _{sc (max)}	Output Short Circuit Current	$V_{CC} = 5.5V$, $V_o = 0V$, $\Delta V_{in} = 1V$				-85	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_{CC} = 5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH		Cl = 50pF	4			23	nS	9
			4			31	nS	10, 11
		Cl = 15pF	3			22	nS	9
			3			30	nS	10, 11
tPHL		Cl = 50pF	4			23	nS	9
			4			31	nS	10, 11
		Cl = 15pF	3			22	nS	9
			3			30	nS	10, 11
tPZH	Enable Time	Cl = 50pF	4			18	nS	9
			4			29	nS	10, 11
		Cl = 15pF	3			16	nS	9
			3			27	nS	10, 11
tPZL	Enable Time	Cl = 50pF	4			20	nS	9
			4			29	nS	10, 11
		Cl = 15pF	3			18	nS	9
			3			27	nS	10, 11
tPHZ	Disable Time	Cl = 50pF	4			55	nS	9
			4			62	nS	10, 11
		Cl = 5pF	3			20	nS	9
			3			27	nS	10, 11
tPLZ	Disable Time	Cl = 50pF	4			30	nS	9
			4			42	nS	10, 11
		Cl = 5pF	3			18	nS	9
			3			30	nS	10, 11

Electrical Characteristics

DC PARAMETERS - DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: NOTE::This section applies to -QMLV devices only and shall be read & recorded at TA = +25C before and after each burn-in and shall not change by more than the limits indicated. The delta rejects shall be included in the PDA calculation.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Voh	Logical "1" Output Voltage	Vcc = 4.5V, Ioh = -440uA, Delta Vin = 1V, Ven = 0.8V = Ven			-250	250	mV	1
Vol	Logical "0" Output Voltage	Vcc = 4.5V, Iol = 4mA, Delta Vin = -1V, Ven = 0.8V = Ven			-45	45	mV	1
		Vcc = 4.5V, Iol = 8mA, Delta Vin = -1V, Ven = 0.8V = Ven			-45	45	mV	1
Iin	Input Current	Vcc = 4.5V, Vin=15V (Pin under test), other inputs -15V <= Vin <= +15V			-0.28	0.28	mA	1
		Vcc = 5.5V, Vin=-15V (Pin under test), other inputs -15V <= Vin <= +15V			-0.28	0.28	mA	1

Note 1: Power dissipation must be externally controlled at elevated temperatures.

Note 2: Parameter tested go-no-go only.

Note 3: Tested at 50pF guarantees limit at 15 & 5pF.

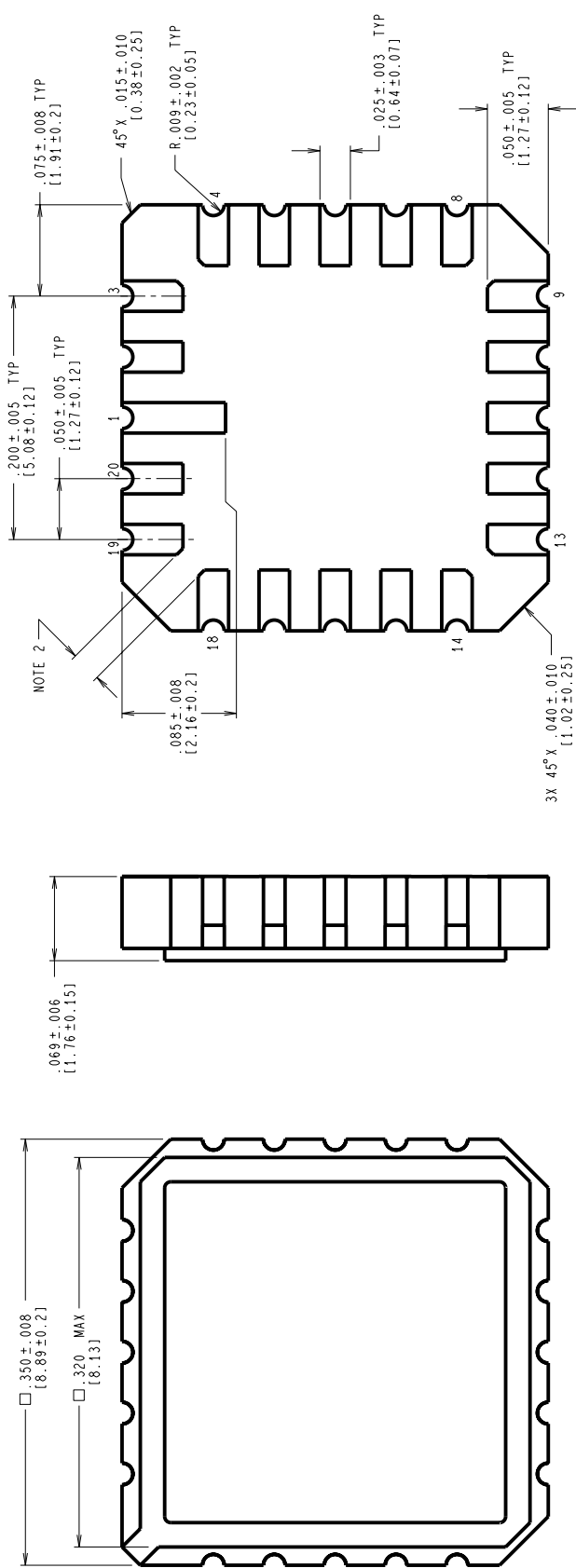
Note 4: Tested at 50pF, system capacitance exceeds 5 to 15pF.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL (P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

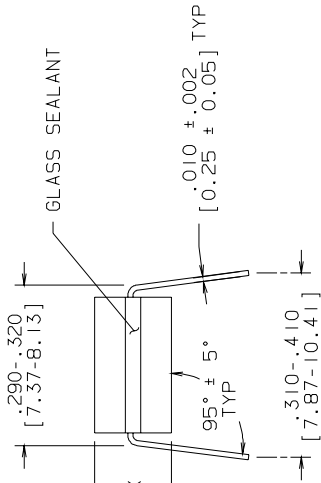
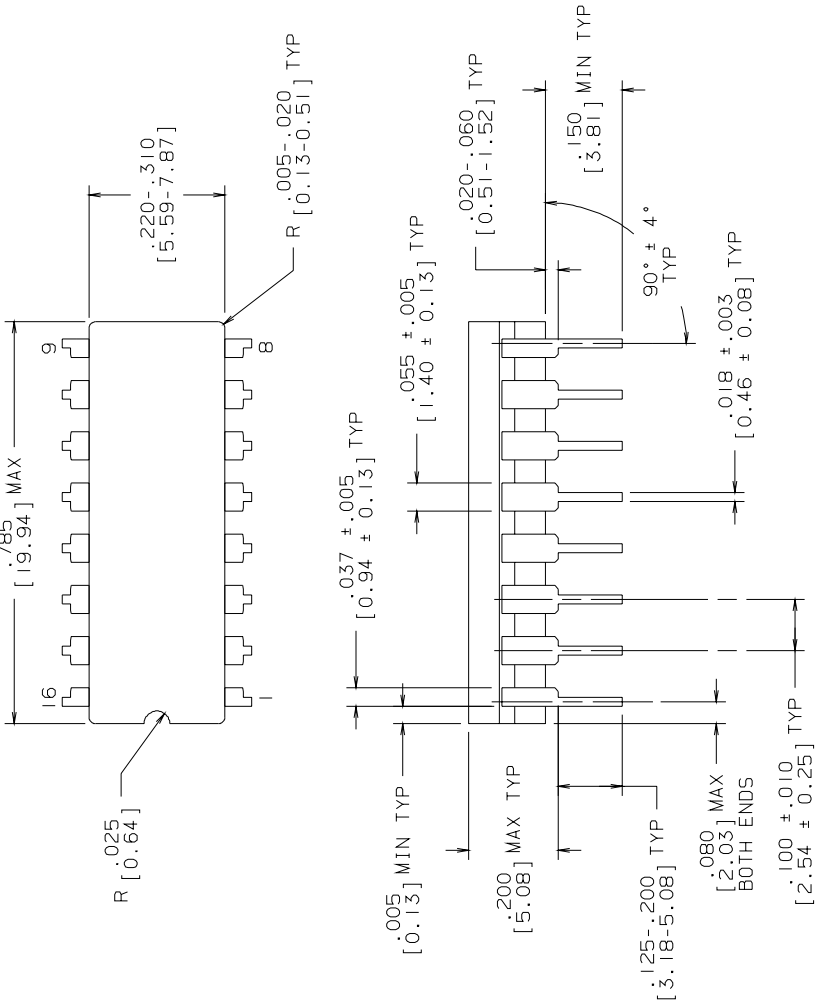
1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

- 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
- SOLDER DIP.
SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
- CORNER PADS MAY HAVE A 45° X $.020$ IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE $.015$ IN/0.38mm DIMENSION.
- REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO CONFIGURATION CONTROL

APPROVALS		DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DESIGN	Design Grady	02/10/94	2000 Semiconductor Drive, Santa Clara, CA 95052-8000	
ESTG. CHK.			LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL	
ENGR. CHK.				
APPROVAL				
PROJECTION			SCALE	SIZE
			N/A	C
			DO NOT SCALE	DRAWING
			REV	REV
			MKT-E20A	E
			SHEET 1 of 1	

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93
			TL/



MIL/AERO

CONFIGURATION CONTROL

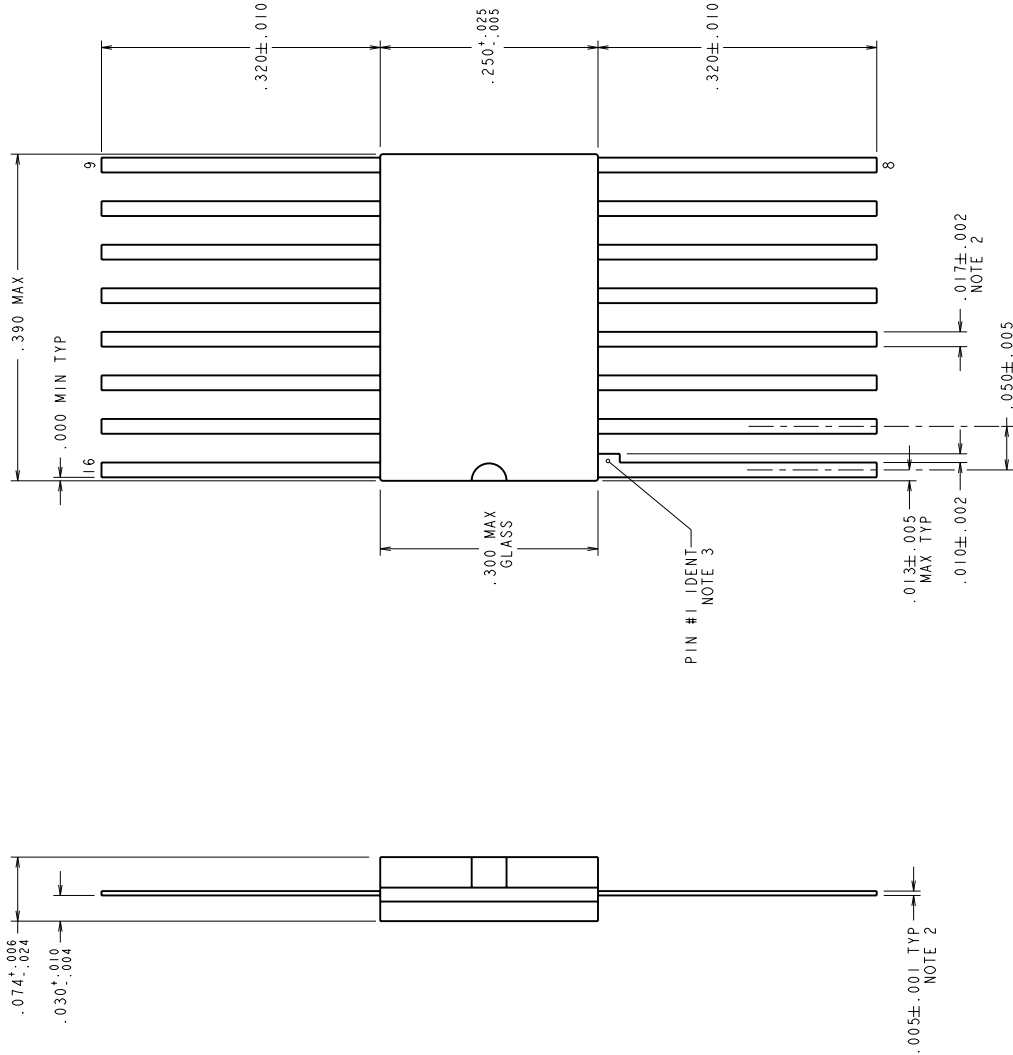
MIL-M-38510

CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH			
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DRAWN LEQUANG	09/15/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
DFTG. CHK.		CERDIP (J) , 16 LEAD	
ENGR. CHK.			
APPROVAL			
 PROJECTION INCH [MM]	SCALE	SIZE	DRAWING NUMBER
	N/A	B	MKT-J16A
DO NOT SCALE DRAWING		SHEET	OF
		I	I

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
 - JEDEC REGISTRATION M0-036, VARIATION AD, DATED 04/1981.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94
L	.017±.002 WAS .017±.020.	10656	10/21/94
			DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
 - a) A NOTCH OR OTHER MARK WITHIN THIS AREA
 - b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS		DATE	
DRN	<i>D.F. Grady</i>	07/28/94	
DFTG. CHK.			
ENGR. CHK.			
PROJECTION			
			
SCALE	N/A	SIZE	C
DRAWING NUMBER		MKT-WI6A	
REV	L		
DO NOT SCALE DRAWING		SHEET 1 of 1	



National Semiconductor

2900 Semiconductor dr., Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

National Semiconductor
2000 Semiconductor dr., Santa Clara, CA 95052-8090

CERPACK, I6 LEAD

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0003015	10/05/98	Linda Collins	Added J-QMLV and W-QMLV and removed DS26F32MJ-MLS and DS26F32MW-MLS NSPN's. Added thermal resistance ratings. Added Drift Values section specific for the QMLV parts.