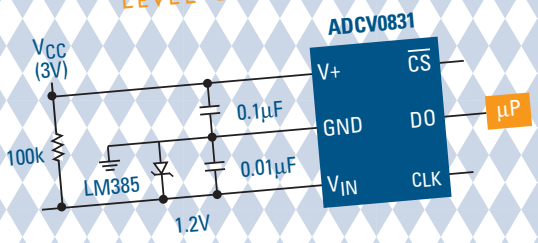
ADCV0831 Qualification Package

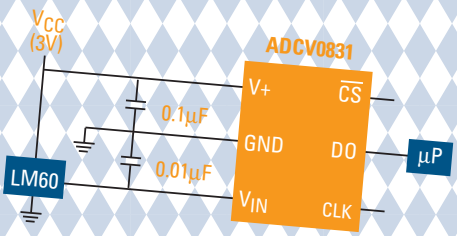
ADCV0831

WORLD'S SMALLEST 3V 8-BIT A/D CONVERTER IN THE SOT23-6 PACKAGE.

POWER SUPPLY LEVEL DETECTION



LOW-COST REMOTE TEMPERATURE SENSOR



National Semiconductor

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ADCV0831
QUALIFICATION PACKAGE

Fall 1998

Table of Contents

1.0 INTRODUCTION

1.1 General Product Description

This qualification packet covers the ADCV0831, low voltage, 8-bit A/D converter with serial I/O. It features 3V operation and auto shutdown and its operation is guaranteed at junction temperatures ranging from 0°C to 70°C. This device is offered in the tiny SOT23-6 package.

1.2 Reliability/Qualification Overview

The ADCV0831 successfully completed all reliability testing per qual plan Q19970916 for qualification as a new device in the SOT23-6 package. This part also passed 3000V of ESD Human Body Model and 200V of Machine Model.

1.3 Technical Assistance

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2.0 DEVICE INFORMATION

2.1 Datasheet

National Semiconductor

August 1998

ADCV0831
8 Bit Serial I/O Low Voltage Low Power ADC with Auto Shutdown in a SOT Package

General Description

The ADCV0831 is a low voltage 8-bit successive approximation A/D converter with serial I/O. The I/O is a 3-wire serial interface compatible with NSC's MICROWIRE ™ & Motorola's SPI standards. It easily interfaces with standard shift registers or microprocessors.

Low voltage and auto shutdown features make the ADCV0831 ideal for portable battery operated electronic devices. The main benefits are most apparent in small portable electronic devices. The tiny A/D converter can be placed anywhere on the board.

Applications

- Digitizing automotive sensors
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Test systems
- Embedded diagnostics

Features

- Tiny 6-pin SOT 23 package
- Serial digital data link requires few I/O pins
- Auto Shutdown
- 0V to 3V analog input range with single 3V power supply
- TTL/CMOS input/output compatible

Key Specifications

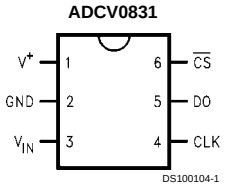
(For 3V supply, typical, unless otherwise noted.)

- Resolution: 8 bits
- Conversion time (f_C = 700 kHz): 16µs
- Low power dissipation: 720µW
- Single supply: 2.7V to $5V_{DC}$
- Linearity error: ±1.5LSB over temperature
- No missing codes over temperature
- Shutdown supply current 10nA

Ordering Information

Temperature Range ($0^\circ C \le T_j \le +70^\circ C$)	Package	Supplied As
ADCV0831M6X	MA06A	3k Units Tape and Reel
ADCV0831M6	MA06A	250 Units Tape and Reel

Connection Diagram



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Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	5.5V
Voltage at Inputs and Outputs	−0.3V to V_{CC} + 0.3V
Input Current at Any Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Power Dissipation at T_A = 25˚C (Note 5)	470 mW
ESD Susceptibility (Note 6)	2000V
Soldering Temperature (Note 7)	
Convection Infrared (15 sec.)	215˚C
Wave Soldering (4 sec.) (Note 7)	260˚C
Storage Temperature	−65˚C to +150˚C
Thermal Resistance (θ_{JA})	265˚C/W

Operating Ratings (Notes 2, 3)

Temperature Range	0˚C≤ T_j ≤70˚C
Supply Voltage (V_{CC})	2.7V_{DC} to 5V

Electrical Characteristics

The following specifications apply for V_{CC} = 3V_{DC}, and f_{CLK} = 500 kHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25˚C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units
	Integral Linearity Error		±0.6	**±1.5**	LSB (max)
	Offset Error		±0.1	**±1.5**	LSB (max)
	Full Scale Error		±0.3	**±1.5**	LSB (max)
	Resolution			**8**	Bits (min)
V_{IN}	Analog Input Voltage			**(V_{CC} + 0.05)** **(GND − 0.05)**	V (max) V (min)
$V_{IN(1)}$	Logical “1” Input Voltage	V_{CC} = 3V		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	V_{CC} = 3V		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	V_{IN} = 3V	0.01	**1**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	V_{IN} = 0V	0.01	**−1**	µA (max)
$V_{OUT(1)}$	Logical “1” Output Voltage	I_{out} =-360µA	2.8	**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	I_{out} =1.6 mA	0.24	**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	V_{OUT} = 0V	0.01	**3.0**	µA (max)
I_{SOURCE}	Output Source Current	V_{OUT} = 0V	2.6	**1.0**	mA (min)
I_{SINK}	Output Sink Current	V_{OUT} = 3V	7.4	**3.0**	mA (min)
I_{CC}	Supply Current	$\overline{CS}$ = HIGH	0.01	30	µA (max)
		$\overline{CS}$ = LOW	200	**400**	µA (max)

AC Electrical Characteristics

The following specifications apply for V_{CC} = +3 V_{DC}, and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25˚C.

Symbol	Parameter		Conditions	Typical (Note 8)	Limits (Note 9)	Units
f_{CLK}	Clock Frequency			10	**700**	kHz (max) kHz (min)
t_{SET-UP}	$\overline{CS}$ failing edge to CLK rising edge			25		ns
	Clock Duty Cycle				**40** **60**	% (min) % (max)
T_C	Conversion Time				**11**	Clock Periods
t_{pd}	CLK Falling Edge to Data Valid	Low to High	C_L = 100 pF	142	250	ns (max)
		High to Low		70	200	
t_{1H}, t_{0H}	$\overline{CS}$ Rising Edge to Data Output TRI-STATE		C_L = 100 pF, R_L =2 kΩ	75	250	ns (max)
	(see TRI-STATE Test Circuits)		C_L = 100 pF, R_L = 10 kΩ	50		

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = +3 V_{DC}, and $t_r = t_f$ = 20 ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units
C_{IN}	Capacitance of Logic Inputs		5		pF
C_{OUT}	Capacitance of Logic Outputs		5		pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND = 0 V_{DC}, unless otherwise specified.

Note 4: When the input voltage V_{IN} at any pin exceeds the power supplies (V_{IN} <GND or V_{IN} > V_{CC}) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four pins.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 6: Human body model, 100 pF capacitor discharged through a 1.5 kΩ resistor.

Note 7: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or Linear Data Book section "Surface Mount" for other methods of soldering surface mount devices.

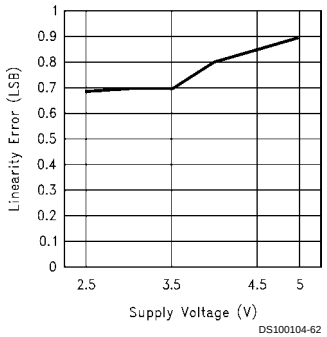
Note 8: Typicals are at T_J = 25°C and represent the most likely parametric norm.

Note 9: Guaranteed to National's AOQL (Average Outgoing Quality Level).

Typical Performance Characteristics

The following specifications apply for V_{CC} = 3V, unless otherwise specified

Integral Linearity Error vs Supply Voltage



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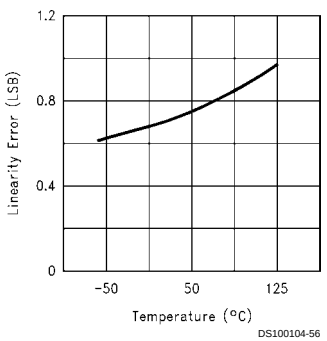
Linearity Error vs Temperature



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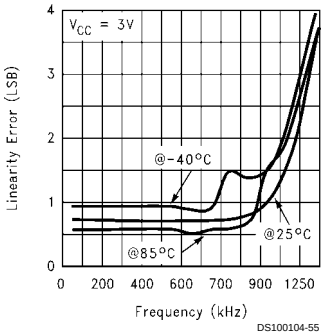
Linearity Error vs Clock Frequency



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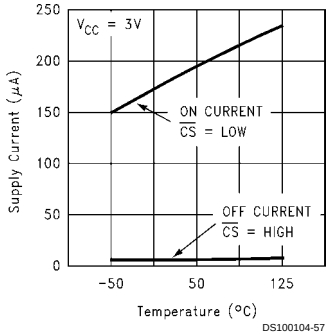
Power Supply Current vs Temperature



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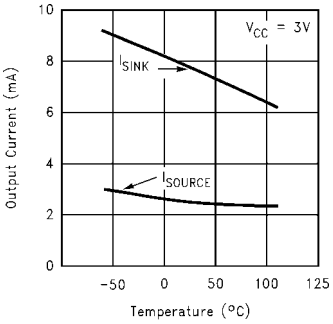
Output Current vs Temperature



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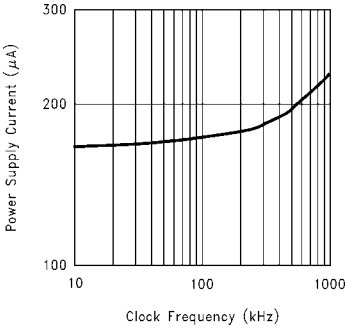
Power Supply Current vs Clock Frequency



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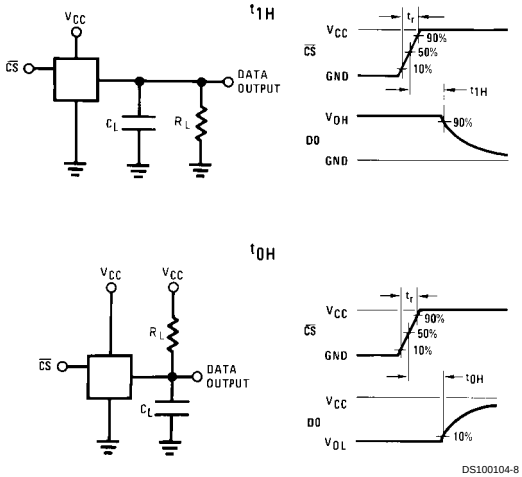
TRI-STATE Test Circuits and Waveforms



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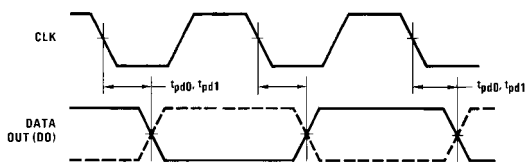
Timing Diagrams

Data Output Timing



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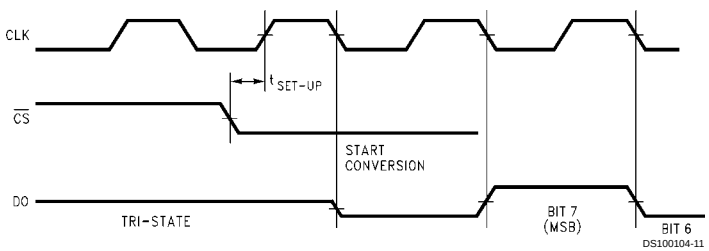
Start Conversion Timing



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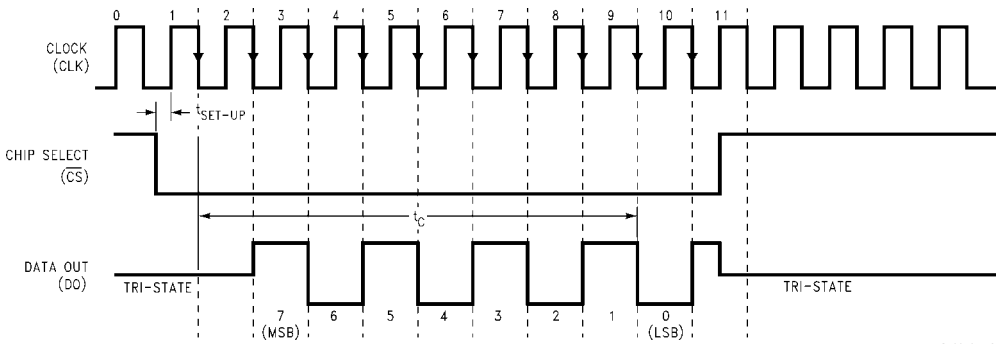
Timing Diagrams (Continued)

Timing



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Functional Description

The design of this converter utilizes a comparator structure with built-in sample-and-hold which provides for V_{IN} to be converted by a successive approximation routine.

The analog input voltage can range from 50mV below ground to 50mV above V_{CC} without degrading conversion accuracy.

The ADCV0831 is intended to work with a CPU which strobes data on the clock's rising edge. The ADCV0831 strobes data on the clock's falling edge so that the data output is stable when the CPU reads it in.

When the Chip Select pin is high, the output is TRI-STATE and the ADCV0831 is in shutdown mode and draws less than 30 µA of current. During shutdown the digital logic draws no current at CMOS logic levels, and the analog circuitry is turned off. When the Chip Select pin goes low, all the analog circuitry turns on, and the conversion process begins.

1.0 THE DIGITAL INTERFACE

The most important characteristic of this converter is the serial data link with the controlling processor. Using a serial communication format offers three very significant system improvements. It allows many functions to be included in a small package, it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor, and can transmit highly noise immune digital data back to the host processor.

To understand the operation of this converter it is best to refer to the Timing Diagrams and to follow a complete conversion sequence.

1. A conversion is initiated by pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion.
2. During the conversion the output of the SAR comparator indicates whether the analog input is greater than (high) or less than (low) a series of successive voltages in a resistor ladder (last 8 bits). After each comparison the comparator's output is shifted to the DO line on the falling edge of CLK. This data is the result of the conversion being shifted out (with the MSB first) and can be read by the processor immediately.
3. After 11 clock periods the conversion is completed.
4. All internal registers are cleared when the $\overline{CS}$ line is high. See Data Input Timing under Timing Diagrams. If another conversion is desired $\overline{CS}$ must make a high to low transition.

2.0 REFERENCE CONSIDERATIONS

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is the system power supply. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

Since there is no separate reference and analog supply pins, the analog side is very sensitive. The PC layout of the ADCV0831 is very critical. The ADCV0831 should be used with an analog ground plane and single-point grounding techniques. The Gnd pin should be tied directly to the ground plane. One supply bypass capacitor (0.1 µF) is recommended to decouple all the digital signals on the supplies. The lead length of the capacitor should be as short as possible.

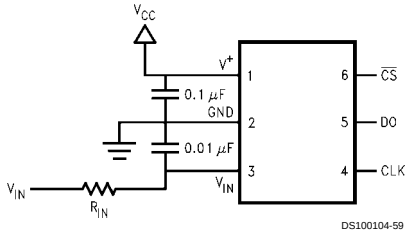
3.0 THE ANALOG INPUT

The most important feature of this converter is that it can be located right at the analog signal source through just a few wires. It can communicate with a processor with a highly noise immune serial bit stream. This greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The input has a sample and hold, therefore a capacitor (0.01 µF) is needed at the input pin in order to swamp out any feedthrough signal coming from the sample and hold circuitry.

The input capacitor lead length is not as critical as the supply decoupling capacitor, as long as the capacitor is large enough to swamp out any sample and hold feedthrough.

Source resistance limitation is important with regard to the DC leakage currents of the input multiplexer. Bypass capacitors should not be used if the source resistance is greater than 1kΩ. The worst-case leakage current of ±1µA over temperature will create a 1mV input error with a 1kΩ source resistance. An op-amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

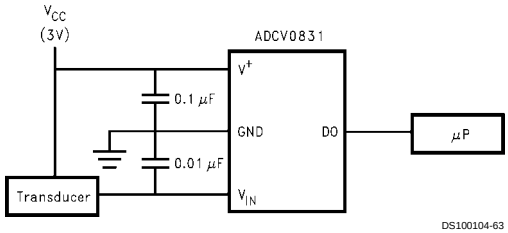


Recommended Power Supply Bypassing

Applications

The ADCV0831 is ideal for applications operating with ratiometric transducers. The ADCV0831 can measure the signal produced by the transducer and produce a corresponding code to the microprocessor. The microprocessor can then control the system producing the signal.

Operating with Ratiometric Transducers



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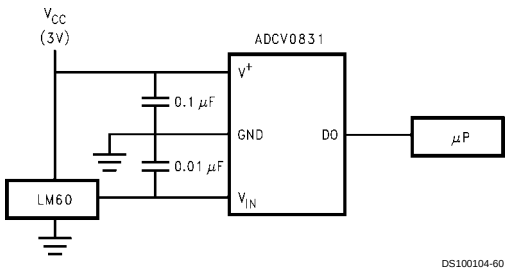
The ADCV0831 can be used in low-cost remote temperature sensor system. For a temperature sensor, the LM60 is an excellent companion to the ADCV0831, since it can operate off 3V supply. The LM60 linear scale factor is 6.25mV/˚C. Therefore, the ADCV0831 can digitize a couple of degrees change in temperature and provide the output to the microprocessor, which in turn can adjust the system environment. For higher accuracy, a low-offset op-amp can be used to gain up the LM60 output.

Low-Cost Remote Temperature Sensor



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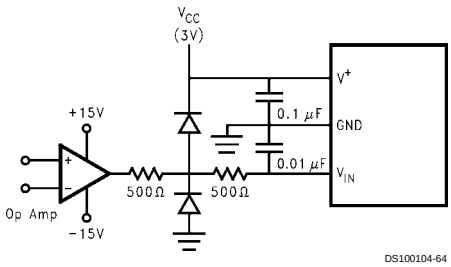
Applications (Continued)

When the input of the ADCV0831 is driven by an op-amp operating at a supply voltage greater than 5V, it is a good idea to protect the input of the ADCV0831 from exceeding the supply voltage. Two diodes can be added to the input one to supply and one to the ground pin.

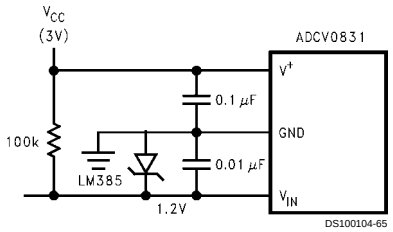
Protecting the input



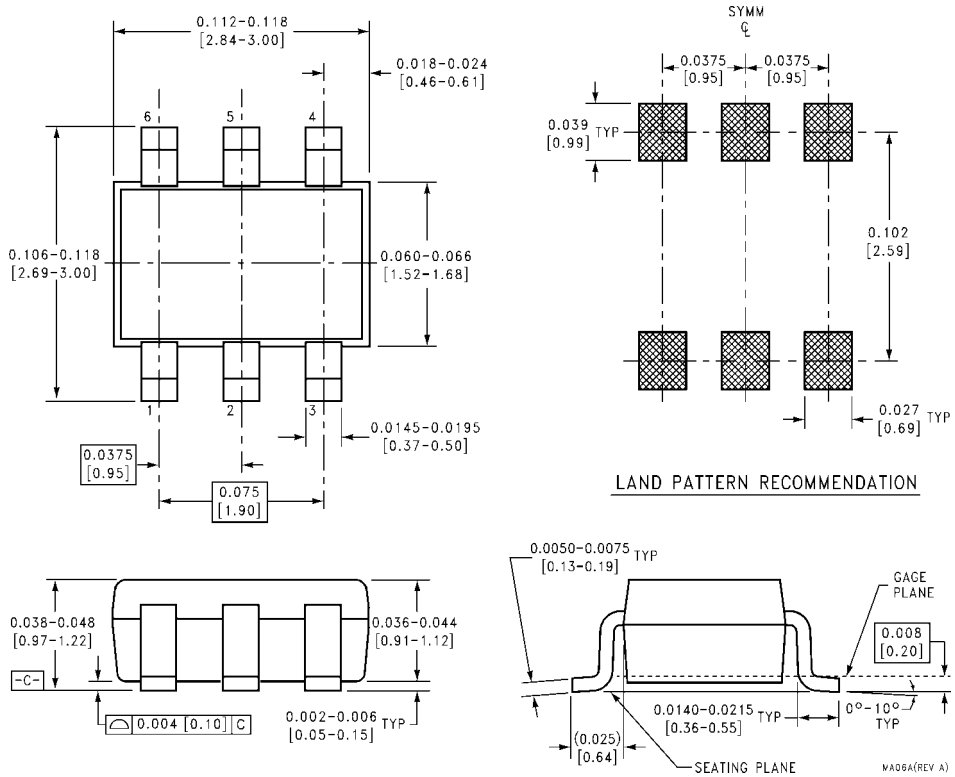
Note: Diodes are IN914

This circuit utilizes the LM385 reference to detect the power supply voltage level. When the supply voltage is 3V, the LSB = 3/256 = 11.7mV. Since the LM385 reference sets the input to 1.2V. The output code is 102. As the supply voltage decreases, the LSB decreases and the output code increases. When the supply voltage reaches 2.7V, the LSB = 10.5 mV. The input voltage is still at 1.2V, and the output code is 114. If the supply voltage increases, the LSB increases and the output code decreases. When the supply voltage reaches 3.3V, the LSB = 12.9mV and the output code is 93.

Power Supply Level Detection



Physical Dimensions inches (millimeters) unless otherwise noted



Order Number ADCV0831M6X, ADCV0831M6
NS Package Number MA06A

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Fax: 81-3-5620-6179

3.0 PROCESS INFORMATION

3.1 Process Details

Fabrication Site: South Portland, Maine
Process Technology: CS80cbi
Wafer Diameter: 6 inches
Number of Masks: 16
Metallization: Al
Passivation: PECVD Oxide/Nitride

Number	Name	Mask	FM_GDS
40	NBURIED	0.8	21
57	PBX	0.9	28
1	NWELL	1.0	1
2	COMP	2.0	2
3	PFIELD	3.0	3
30	NCAPSINK	3.5	20
4	POLY	4.0	4
16	PLDD	4.3	16
15	NLDD	4.5	15
5	NPLUS	5.0	5
6	PPLUS	6.0	6
7	CONT	7.1	7
8	MET1	8.0	8
9	VIA1	9.0	9
10	MET2	10.0	10
13	PS01	13.0	13

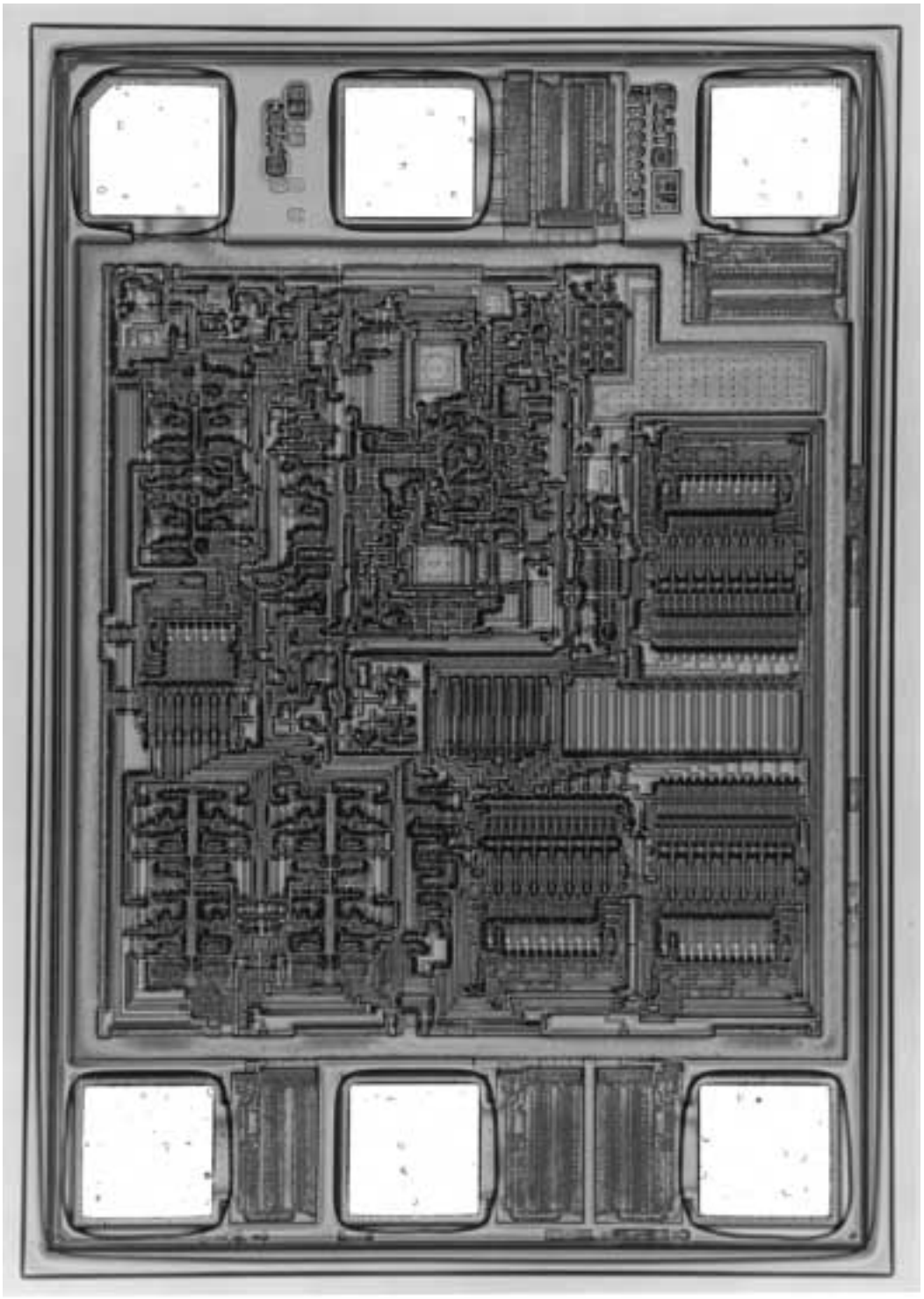
1. Initial Ox
2. Trench Define & Etch
3. N-Iso Def & Imp
4. N-Iso Drive
5. N-Iso Ox Strip & Screen Ox
6. N+ BL Def & Imp
7. P+ BL Def & Imp
8. N/P BL Anneal
9. Epi
10. Comp Pad & Cmp Nit
11. N-Well
12. Selective Ox
13. N-Well Nitride Strip
14. P-Well Implant
15. Selective Ox Etch
16. N-Well P-Well Dr-Ox
17. Drive-In Ox Strip
18. Comp Pad/Nit/Define
19. Comp Mask Etch
20. P-Field Define/Implant
21. Iso Ox
22. Active Nitride Strip
23. Pad Remove, Sac, Vt Adj
24. Sink Define/Imp
25. Sac Strip, Gate/Poly Dep
26. Poly Dope, Poly Anneal
27. Poly Etch
28. Poly Seal Ox
29. P-LDD Mask & Imp
30. N-LDD Mask & Imp
31. Spacer Ox Dep/Etch
32. N+S/D Def & Imp
33. Base Def/Etch/Imp
34. N+ Drive
35. P+ S/D Def & Imp
36. D1 & P+ Anneal
37. D1 SOG & Cap TEOS
38. Window TEOS Dep
39. Contact Def & Etch
40. Cont Liner/Dep/Etch
41. Metal 1 Dep/Def/Etch
42. Metal 1 Alloy & ET
43. D2
44. Via Def & Etch
45. Via Liner-M2 Etch
46. Passivation

4.0 PACKAGING INFORMATION

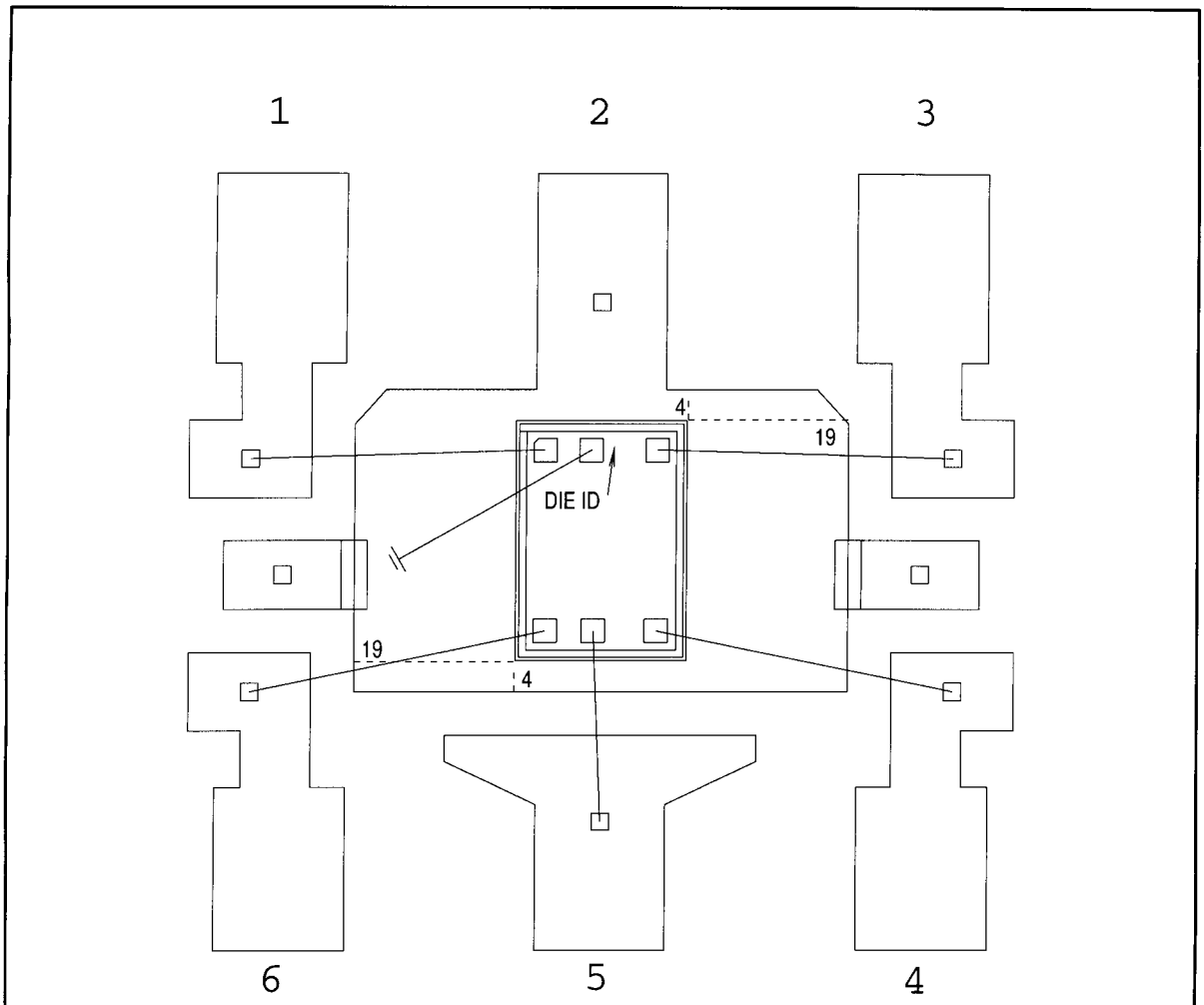
4.1 Package Material

Generic Package Type	**6 Lead SOT-23**
NS Package Number	MA06A
Package Material Type	Molded Plastic
Mold Compound Manufacturer's Designation	Sumitomo EME6710
Lead Frame Material	Copper
Lead Frame Manufacturer	QPL
External Lead Frame Coating	Sn/Pb Solder Plate
Die Attached Method	Preform (Eutectic)
Bond Wire	Gold, 1.5mils
Bond Type	Thermosonic Ball
Package Thermal	325°C/W

4.2 Die Photo

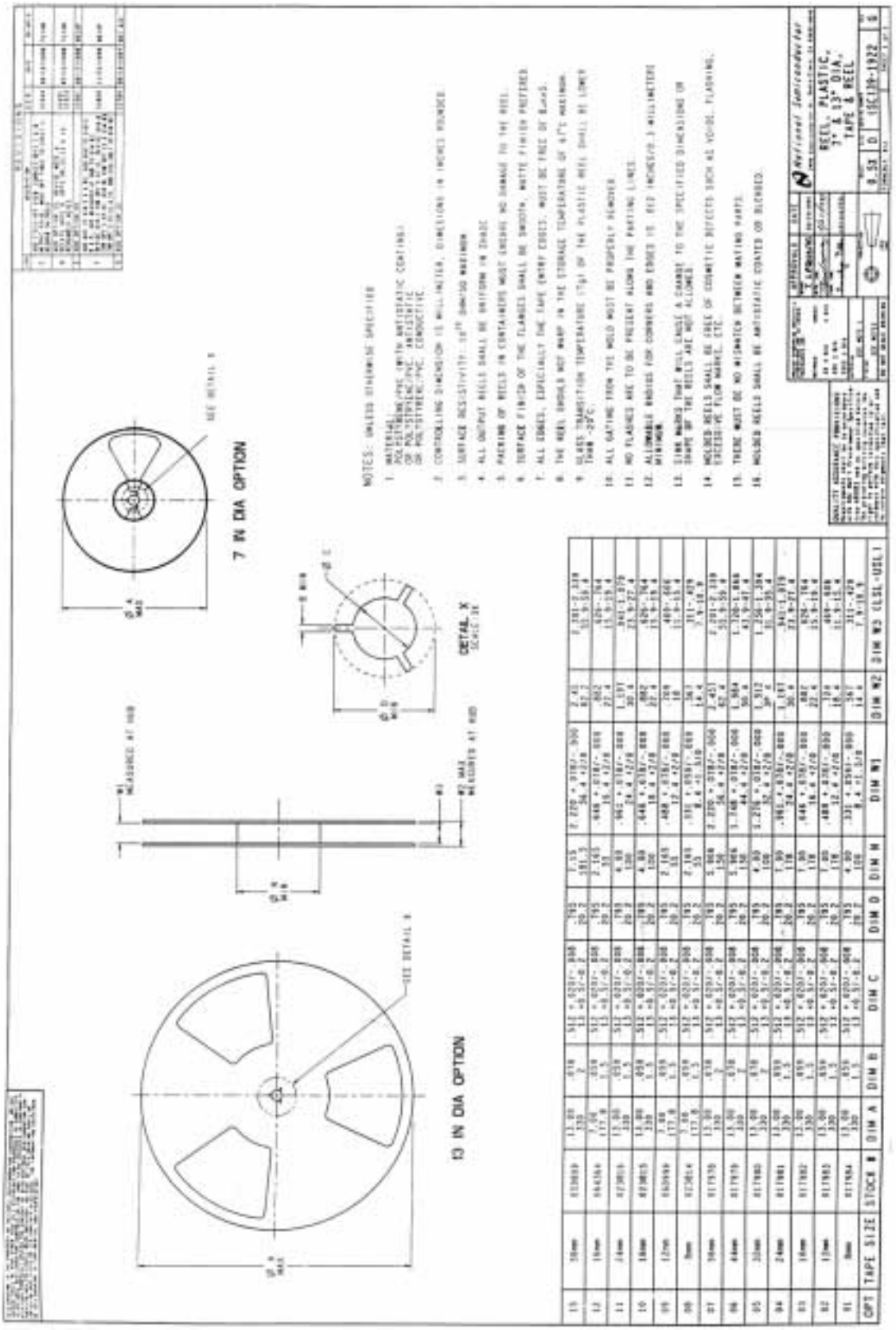


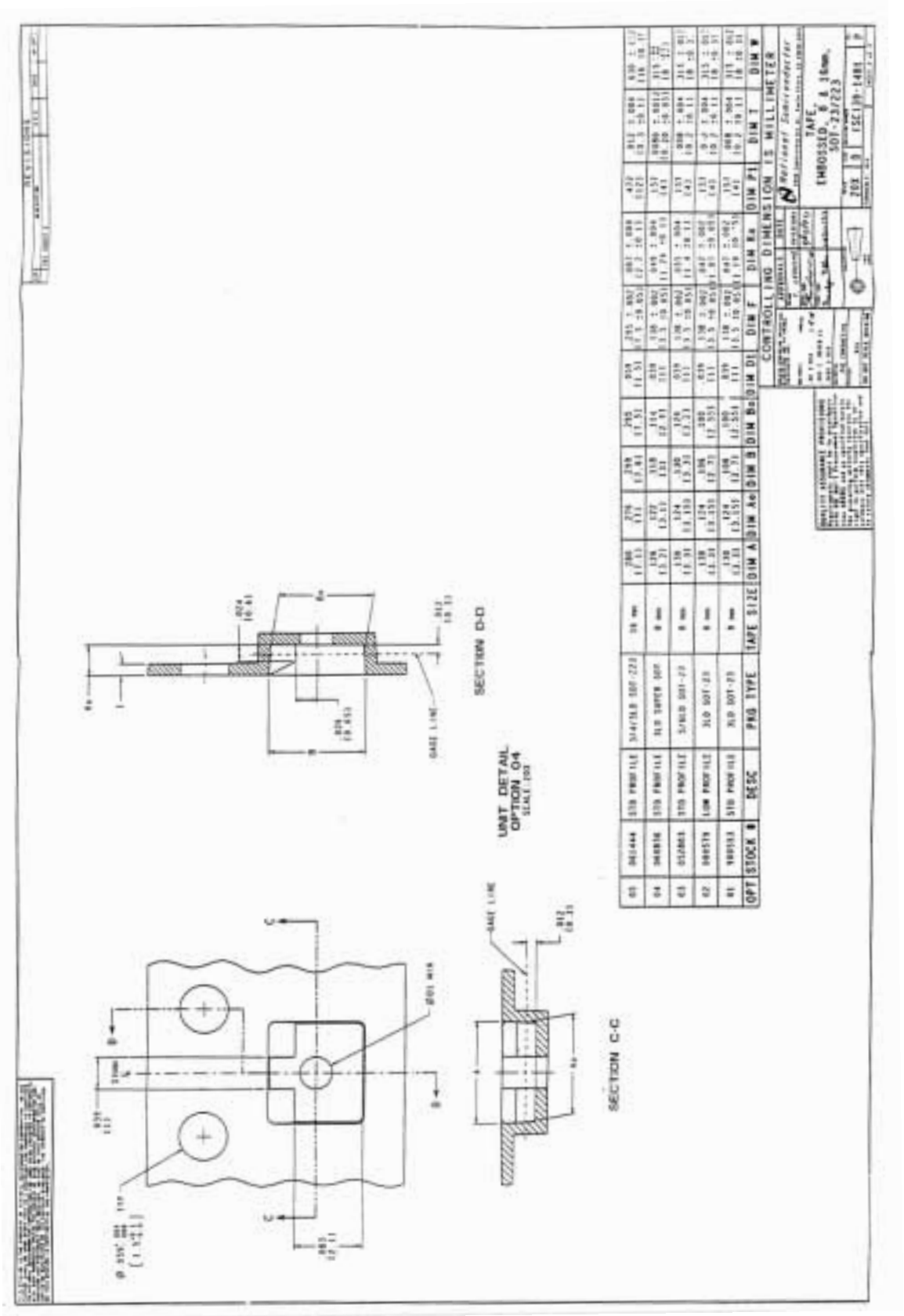
4.3 Bonding Diagram



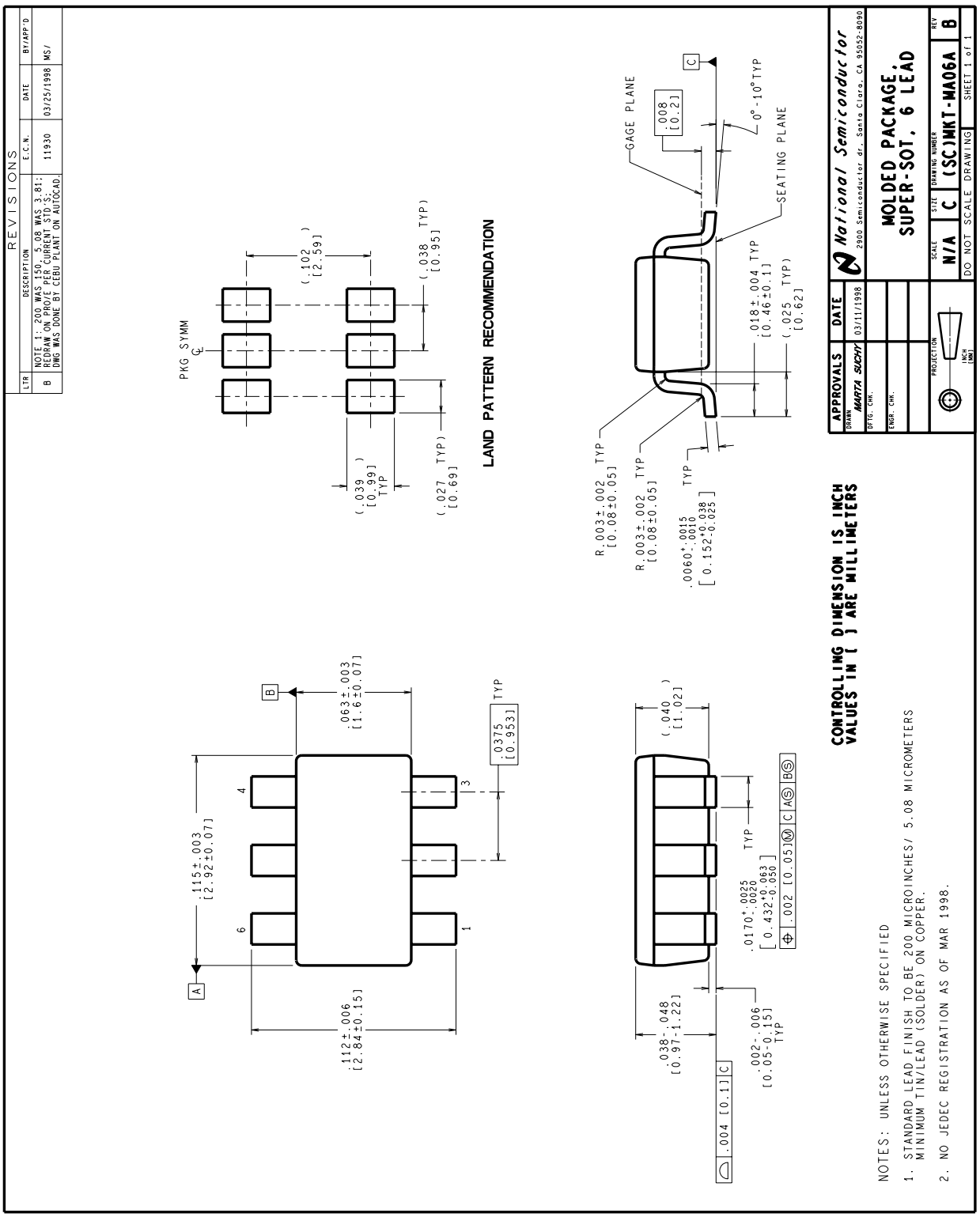
□FRAME DWG: 36-0852-01 SK: 062412 PAD: .057 X .035	AD- MA006ACB MB REV: B PKG: MA DIE ID: ADCV0831BZ STEP/REV: B	Metalization:	BOND-CODE:
		0.5% CU, DLM	
□DIE ATTACH SK: N/A TYPE: N/A	DIE SIZE(* CALCULATED) (MIL): 20 X 28 (MIC): 503 X 706 *	MBS NOTE	THERE ARE 3 BOND LOCATIONS FOR P IN 2, EBS ONLY ALLOWS FOR 1 BOND LOCATION. THIS MAY RESULT IN A DRC ERROR.
□WIRE SK: 022628 TYPE: AU DIA = .001 # WIRES: 6	DIE PLACEMENT X= 19 Y= 4 ANGLE= 0.0		
□MOLD COMPOUND SK: 058072 TYPE: B18	□ADHESIVE SK: N/A □HEAT SINK SK: N/A □CHIP CAPS SK: N/A QTY: N/A DWG: N/A		
	NOTE: EUTECTIC DIE ATTACH PHYSICAL DIE ID: ADCV0831B	04/21/98 05/06/98	CLLHEM CFWSSC
MIN. PAD PITCH: 5.29 MILS	ASS'Y : ADCV0831M6 DASH- 02 REV: A PDCN: BHQ723		

4.4 Tape & Reel Dimensions





4.5 Package Dimensions



5.0 RELIABILITY DATA

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Nick Stanco
Corporate Reliability
Tel 408.721.3073
Fax 408.721.7449

National Semiconductor Reliability Data

(ADCV0831 Serial I/O A/D Converter)

RESULTS

		Rejects per Lot Sample Size		
Tests	**Time/Cycles**	**Lot 1 (REV A1)**	**Lot 2 (REV A1)**	**Lot 3 (REV B1)**
SOPL-IB1	168 hours	0/77	0/77	0/77
	500 hours	0/77	0/77	0/77
	1000 hours	0/77	0/77	0/77
THBT-IB1	168 hours	0/77		
	500 hours	0/77		
	1000 hours	0/77		
ACLV-IB1	168 hours	0/77		
TMCL-IB1	500 cycles	0/77		
	1000 cycles	0/77		

	8L MDIP PACKAGE		6L SOT-23 PACKAGE	
HBM ESD (REV B1)				
	500 volts	0/5	500 volts	0/5
	1000 volts	0/5	1000 volts	0/5
	1500 volts	0/5	1500 volts	0/5
	2000 volts	0/5	2000 volts	0/5
	2500 volts	0/5	2500 volts	0/5
	3000 volts	0/5		
MM ESD (REV B1)	50 volts	0/5		
	100 volts	0/5		
	150 volts	0/5		
	200 volts	0/5		

TEST DESCRIPTIONS

Static Operating Life (statically biased life test at Ta = 150°)
Temperature Humidity Bias Test (85°C/85% RH, preconditioned)
Autoclave (121°C, 100% rel humidity, 15 psig, preconditioned)
Temperature Cycling (-65°C to +150°C, preconditioned)
Preconditioning (IB1 Flow)(MSL Level 1, 3 passes 235°C IR reflow)

6.0 CHARACTERIZATION DATA

Characterization Data

	Average	Sigma	Units
Linearity	-0.9	.09	LSB
Full Scale Error	0.56	0.25	LSB
Zero Error	0.12	0.20	LSB
Resolution	8	0	LSB
Power Supply Sensitivity	0.02	0.05	LSB
Logic Input Threshold	1.26	0.03	V
Logic Input Leakage	0.01	0.02	µA
Logic Out -360µA	2.8	0.01	V
Logic Out 1.6mA	0.24	0.015	V
Output Sink	7.4	0.1	mA
Output Source	2.6	0.05	mA
Tri-State Leakage	0.01	0.02	µA
Supply Current	240	20	µA
Shutdown Current	0.01	0.02	µA
Output Propagation Delay 10pF	20	5	ns
Tri-State Propagation Delay 10pF	20	5	ns

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