National Semiconductor

July 1999

LM2685
Dual Output Regulated Switched Capacitor Voltage Converter

General Description

The LM2685 CMOS charge-pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. Five low cost capacitors are used in this circuit to provide up to 50mA of output current at +5V (± 5%), and 15mA at −5V. The LM2685 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 800µA (operating efficiency greater than 80% with most loads) and 6µA typical shutdown current, the LM2685 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

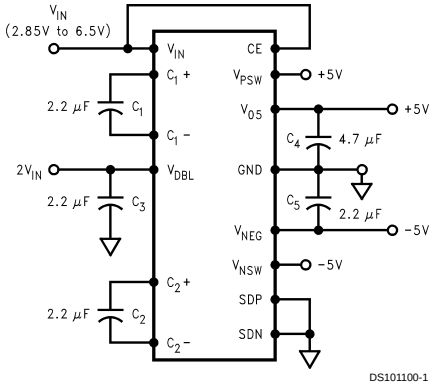
Features

- +5V regulated output
- Inverts V_{05}(+5V) to V_{NEG}(−5V)
- Doubles input supply voltage
- TSSOP-14 package
- 80% typical conversion efficiency at 25mA
- Input voltage range of 2.85V to 6.5V
- Independent shutdown control pins

Applications

- Cellular phones
- Pagers
- PDAs
- Handheld instrumentation
- 3.3V to 5V voltage conversion applications

Typical Application and Connection Diagram



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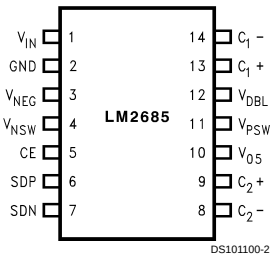


DS101100-2

14-Pin TSSOP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2685MTC	TSSOP-14	MTC14	94 Units, Rail
LM2685MTCX	TSSOP-14	MTC14	2.5k Units, Tape and Reel

Pin Description

Pin No.	Name	Function
1	V_{IN}	Power supply input voltage.
2	GND	Power supply ground.
3	V_{NEG}	Negative output voltage created by inverting V_{05}.
4	V_{NSW}	V_{NEG} output connected through a series switch, NSW.
5	CE	Chip enable input. This pin is high for normal operation and low for shutdown. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
6	SDP	Positive side shutdown input. This pin is low for normal operation and high for positive side shutdown and V_{PSW} load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
7	SDN	Negative side shutdown input. This pin is low for normal operation and high for negative side shutdown and V_{NSW} load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
8	C_2^-	The negative terminal of inverting charge-pump capacitor, C2.
9	C_2^+	The positive terminal of inverting charge-pump capacitor, C2.
10	V_{05}	Regulated +5V output.
11	V_{PSW}	V_{05} output connected through a series switch, PSW.
12	V_{DBL}	Voltage Doubler Output. ($2.85V \leq V_{IN} \leq 5.4V$. See Voltage Doubler section).
13	C_1^+	The positive terminal of doubling charge-pump capacitor, C1.
14	C_1^-	The negative terminal of doubling charge-pump capacitor, C1.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{IN} to GND or GND to V_{NEG})	6.8V
SDN, SDP, CE	(GND − 0.3V) to (V_{IN} + 0.3V)
V_{05} Continuous Output Current	80mA
V_{05} Short-Circuit Duration to GND (Note 2)	Indefinite
Continuous Power Dissipation (T_A = 25˚C) (Note 3)	600mW
T_{JMAX} (Note 3)	150˚C
θ_{JA} (Note 3)	140˚C/W
Operating Ambient Temp. Range	−40˚C to 85˚C
Operating Junction Temp. Range	−40˚C to 125˚C
Storage Temp. Range	−65˚C to 150˚C
Lead Temp. (Soldering, 10 sec.)	300˚C
ESD Rating (Note 4)	2kV

Electrical Characteristics

Limits with standard typeface apply for T_J = 25˚C, and limits in **boldface type** apply over the full temperature range. Unless otherwise specified V_{IN} = 3.6V, C_1 = C_2 = C_3 = C_5 = 2.2µF. C_4 = 4.7µF (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V^+	Supply Voltage		**2.85**		**6.5**	V
I_Q	Supply Current	No Load		800	**1600**	µA
		No Load, V_{IN} = 6.5V		300	**600**	
I_{SD}	Shutdown Supply Current	V_{IN} = 6.5V		6	30	µA
V_{SD}	Shutdown Pin Input Voltage for CE, SDP, SDN	Logic Input High @ 6.5V	**2.4**			V
		Logic Input Low @ 6.5V			**0.8**	
I_L (+5V)	Output Current at V_{05}	2.85V < V_{IN} < 6.5V			**50**	mA
R_O (−5V)	Output Resistance at V_{NEG}	I_L = 15mA (Note 6)		20	**40**	Ω
F_{SW}	Switch Frequency		**85**	130	**180**	kHz
P_{EFF}	Average Power Efficiency at V_{05}	2.85V ≤ V_{IN} ≤ 6.5V I_L = 25mA to GND		82		%
V_{05}	Output Regulation	1mA < I_L < 50mA (Note 7)	4.896	5.10	5.304	V
		1mA < I_L < 50mA (Note 7)	**4.845**	5.10	**5.355**	
G_{LINE}	Line Regulation	2.85V < V_{IN} < 3.6V		0.25		%/V
G_{LOAD}	Load Regulation	1mA < I_L < 50mA		0.3	1.0	%
R_{SW}	Series Switch Resistance V_{NEG} to V_{NSW}	V_{IN} > 2.85V		1.5		Ω
	V_{05} to V_{PSW}			5.0		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: V_{05} may be shorted to GND without damage. However, shorting V_{NEG} to V_{05} may damage the device and must be avoided. Also, for temperature above 85˚C, V_{05} must not be shorted to GND or device may be damaged.

Note 3: The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} — T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package.

Note 4: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

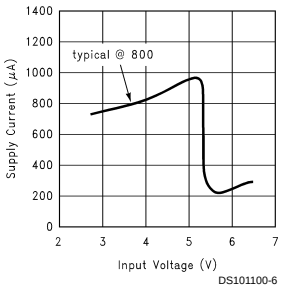
Note 5: In the typical operating circuit, capacitors C_1 and C_2 are 2.2µF, 0.3Ω maximum ESR capacitors. Capacitors with higher ESR will increase output resistance, reduce output voltage and efficiency.

Note 6: Specified output resistance includes internal switch resistance and ESR of capacitors. See the Detailed Device Description section.

Note 7: The 50 mA maximum current assumes no current is drawn from V_{DBL} pin. See Voltage Doubler section in the Detailed Device Description.

Typical Performance Characteristics Unless otherwise specified, T_A = 25˚C, V_{IN} = 3.6V.

Supply Current vs Input Voltage



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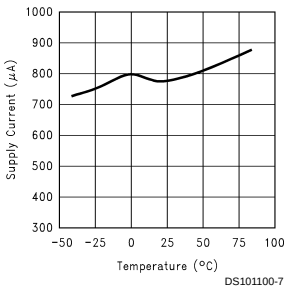
Supply Current vs Temperature



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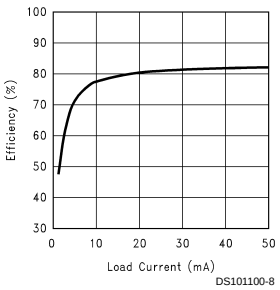
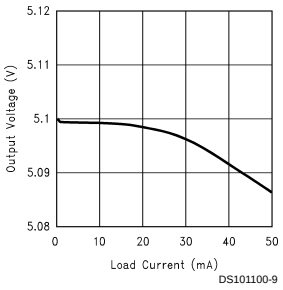
Efficiency vs Load Current



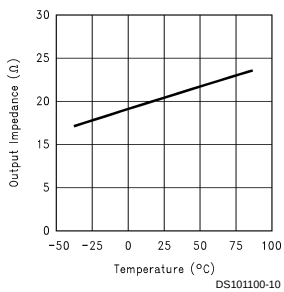
DS101100-8

Output Voltage (V_{05}) vs. Load Current



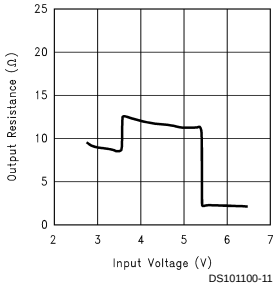
DS101100-9

Output Resistance (VNEG) vs. Temperature



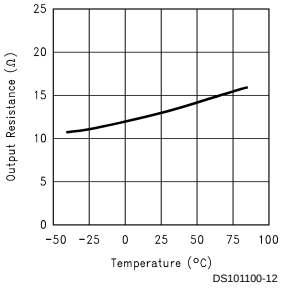
DS101100-10

Output Resistance (VDBL) vs. Input Voltage



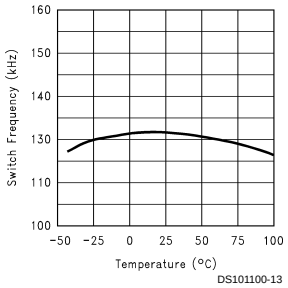
DS101100-11

Output Resistance (VDBL) vs. Temperature



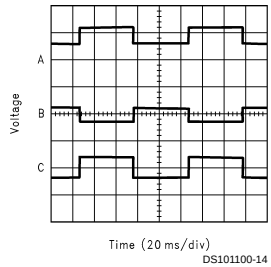
DS101100-12

Switch Frequency vs. Temperature



DS101100-13

Line Transient Response (with 5mA Load)

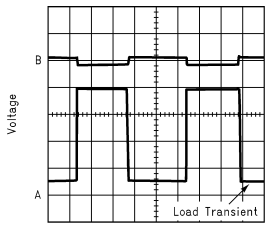


DS101100-14

A: INPUT VOLTAGE: V_{IN} = 3.2V to 6.0V, 5V/div
B: OUTPUT VOLTAGE: V_{PSW}: 100mV/div
C: OUTPUT VOLTAGE: V_{NSW}: 100mV/div

Typical Performance Characteristics Unless otherwise specified, T_A = 25˚C, V_{IN} = 3.6V. (Continued)

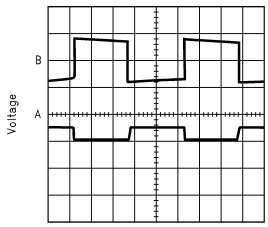
V_{05} Load Transient Response



DS101100-15

A: LOAD CURRENT: I_{LOAD} = 5mA to 39.6mA, 10mA/div
B: OUTPUT VOLTAGE: V_{05}: 10mV/div

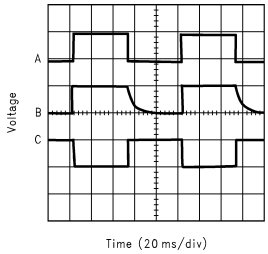
V_{NSW} Load Transient Response



DS101100-16

A: LOAD CURRENT: I_{LOAD} = 4.4mA to −9.4mA, 10mA/div
B: OUTPUT VOLTAGE: V_{NSW}: 50mV/div

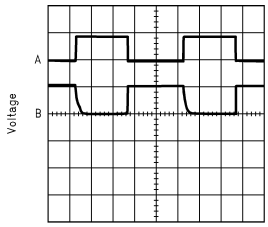
V_{PSW} and V_{NSW} Response to CE (with 5mA Load)



DS101100-17

A: CE INPUT: 5V/div
B: OUTPUT VOLTAGE: V_{PSW}: 5V/div
C: OUTPUT VOLTAGE: V_{NSW}: 5V/div

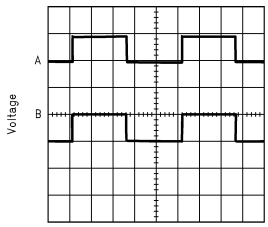
V_{05} Response to SDP (with 5mA Load)



DS101100-18

A: SDP INPUT: 5V/div
B: OUTPUT VOLTAGE: 5V/div

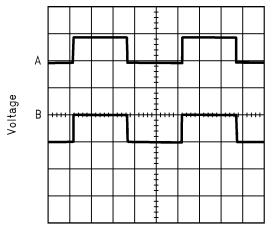
V_{NSW} Response to SDP (with 5mA Load)



DS101100-19

A: SDP INPUT: 5V/div
B: OUTPUT VOLTAGE (V_{NSW}): 5V/div

V_{NSW} Response to SDN (with 5mA Load)



DS101100-20

A: SDN INPUT: 5V/div
B: OUTPUT VOLTAGE (V_{NSW}): 5V/div

Detailed Device Description

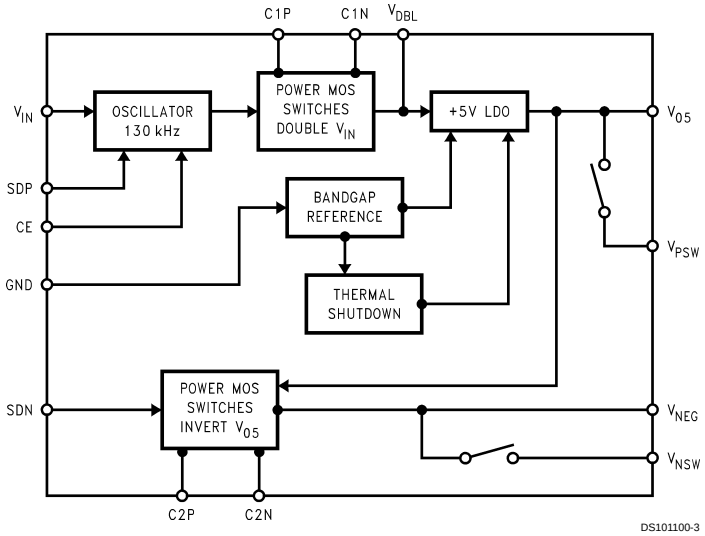


FIGURE 1. Functional Block Diagram

The LM2685 CMOS charge pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. It delivers maximum load currents of 50mA and 15mA for the regulated +5V and the inverted output voltages respectively, with an operating current of only 800µA. It also has a typical shutdown current of 6µA. All these performance qualities make the LM2685 an ideal device for battery powered systems.

The LM2685 has three main functional blocks: a voltage doubler, a low dropout (LDO) regulator, and a voltage inverter. *Figure 1* shows the LM2685 functional block diagram.

Voltage Doubler

The voltage doubler stage doubles the input voltage V_{IN}, within the range of +2.85V to +5.4V. For V_{IN} above 5.4V, the doubler shuts off and the input voltage is passed directly to V_{DBL} via an internal power switch.

The doubler contains four large CMOS switches which are switched in a sequence to double the input supply voltage. *Figure 2* illustrates the voltage conversion scheme. When S2 and S4 are closed, C1 charges to the supply voltage V_{IN}. During this time interval, switches S1 and S3 are open. In the next time interval, S2 and S4 are opened at the same time, S1 and S3 are closed, the sum of the input voltage V_{IN} and the voltage across C1 gives the $2V_{In}$ and the voltage across C1 gives the $2V_{IN}$ at V_{DBL} output. V_{DBL} supplies the LDO regulator. It is recommended not to load V_{DBL} when V_{05} has a load of 50mA. For proper operation, the sum of V_{DBL} and V_{05} loads must not be more than 50mA.

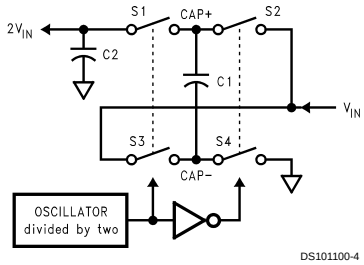


FIGURE 2. Voltage Doubler Principle

+5 LDO Regulator

V_{DBL} is the input to an LDO regulator that regulates it to a +5 output voltage at V_{05}. V_{PSW} is tied to V_{05} through a series switch PSW. The LDO output capacitor (4.7µF Tantalum) may be tied to either V_{05} or V_{PSW}.

Inverter

From the V_{05} output, a −5V output is created at V_{NEG} by means of an inverting charge pump. This negative output is unregulated, meaning that it's output will droop as the load current at V_{NEG} increases. The inverter contains four large CMOS switches which are in a sequence to invert the input supply voltage. *Figure 3* illustrates the voltage conversion scheme. When S1 and S3 are closed, C1 charges to the supply voltage V_{05}. During this time interval, switches S2 and S4 are open. In the second time interval, S1 and S3 are open;at the same time, S2 and S4 are closed, C1 is charging C2. After a number of cycles, the voltage cross C2 will be pumped to V_{05}. Since the anode of C2 is connected to ground, the output at the cathode of C2 equals $-(V_{05})$ when there is no load current. The output voltage drop when a load

Detailed Device Description

(Continued)

is added is determined by the parasitic resistance (R_{ds}(on) of the MOSFET switches and the ESR of the capacitors) and the charge transfer loss between capacitors.

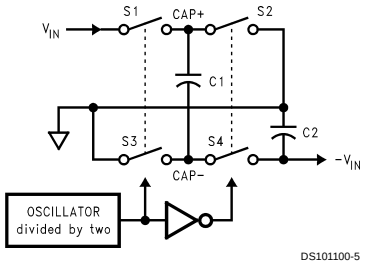


FIGURE 3. Voltage Inverter Principle

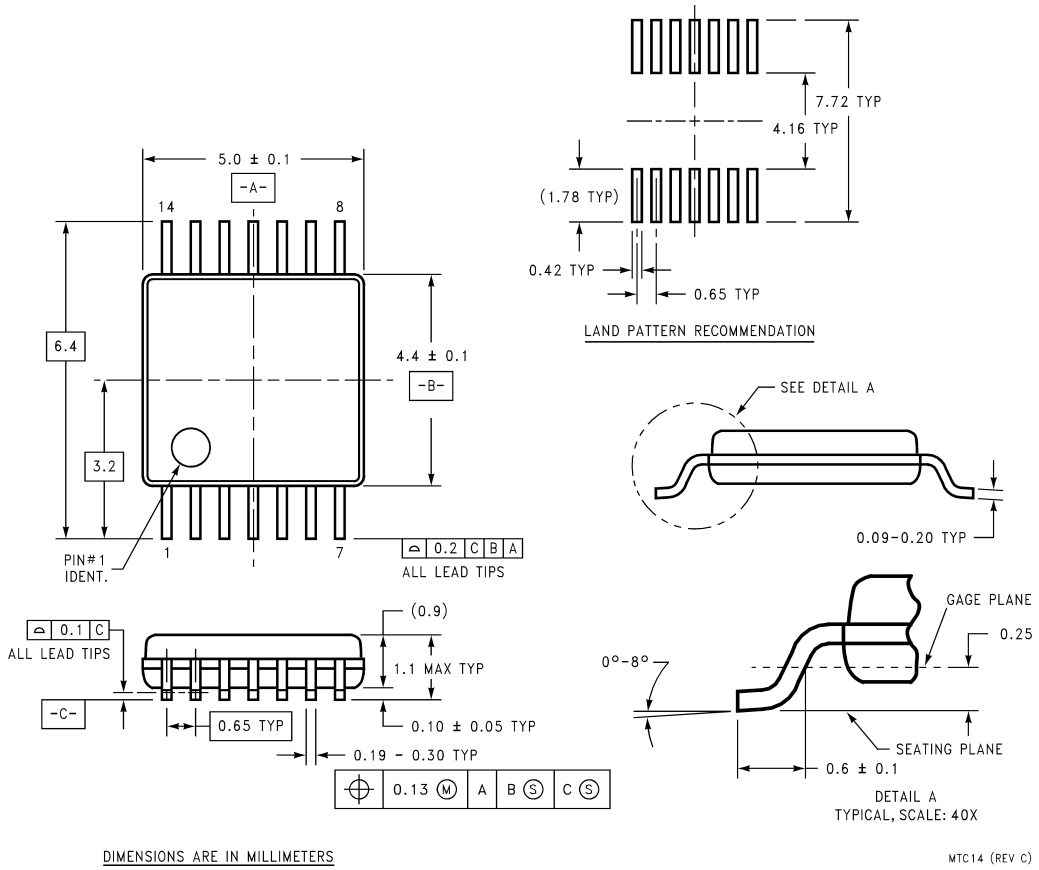
Shutdown and Load Disconnect

In addition to the nominal charge pump and regulator functions, the LM2685 features shutdown and load disconnect circuitry. CE (chip enable) and SDP (shutdown positive) perform the same task with opposite input polarities. When CE is low or SDP is high, all circuit blocks are disabled and V_{05} falls to ground potential. This is the same result as when the die temperature exceeds 150˚C (typical), and the device's internal thermal shutdown is triggered.

Forcing SDN (shutdown negative) high disables only the inverting charge pump. The doubling charge pump and the LDO regulator continue to operate, so the V_{05} and the V_{PSW} remain at 5V.

The LM2685 incorporates two low impedance switches tied to the V_{05} and V_{NEG} outputs, because some special applications require load disconnect and this is achievable via the switches. Switch PSW connects V_{05} to V_{PSW}, and switch NSW connects V_{NEG} to V_{NSW}. In normal operation, these switches are closed, allowing 5V loads to be tied to either V_{05} or V_{PSW} and −5V loads to be tied to either V_{NEG} or V_{NSW}. Driving SDN high opens switch NSW only, while forcing CE low or SDP high, opens both the PSW and NSW.

Physical Dimensions inches (millimeters) unless otherwise noted



TSSOP-14 Package
14-Lead Thin Shrink Small-Outline Package
For Ordering, Refer to Ordering Information Table
NS Package Number MTC14

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