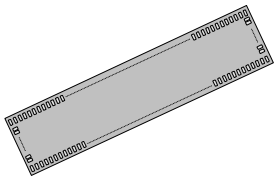
162COMMON x 128RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6825** is a 162COMMON x 128RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 248,832-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16).

In addition, the **NJU6825** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



BUMP CHIP

■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 162-common Drivers x 128RGB Drivers (384-segment Drivers in B&W)
- Built-in Display Data RAM (DDRAM) : 248,832 bits for Graphic Display
- Programmable Display Mode
  - Variable 16-grayscale Mode : 4,096 Colors
  - Variable 8-grayscale Mode : 256 Colors
  - Fixed 8-grayscale Mode : 256 Colors
  - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 7 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- Various Useful Instructions
- Low Operating Current : 450uA Typical at V_{DD}=3V, 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

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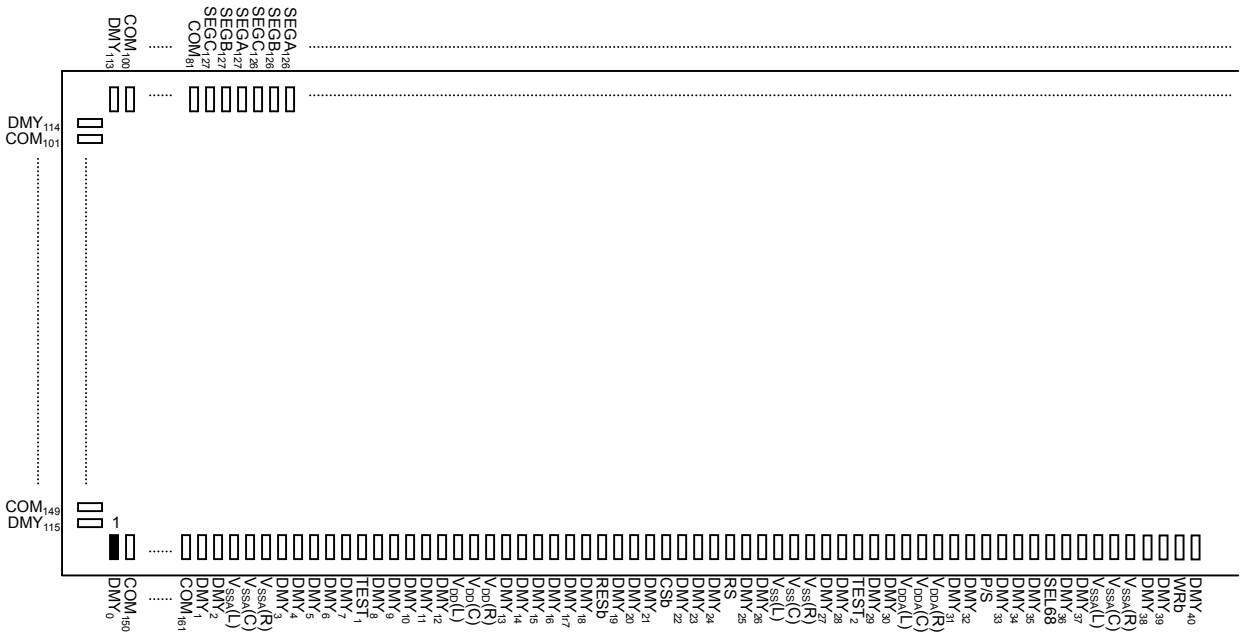
■ PAD LOCATION

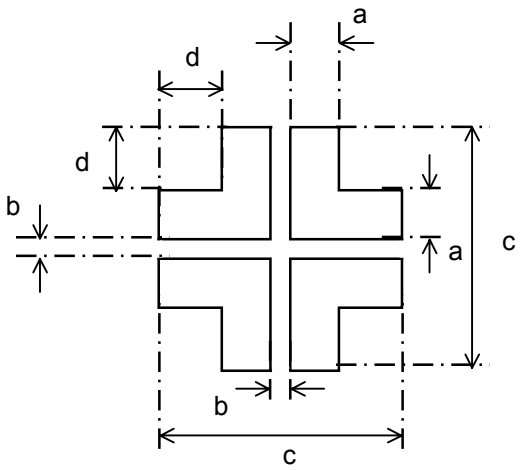


NOTE1) Multiple PADs with successive numbers are internally connected.
NOTE2) Dummy PADs, symbolized with DUMMY, are electrically open.
NOTE3) The purpose of this drawing is to show the order of PADs. Use "PAD CORDINATE TABLE 1 to 6" for design.

Chip Center	:X=0um, Y=0um
Chip Size	:X=20.00mm, Y= 3.13mm
Chip Thickness	:625um ± 25um
Bump Pitch	:45um(Min)
Bump Space	:15um
Bump Size	:32um x 68um (COM/SEG), 47um x 68um (Interface)
	:68um x 68um ($DMY_{0, 109, 110, 111, 112, 113, 114, 115}$)
Bump Height	:17.5um± 3.5um
Bump Material	:Au

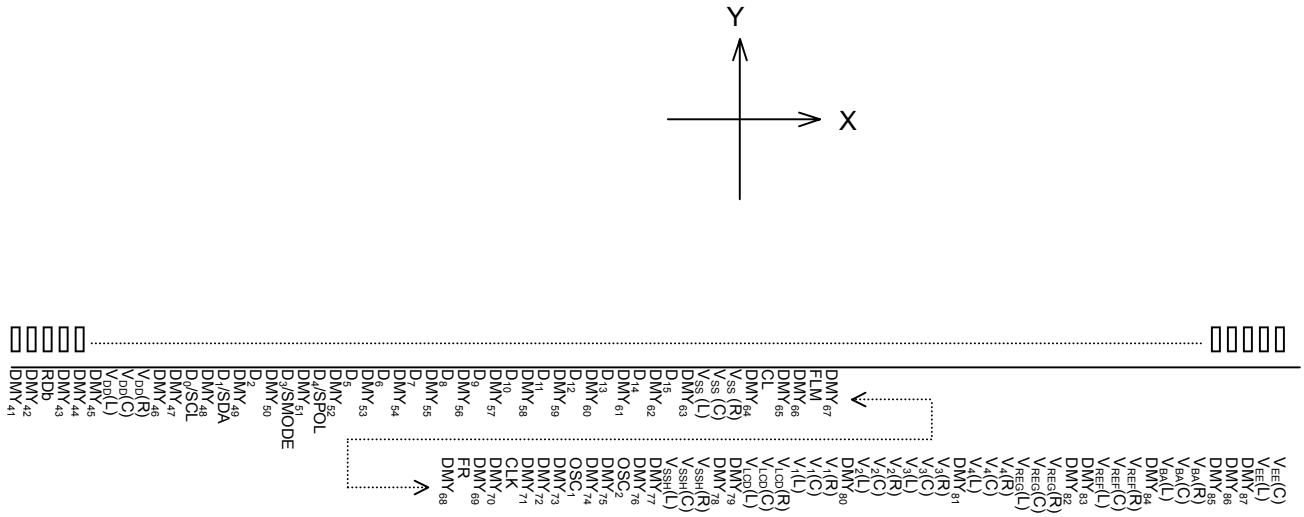
Alignment marks

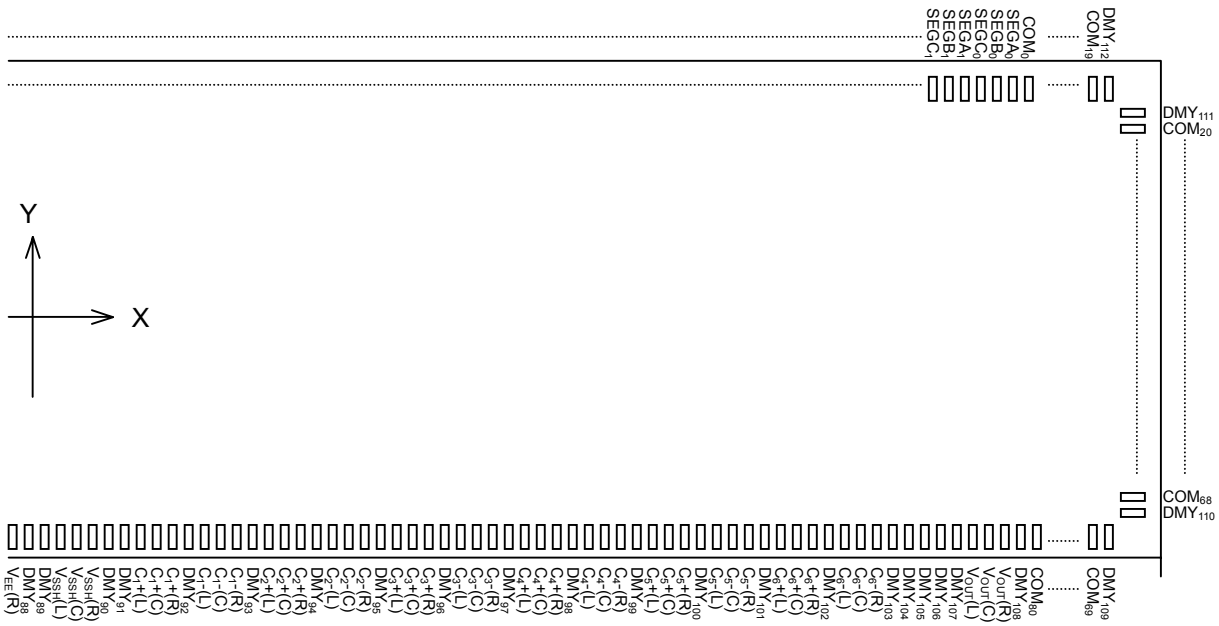
a: 30μm
b: 6μm
c: 120μm
d: 27μm



Alignment mark coordinates

X=-9831μm, Y=-1396μm
X= 9831μm, Y=-1396μm


Y
X
DMY 41
DMY 42
RDb
DMY 43
DMY 44
DMY 45
VDD(L)
VDD(C)
VDD(R)
DMY 46
DMY 47
D0/SCL
DMY 48
D1/SDA
DMY 49
D2
DMY 50
D3/SMODE
DMY 51
D4/SPOL
DMY 52
D5
DMY 53
D6
DMY 54
D7
DMY 55
D8
DMY 56
D9
DMY 57
D10
DMY 58
D11
DMY 59
D12
DMY 60
D13
DMY 61
D14
DMY 62
D15
DMY 63
VSS(L)
VSS(C)
VSS(R)
DMY 64
CL
DMY 65
DMY 66
FLM
DMY 67
A
DMY 68
FR
DMY 69
DMY 70
CLK
DMY 71
DMY 72
DMY 73
OSC1
DMY 74
OSC2
DMY 75
DMY 76
VSSY(L)
DMY 77
VSSH(C)
VSSH(R)
DMY 78
VLCD(L)
VLCD(C)
VLCD(R)
DMY 79
V1(L)
V1(C)
V1(R)
DMY 80
V2(L)
V2(C)
V2(R)
V3(L)
V3(C)
V3(R)
DMY 81
V4(L)
V4(C)
V4(R)
VREG(L)
VREG(C)
VREG(R)
DMY 82
DMY 83
VREF(L)
VREF(C)
VREF(R)
DMY 84
VBA(L)
VBA(C)
VBA(R)
DMY 85
DMY 86
DMY 87
VEE(L)
VEE(C)


SEGC1
SEGB1
SEGA1
SEGC0
SEGB0
SEGA0
COM0
DMY112
COM19
DMY111
COM20
COM68
DMY110
Y
X
VEE(R)
DMY89
VSSH(C)
VSSH(L)
VSSH(R)
DMY90
DMY91
C1+(L)
C1+(C)
C1+(R)
DMY92
C1-(L)
C1-(C)
C1-(R)
DMY93
C2+(L)
C2+(C)
C2+(R)
DMY94
C2-(L)
C2-(C)
C2-(R)
DMY95
C3+(L)
C3+(C)
C3+(R)
DMY96
C3-(L)
C3-(C)
C3-(R)
DMY97
C4+(L)
C4+(C)
C4+(R)
DMY98
C4-(L)
C4-(C)
C4-(R)
DMY99
C5+(L)
C5+(C)
C5+(R)
DMY100
C5-(L)
C5-(C)
C5-(R)
DMY101
C6+(L)
C6+(C)
C6+(R)
DMY102
C6-(L)
C6-(C)
C6-(R)
DMY103
DMY104
DMY105
DMY106
DMY107
VOUT(L)
VOUT(C)
VOUT(R)
DMY108
COM80
DMY109
COM69

■ PAD COORDINATES 1

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)
1	DMY_0	-9581	-1396	52	V_{SS}(R)	-6510	-1396	103	DMY_{55}	-2250	-1396
2	COM_{150}	-9518	-1396	53	DMY_{27}	-6330	-1396	104	D_8	-2130	-1396
3	COM_{151}	-9473	-1396	54	DMY_{28}	-6270	-1396	105	DMY_{56}	-2010	-1396
4	COM_{152}	-9428	-1396	55	$TEST_2$	-6210	-1396	106	D_9	-1890	-1396
5	COM_{153}	-9383	-1396	56	DMY_{29}	-6150	-1396	107	DMY_{57}	-1770	-1396
6	COM_{154}	-9338	-1396	57	DMY_{30}	-6090	-1396	108	D_{10}	-1650	-1396
7	COM_{155}	-9293	-1396	58	V_{DDA}(L)	-6030	-1396	109	DMY_{58}	-1530	-1396
8	COM_{156}	-9248	-1396	59	V_{DDA}(C)	-5970	-1396	110	D_{11}	-1410	-1396
9	COM_{157}	-9203	-1396	60	V_{DDA}(R)	-5910	-1396	111	DMY_{59}	-1290	-1396
10	COM_{158}	-9158	-1396	61	DMY_{31}	-5850	-1396	112	D_{12}	-1170	-1396
11	COM_{159}	-9113	-1396	62	DMY_{32}	-5790	-1396	113	DMY_{60}	-1050	-1396
12	COM_{160}	-9068	-1396	63	P/S	-5730	-1396	114	D_{13}	-930	-1396
13	COM_{161}	-9023	-1396	64	DMY_{33}	-5670	-1396	115	DMY_{61}	-810	-1396
14	DMY_1	-8910	-1396	65	DMY_{34}	-5610	-1396	116	D_{14}	-690	-1396
15	DMY_2	-8850	-1396	66	DMY_{35}	-5550	-1396	117	DMY_{62}	-570	-1396
16	V_{SSA}(L)	-8790	-1396	67	SEL68	-5490	-1396	118	D_{15}	-450	-1396
17	V_{SSA}(C)	-8730	-1396	68	DMY_{36}	-5430	-1396	119	DMY_{63}	-330	-1396
18	V_{SSA}(R)	-8670	-1396	69	DMY_{37}	-5370	-1396	120	V_{SS}(L)	-270	-1396
19	DMY_3	-8610	-1396	70	V_{SSA}(L)	-5310	-1396	121	V_{SS}(C)	-210	-1396
20	DMY_4	-8550	-1396	71	V_{SSA}(C)	-5250	-1396	122	V_{SS}(R)	-150	-1396
21	DMY_5	-8490	-1396	72	V_{SSA}(R)	-5190	-1396	123	DMY_{64}	30	-1396
22	DMY_6	-8430	-1396	73	DMY_{38}	-5130	-1396	124	CL	150	-1396
23	DMY_7	-8370	-1396	74	DMY_{39}	-5070	-1396	125	DMY_{65}	270	-1396
24	$TEST_1$	-8310	-1396	75	WRb	-5010	-1396	126	DMY_{66}	330	-1396
25	DMY_8	-8250	-1396	76	DMY_{40}	-4950	-1396	127	FLM	450	-1396
26	DMY_9	-8190	-1396	77	DMY_{41}	-4890	-1396	128	DMY_{67}	570	-1396
27	DMY_{10}	-8130	-1396	78	DMY_{42}	-4830	-1396	129	DMY_{68}	630	-1396
28	DMY_{11}	-8070	-1396	79	RDb	-4770	-1396	130	FR	750	-1396
29	DMY_{12}	-8010	-1396	80	DMY_{43}	-4710	-1396	131	DMY_{69}	870	-1396
30	V_{DD}(L)	-7950	-1396	81	DMY_{44}	-4650	-1396	132	DMY_{70}	930	-1396
31	V_{DD}(C)	-7890	-1396	82	DMY_{45}	-4590	-1396	133	CLK	1050	-1396
32	V_{DD}(R)	-7830	-1396	83	V_{DD}(L)	-4530	-1396	134	DMY_{71}	1170	-1396
33	DMY_{13}	-7650	-1396	84	V_{DD}(C)	-4470	-1396	135	DMY_{72}	1230	-1396
34	DMY_{14}	-7590	-1396	85	V_{DD}(R)	-4410	-1396	136	DMY_{73}	1290	-1396
35	DMY_{15}	-7530	-1396	86	DMY_{46}	-4230	-1396	137	OSC_1	1350	-1396
36	DMY_{16}	-7470	-1396	87	DMY_{47}	-4170	-1396	138	DMY_{74}	1410	-1396
37	DMY_{17}	-7410	-1396	88	D_0	-4050	-1396	139	DMY_{75}	1470	-1396
38	DMY_{18}	-7350	-1396	89	DMY_{48}	-3930	-1396	140	OSC_2	1650	-1396
39	RESb	-7290	-1396	90	D_1	-3810	-1396	141	DMY_{76}	1830	-1396
40	DMY_{19}	-7230	-1396	91	DMY_{49}	-3690	-1396	142	DMY_{77}	1890	-1396
41	DMY_{20}	-7170	-1396	92	D_2	-3570	-1396	143	V_{SSH}(L)	1950	-1396
42	DMY_{21}	-7110	-1396	93	DMY_{50}	-3450	-1396	144	V_{SSH}(C)	2010	-1396
43	CSb	-7050	-1396	94	D_3	-3330	-1396	145	V_{SSH}(R)	2070	-1396
44	DMY_{22}	-6990	-1396	95	DMY_{51}	-3210	-1396	146	DMY_{78}	2250	-1396
45	DMY_{23}	-6930	-1396	96	D_4	-3090	-1396	147	DMY_{79}	2310	-1396
46	DMY_{24}	-6870	-1396	97	DMY_{52}	-2970	-1396	148	V_{LCD}(L)	2370	-1396
47	RS	-6810	-1396	98	D_5	-2850	-1396	149	V_{LCD}(C)	2430	-1396
48	DMY_{25}	-6750	-1396	99	DMY_{53}	-2730	-1396	150	V_{LCD}(R)	2490	-1396
49	DMY_{26}	-6690	-1396	100	D_6	-2610	-1396	151	V_1(L)	2670	-1396
50	V_{SS}(L)	-6630	-1396	101	DMY_{54}	-2490	-1396	152	V_1(C)	2730	-1396
51	V_{SS}(C)	-6570	-1396	102	D_7	-2370	-1396	153	V_1(R)	2790	-1396

■ PAD COORDINATES 2

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)
154	DMY_{80}	2850	-1396	205	DMY_{95}	6390	-1396	256	COM_{70}	9473	-1396
155	V_2(L)	2910	-1396	206	C_3+(L)	6450	-1396	257	COM_{69}	9518	-1396
156	V_2(C)	2970	-1396	207	C_3+(C)	6510	-1396	258	DMY_{109}	9581	-1396
157	V_2(R)	3030	-1396	208	C_3+(R)	6570	-1396	259	DMY_{110}	9831	-1143
158	V_3(L)	3210	-1396	209	DMY_{96}	6630	-1396	260	COM_{68}	9831	-1080
159	V_3(C)	3270	-1396	210	C_3-(L)	6690	-1396	261	COM_{67}	9831	-1035
160	V_3(R)	3330	-1396	211	C_3-(C)	6750	-1396	262	COM_{66}	9831	-990
161	DMY_{81}	3390	-1396	212	C_3-(R)	6810	-1396	263	COM_{65}	9831	-945
162	V_4(L)	3450	-1396	213	DMY_{97}	6870	-1396	264	COM_{64}	9831	-900
163	V_4(C)	3510	-1396	214	C_4+(L)	6930	-1396	265	COM_{63}	9831	-855
164	V_4(R)	3570	-1396	215	C_4+(C)	6990	-1396	266	COM_{62}	9831	-810
165	V_{REG}(L)	3750	-1396	216	C_4+(R)	7050	-1396	267	COM_{61}	9831	-765
166	V_{REG}(C)	3810	-1396	217	DMY_{98}	7110	-1396	268	COM_{60}	9831	-720
167	V_{REG}(R)	3870	-1396	218	C_4-(L)	7170	-1396	269	COM_{59}	9831	-675
168	DMY_{82}	3930	-1396	219	C_4-(C)	7230	-1396	270	COM_{58}	9831	-630
169	DMY_{83}	3990	-1396	220	C_4-(R)	7290	-1396	271	COM_{57}	9831	-585
170	V_{REF}(L)	4050	-1396	221	DMY_{99}	7350	-1396	272	COM_{56}	9831	-540
171	V_{REF}(C)	4110	-1396	222	C_5+(L)	7410	-1396	273	COM_{55}	9831	-495
172	V_{REF}(R)	4170	-1396	223	C_5+(C)	7470	-1396	274	COM_{54}	9831	-450
173	DMY_{84}	4230	-1396	224	C_5+(R)	7530	-1396	275	COM_{53}	9831	-405
174	V_{BA}(L)	4290	-1396	225	DMY_{100}	7590	-1396	276	COM_{52}	9831	-360
175	V_{BA}(C)	4350	-1396	226	C_5-(L)	7650	-1396	277	COM_{51}	9831	-315
176	V_{BA}(R)	4410	-1396	227	C_5-(C)	7710	-1396	278	COM_{50}	9831	-270
177	DMY_{85}	4470	-1396	228	C_5-(R)	7770	-1396	279	COM_{49}	9831	-225
178	DMY_{86}	4530	-1396	229	DMY_{101}	7830	-1396	280	COM_{48}	9831	-180
179	DMY_{87}	4590	-1396	230	C_6+(L)	7890	-1396	281	COM_{47}	9831	-135
180	V_{EE}(L)	4650	-1396	231	C_6+(C)	7950	-1396	282	COM_{46}	9831	-90
181	V_{EE}(C)	4710	-1396	232	C_6+(R)	8010	-1396	283	COM_{45}	9831	-45
182	V_{EE}(R)	4770	-1396	233	DMY_{102}	8070	-1396	284	COM_{44}	9831	0
183	DMY_{88}	4950	-1396	234	C_6-(L)	8130	-1396	285	COM_{43}	9831	45
184	DMY_{89}	5010	-1396	235	C_6-(C)	8190	-1396	286	COM_{42}	9831	90
185	V_{SSH}(L)	5190	-1396	236	C_6-(R)	8250	-1396	287	COM_{41}	9831	135
186	V_{SSH}(C)	5250	-1396	237	DMY_{103}	8310	-1396	288	COM_{40}	9831	180
187	V_{SSH}(R)	5310	-1396	238	DMY_{104}	8370	-1396	289	COM_{39}	9831	225
188	DMY_{90}	5370	-1396	239	DMY_{105}	8430	-1396	290	COM_{38}	9831	270
189	DMY_{91}	5430	-1396	240	DMY_{106}	8490	-1396	291	COM_{37}	9831	315
190	C_1+(L)	5490	-1396	241	DMY_{107}	8550	-1396	292	COM_{36}	9831	360
191	C_1+(C)	5550	-1396	242	V_{OUT}(L)	8610	-1396	293	COM_{35}	9831	405
192	C_1+(R)	5610	-1396	243	V_{OUT}(C)	8670	-1396	294	COM_{34}	9831	450
193	DMY_{92}	5670	-1396	244	V_{OUT}(R)	8730	-1396	295	COM_{33}	9831	495
194	C_1-(L)	5730	-1396	245	DMY_{108}	8910	-1396	296	COM_{32}	9831	540
195	C_1-(C)	5790	-1396	246	COM_{80}	9023	-1396	297	COM_{31}	9831	585
196	C_1-(R)	5850	-1396	247	COM_{79}	9068	-1396	298	COM_{30}	9831	630
197	DMY_{93}	5910	-1396	248	COM_{78}	9113	-1396	299	COM_{29}	9831	675
198	C_2+(L)	5970	-1396	249	COM_{77}	9158	-1396	300	COM_{28}	9831	720
199	C_2+(C)	6030	-1396	250	COM_{76}	9203	-1396	301	COM_{27}	9831	765
200	C_2+(R)	6090	-1396	251	COM_{75}	9248	-1396	302	COM_{26}	9831	810
201	DMY_{94}	6150	-1396	252	COM_{74}	9293	-1396	303	COM_{25}	9831	855
202	C_2-(L)	6210	-1396	253	COM_{73}	9338	-1396	304	COM_{24}	9831	900
203	C_2-(C)	6270	-1396	254	COM_{72}	9383	-1396	305	COM_{23}	9831	945
204	C_2-(R)	6330	-1396	255	COM_{71}	9428	-1396	306	COM_{22}	9831	990

■ PAD COORDINATES 3

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)
307	COM_{21}	9831	1035	358	$SEGA_{9}$	7403	1396	409	$SEGA_{26}$	5108	1396
308	COM_{20}	9831	1080	359	$SEGB_{9}$	7358	1396	410	$SEGB_{26}$	5063	1396
309	DMY_{111}	9831	1144	360	$SEGC_{9}$	7313	1396	411	$SEGC_{26}$	5018	1396
310	DMY_{112}	9581	1396	361	$SEGA_{10}$	7268	1396	412	$SEGA_{27}$	4973	1396
311	COM_{19}	9518	1396	362	$SEGB_{10}$	7223	1396	413	$SEGB_{27}$	4928	1396
312	COM_{18}	9473	1396	363	$SEGC_{10}$	7178	1396	414	$SEGC_{27}$	4883	1396
313	COM_{17}	9428	1396	364	$SEGA_{11}$	7133	1396	415	$SEGA_{28}$	4838	1396
314	COM_{16}	9383	1396	365	$SEGB_{11}$	7088	1396	416	$SEGB_{28}$	4793	1396
315	COM_{15}	9338	1396	366	$SEGC_{11}$	7043	1396	417	$SEGC_{28}$	4748	1396
316	COM_{14}	9293	1396	367	$SEGA_{12}$	6998	1396	418	$SEGA_{29}$	4703	1396
317	COM_{13}	9248	1396	368	$SEGB_{12}$	6953	1396	419	$SEGB_{29}$	4658	1396
318	COM_{12}	9203	1396	369	$SEGC_{12}$	6908	1396	420	$SEGC_{29}$	4613	1396
319	COM_{11}	9158	1396	370	$SEGA_{13}$	6863	1396	421	$SEGA_{30}$	4568	1396
320	COM_{10}	9113	1396	371	$SEGB_{13}$	6818	1396	422	$SEGB_{30}$	4523	1396
321	COM_{9}	9068	1396	372	$SEGC_{13}$	6773	1396	423	$SEGC_{30}$	4478	1396
322	COM_{8}	9023	1396	373	$SEGA_{14}$	6728	1396	424	$SEGA_{31}$	4433	1396
323	COM_{7}	8978	1396	374	$SEGB_{14}$	6683	1396	425	$SEGB_{31}$	4388	1396
324	COM_{6}	8933	1396	375	$SEGC_{14}$	6638	1396	426	$SEGC_{31}$	4343	1396
325	COM_{5}	8888	1396	376	$SEGA_{15}$	6593	1396	427	$SEGA_{32}$	4298	1396
326	COM_{4}	8843	1396	377	$SEGB_{15}$	6548	1396	428	$SEGB_{32}$	4253	1396
327	COM_{3}	8798	1396	378	$SEGC_{15}$	6503	1396	429	$SEGC_{32}$	4208	1396
328	COM_{2}	8753	1396	379	$SEGA_{16}$	6458	1396	430	$SEGA_{33}$	4163	1396
329	COM_{1}	8708	1396	380	$SEGB_{16}$	6413	1396	431	$SEGB_{33}$	4118	1396
330	COM_{0}	8663	1396	381	$SEGC_{16}$	6368	1396	432	$SEGC_{33}$	4073	1396
331	$SEGA_{0}$	8618	1396	382	$SEGA_{17}$	6323	1396	433	$SEGA_{34}$	4028	1396
332	$SEGB_{0}$	8573	1396	383	$SEGB_{17}$	6278	1396	434	$SEGB_{34}$	3983	1396
333	$SEGC_{0}$	8528	1396	384	$SEGC_{17}$	6233	1396	435	$SEGC_{34}$	3938	1396
334	$SEGA_{1}$	8483	1396	385	$SEGA_{18}$	6188	1396	436	$SEGA_{35}$	3893	1396
335	$SEGB_{1}$	8438	1396	386	$SEGB_{18}$	6143	1396	437	$SEGB_{35}$	3848	1396
336	$SEGC_{1}$	8393	1396	387	$SEGC_{18}$	6098	1396	438	$SEGC_{35}$	3803	1396
337	$SEGA_{2}$	8348	1396	388	$SEGA_{19}$	6053	1396	439	$SEGA_{36}$	3758	1396
338	$SEGB_{2}$	8303	1396	389	$SEGB_{19}$	6008	1396	440	$SEGB_{36}$	3713	1396
339	$SEGC_{2}$	8258	1396	390	$SEGC_{19}$	5963	1396	441	$SEGC_{36}$	3668	1396
340	$SEGA_{2}$	8213	1396	391	$SEGA_{20}$	5918	1396	442	$SEGA_{37}$	3623	1396
341	$SEGB_{3}$	8168	1396	392	$SEGB_{20}$	5873	1396	443	$SEGB_{37}$	3578	1396
342	$SEGC_{3}$	8123	1396	393	$SEGC_{20}$	5828	1396	444	$SEGC_{37}$	3533	1396
343	$SEGA_{4}$	8078	1396	394	$SEGA_{21}$	5783	1396	445	$SEGA_{38}$	3488	1396
344	$SEGB_{4}$	8033	1396	395	$SEGB_{21}$	5738	1396	446	$SEGB_{38}$	3443	1396
345	$SEGC_{4}$	7988	1396	396	$SEGC_{21}$	5693	1396	447	$SEGC_{38}$	3398	1396
346	$SEGA_{5}$	7943	1396	397	$SEGA_{22}$	5648	1396	448	$SEGA_{39}$	3353	1396
347	$SEGB_{5}$	7898	1396	398	$SEGB_{22}$	5603	1396	449	$SEGB_{39}$	3308	1396
348	$SEGC_{5}$	7853	1396	399	$SEGC_{22}$	5558	1396	450	$SEGC_{39}$	3263	1396
349	$SEGA_{6}$	7808	1396	400	$SEGA_{23}$	5513	1396	451	$SEGA_{40}$	3218	1396
350	$SEGB_{6}$	7763	1396	401	$SEGB_{23}$	5468	1396	452	$SEGB_{40}$	3173	1396
351	$SEGC_{6}$	7718	1396	402	$SEGC_{23}$	5423	1396	453	$SEGC_{40}$	3128	1396
352	$SEGA_{7}$	7673	1396	403	$SEGA_{24}$	5378	1396	454	$SEGA_{41}$	3083	1396
353	$SEGB_{7}$	7628	1396	404	$SEGB_{24}$	5333	1396	455	$SEGB_{41}$	3038	1396
354	$SEGC_{7}$	7583	1396	405	$SEGC_{24}$	5288	1396	456	$SEGC_{41}$	2993	1396
355	$SEGA_{8}$	7538	1396	406	$SEGA_{25}$	5243	1396	457	$SEGA_{42}$	2948	1396
356	$SEGB_{8}$	7493	1396	407	$SEGB_{25}$	5198	1396	458	$SEGB_{42}$	2903	1396
357	$SEGC_{8}$	7448	1396	408	$SEGC_{25}$	5153	1396	459	$SEGC_{42}$	2858	1396

■ PAD COORDINATES 4

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)
460	$SEGA_{43}$	2813	1396	511	$SEGA_{60}$	518	1396	562	$SEGA_{77}$	-1778	1396
461	$SEGB_{43}$	2768	1396	512	$SEGB_{60}$	473	1396	563	$SEGB_{77}$	-1823	1396
462	$SEGC_{43}$	2723	1396	513	$SEGC_{60}$	428	1396	564	$SEGC_{77}$	-1868	1396
463	$SEGA_{44}$	2678	1396	514	$SEGA_{61}$	383	1396	565	$SEGA_{78}$	-1913	1396
464	$SEGB_{44}$	2633	1396	515	$SEGB_{61}$	338	1396	566	$SEGB_{78}$	-1958	1396
465	$SEGC_{44}$	2588	1396	516	$SEGC_{61}$	293	1396	567	$SEGC_{78}$	-2003	1396
466	$SEGA_{45}$	2543	1396	517	$SEGA_{62}$	248	1396	568	$SEGA_{79}$	-2048	1396
467	$SEGB_{45}$	2498	1396	518	$SEGB_{62}$	203	1396	569	$SEGB_{79}$	-2093	1396
468	$SEGC_{45}$	2453	1396	519	$SEGC_{62}$	158	1396	570	$SEGC_{79}$	-2138	1396
469	$SEGA_{46}$	2408	1396	520	$SEGA_{63}$	113	1396	571	$SEGA_{80}$	-2183	1396
470	$SEGB_{46}$	2363	1396	521	$SEGB_{63}$	68	1396	572	$SEGB_{80}$	-2228	1396
471	$SEGC_{46}$	2318	1396	522	$SEGC_{63}$	23	1396	573	$SEGC_{80}$	-2273	1396
472	$SEGA_{47}$	2273	1396	523	$SEGA_{64}$	-23	1396	574	$SEGA_{81}$	-2318	1396
473	$SEGB_{47}$	2228	1396	524	$SEGB_{64}$	-68	1396	575	$SEGB_{81}$	-2363	1396
474	$SEGC_{47}$	2183	1396	525	$SEGC_{64}$	-113	1396	576	$SEGC_{81}$	-2408	1396
475	$SEGA_{48}$	2138	1396	526	$SEGA_{65}$	-158	1396	577	$SEGA_{82}$	-2453	1396
476	$SEGB_{48}$	2093	1396	527	$SEGB_{65}$	-203	1396	578	$SEGB_{82}$	-2498	1396
477	$SEGC_{48}$	2048	1396	528	$SEGC_{65}$	-248	1396	579	$SEGC_{82}$	-2543	1396
478	$SEGA_{49}$	2003	1396	529	$SEGA_{66}$	-293	1396	580	$SEGA_{83}$	-2588	1396
479	$SEGB_{49}$	1958	1396	530	$SEGB_{66}$	-338	1396	581	$SEGB_{83}$	-2633	1396
480	$SEGC_{49}$	1913	1396	531	$SEGC_{66}$	-383	1396	582	$SEGC_{83}$	-2678	1396
481	$SEGA_{50}$	1868	1396	532	$SEGA_{67}$	-428	1396	583	$SEGA_{84}$	-2723	1396
482	$SEGB_{50}$	1823	1396	533	$SEGB_{67}$	-473	1396	584	$SEGB_{84}$	-2768	1396
483	$SEGC_{50}$	1778	1396	534	$SEGC_{67}$	-518	1396	585	$SEGC_{84}$	-2813	1396
484	$SEGA_{51}$	1733	1396	535	$SEGA_{68}$	-563	1396	586	$SEGA_{85}$	-2858	1396
485	$SEGB_{51}$	1688	1396	536	$SEGB_{68}$	-608	1396	587	$SEGB_{85}$	-2903	1396
486	$SEGC_{51}$	1643	1396	537	$SEGC_{68}$	-653	1396	588	$SEGC_{85}$	-2948	1396
487	$SEGA_{52}$	1598	1396	538	$SEGA_{69}$	-698	1396	589	$SEGA_{86}$	-2993	1396
488	$SEGB_{52}$	1553	1396	539	$SEGB_{69}$	-743	1396	590	$SEGB_{86}$	-3038	1396
489	$SEGC_{52}$	1508	1396	540	$SEGC_{69}$	-788	1396	591	$SEGC_{86}$	-3083	1396
490	$SEGA_{53}$	1463	1396	541	$SEGA_{70}$	-833	1396	592	$SEGA_{87}$	-3128	1396
491	$SEGB_{53}$	1418	1396	542	$SEGB_{70}$	-878	1396	593	$SEGB_{87}$	-3173	1396
492	$SEGC_{53}$	1373	1396	543	$SEGC_{70}$	-923	1396	594	$SEGC_{87}$	-3218	1396
493	$SEGA_{54}$	1328	1396	544	$SEGA_{71}$	-968	1396	595	$SEGA_{88}$	-3263	1396
494	$SEGB_{54}$	1283	1396	545	$SEGB_{71}$	-1013	1396	596	$SEGB_{88}$	-3308	1396
495	$SEGC_{54}$	1238	1396	546	$SEGC_{71}$	-1058	1396	597	$SEGC_{88}$	-3353	1396
496	$SEGA_{55}$	1193	1396	547	$SEGA_{72}$	-1103	1396	598	$SEGA_{89}$	-3398	1396
497	$SEGB_{55}$	1148	1396	548	$SEGB_{72}$	-1148	1396	599	$SEGB_{89}$	-3443	1396
498	$SEGC_{55}$	1103	1396	549	$SEGC_{72}$	-1193	1396	600	$SEGC_{89}$	-3488	1396
499	$SEGA_{56}$	1058	1396	550	$SEGA_{73}$	-1238	1396	601	$SEGA_{90}$	-3533	1396
500	$SEGB_{56}$	1013	1396	551	$SEGB_{73}$	-1283	1396	602	$SEGB_{90}$	-3578	1396
501	$SEGC_{56}$	968	1396	552	$SEGC_{73}$	-1328	1396	603	$SEGC_{90}$	-3623	1396
502	$SEGA_{57}$	923	1396	553	$SEGA_{74}$	-1373	1396	604	$SEGA_{91}$	-3668	1396
503	$SEGB_{57}$	878	1396	554	$SEGB_{74}$	-1418	1396	605	$SEGB_{91}$	-3713	1396
504	$SEGC_{57}$	833	1396	555	$SEGC_{74}$	-1463	1396	606	$SEGC_{91}$	-3758	1396
505	$SEGA_{58}$	788	1396	556	$SEGA_{75}$	-1508	1396	607	$SEGA_{92}$	-3803	1396
506	$SEGB_{58}$	743	1396	557	$SEGB_{75}$	-1553	1396	608	$SEGB_{92}$	-3848	1396
507	$SEGC_{58}$	698	1396	558	$SEGC_{75}$	-1598	1396	609	$SEGC_{92}$	-3893	1396
508	$SEGA_{59}$	653	1396	559	$SEGA_{76}$	-1643	1396	610	$SEGA_{93}$	-3938	1396
509	$SEGB_{59}$	608	1396	560	$SEGB_{76}$	-1688	1396	611	$SEGB_{93}$	-3983	1396
510	$SEGC_{59}$	563	1396	561	$SEGC_{76}$	-1733	1396	612	$SEGC_{93}$	-4028	1396

■ PAD COORDINATES 5

Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

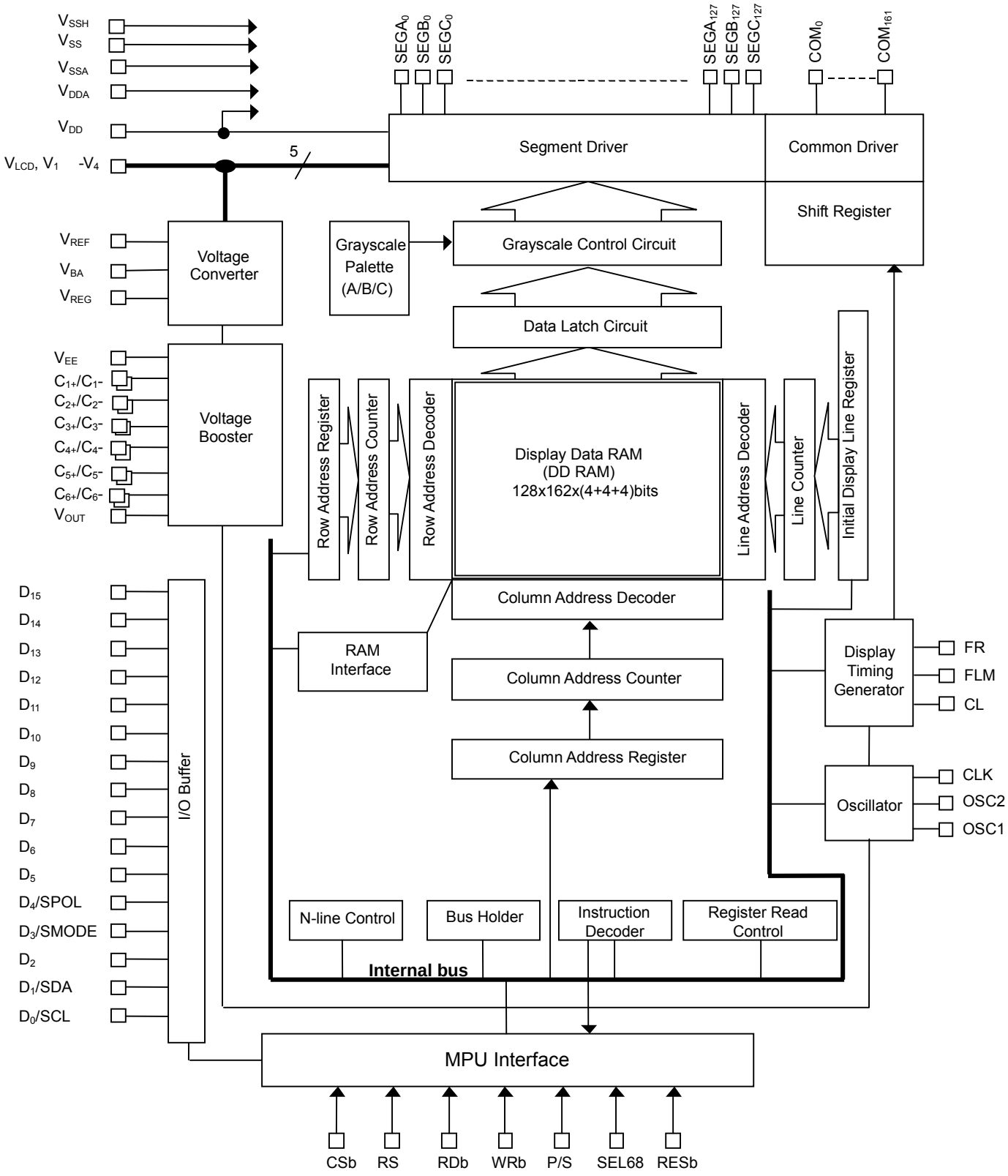
No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)	No.	PAD NAME	X (um)	Y (um)
613	$SEGA_{94}$	-4073	1396	664	$SEGA_{111}$	-6368	1396	715	COM_{81}	-8663	1396
614	$SEGB_{94}$	-4118	1396	665	$SEGB_{111}$	-6413	1396	716	COM_{82}	-8708	1396
615	$SEGC_{94}$	-4163	1396	666	$SEGC_{111}$	-6458	1396	717	COM_{83}	-8753	1396
616	$SEGA_{95}$	-4208	1396	667	$SEGA_{112}$	-6503	1396	718	COM_{84}	-8798	1396
617	$SEGB_{95}$	-4253	1396	668	$SEGB_{112}$	-6548	1396	719	COM_{85}	-8843	1396
618	$SEGC_{95}$	-4298	1396	669	$SEGC_{112}$	-6593	1396	720	COM_{86}	-8888	1396
619	$SEGA_{96}$	-4343	1396	670	$SEGA_{113}$	-6638	1396	721	COM_{87}	-8933	1396
620	$SEGB_{96}$	-4388	1396	671	$SEGB_{113}$	-6683	1396	722	COM_{88}	-8978	1396
621	$SEGC_{96}$	-4433	1396	672	$SEGC_{113}$	-6728	1396	723	COM_{89}	-9023	1396
622	$SEGA_{97}$	-4478	1396	673	$SEGA_{114}$	-6773	1396	724	COM_{90}	-9068	1396
623	$SEGB_{97}$	-4523	1396	674	$SEGB_{114}$	-6818	1396	725	COM_{91}	-9113	1396
624	$SEGC_{97}$	-4568	1396	675	$SEGC_{114}$	-6863	1396	726	COM_{92}	-9158	1396
625	$SEGA_{98}$	-4613	1396	676	$SEGA_{115}$	-6908	1396	727	COM_{93}	-9203	1396
626	$SEGB_{98}$	-4658	1396	677	$SEGB_{115}$	-6953	1396	728	COM_{94}	-9248	1396
627	$SEGC_{98}$	-4703	1396	678	$SEGC_{115}$	-6998	1396	729	COM_{95}	-9293	1396
628	$SEGA_{99}$	-4748	1396	679	$SEGA_{116}$	-7043	1396	730	COM_{96}	-9338	1396
629	$SEGB_{99}$	-4793	1396	680	$SEGB_{116}$	-7088	1396	731	COM_{97}	-9383	1396
630	$SEGC_{99}$	-4838	1396	681	$SEGC_{116}$	-7133	1396	732	COM_{98}	-9428	1396
631	$SEGA_{100}$	-4883	1396	682	$SEGA_{117}$	-7178	1396	733	COM_{99}	-9473	1396
632	$SEGB_{100}$	-4928	1396	683	$SEGB_{117}$	-7223	1396	734	COM_{100}	-9518	1396
633	$SEGC_{100}$	-4973	1396	684	$SEGC_{117}$	-7268	1396	735	DMY_{113}	-9581	1396
634	$SEGA_{101}$	-5018	1396	685	$SEGA_{118}$	-7313	1396	736	DMY_{114}	-9831	1143
635	$SEGB_{101}$	-5063	1396	686	$SEGB_{118}$	-7358	1396	737	COM_{101}	-9831	1080
636	$SEGC_{101}$	-5108	1396	687	$SEGC_{118}$	-7403	1396	738	COM_{102}	-9831	1035
637	$SEGA_{102}$	-5153	1396	688	$SEGA_{119}$	-7448	1396	739	COM_{103}	-9831	990
638	$SEGB_{102}$	-5198	1396	689	$SEGB_{119}$	-7493	1396	740	COM_{104}	-9831	945
639	$SEGC_{102}$	-5243	1396	690	$SEGC_{119}$	-7538	1396	741	COM_{105}	-9831	900
640	$SEGA_{103}$	-5288	1396	691	$SEGA_{120}$	-7583	1396	742	COM_{106}	-9831	855
641	$SEGB_{103}$	-5333	1396	692	$SEGB_{120}$	-7628	1396	743	COM_{107}	-9831	810
642	$SEGC_{103}$	-5378	1396	693	$SEGC_{120}$	-7673	1396	744	COM_{108}	-9831	765
643	$SEGA_{104}$	-5423	1396	694	$SEGA_{121}$	-7718	1396	745	COM_{109}	-9831	720
644	$SEGB_{104}$	-5468	1396	695	$SEGB_{121}$	-7763	1396	746	COM_{110}	-9831	675
645	$SEGC_{104}$	-5513	1396	696	$SEGC_{121}$	-7808	1396	747	COM_{111}	-9831	630
646	$SEGA_{105}$	-5558	1396	697	$SEGA_{122}$	-7853	1396	748	COM_{112}	-9831	585
647	$SEGB_{105}$	-5603	1396	698	$SEGB_{122}$	-7898	1396	749	COM_{113}	-9831	540
648	$SEGC_{105}$	-5648	1396	699	$SEGC_{122}$	-7943	1396	750	COM_{114}	-9831	495
649	$SEGA_{106}$	-5693	1396	700	$SEGA_{123}$	-7988	1396	751	COM_{115}	-9831	450
650	$SEGB_{106}$	-5738	1396	701	$SEGB_{123}$	-8033	1396	752	COM_{116}	-9831	405
651	$SEGC_{106}$	-5783	1396	702	$SEGC_{123}$	-8078	1396	753	COM_{117}	-9831	360
652	$SEGA_{107}$	-5828	1396	703	$SEGA_{124}$	-8123	1396	754	COM_{118}	-9831	315
653	$SEGB_{107}$	-5873	1396	704	$SEGB_{124}$	-8168	1396	755	COM_{119}	-9831	270
654	$SEGC_{107}$	-5918	1396	705	$SEGC_{124}$	-8213	1396	756	COM_{120}	-9831	225
655	$SEGA_{108}$	-5963	1396	706	$SEGA_{125}$	-8258	1396	757	COM_{121}	-9831	180
656	$SEGB_{108}$	-6008	1396	707	$SEGB_{125}$	-8303	1396	758	COM_{122}	-9831	135
657	$SEGC_{108}$	-6053	1396	708	$SEGC_{125}$	-8348	1396	759	COM_{123}	-9831	90
658	$SEGA_{109}$	-6098	1396	709	$SEGA_{126}$	-8393	1396	760	COM_{124}	-9831	45
659	$SEGB_{109}$	-6143	1396	710	$SEGB_{126}$	-8438	1396	761	COM_{125}	-9831	0
660	$SEGC_{109}$	-6188	1396	711	$SEGC_{126}$	-8483	1396	762	COM_{126}	-9831	-45
661	$SEGA_{110}$	-6233	1396	712	$SEGA_{127}$	-8528	1396	763	COM_{127}	-9831	-90
662	$SEGB_{110}$	-6278	1396	713	$SEGB_{127}$	-8573	1396	764	COM_{128}	-9831	-135
663	$SEGC_{110}$	-6323	1396	714	$SEGC_{127}$	-8618	1396	765	COM_{129}	-9831	-180

■ PAD COORDINATES 6

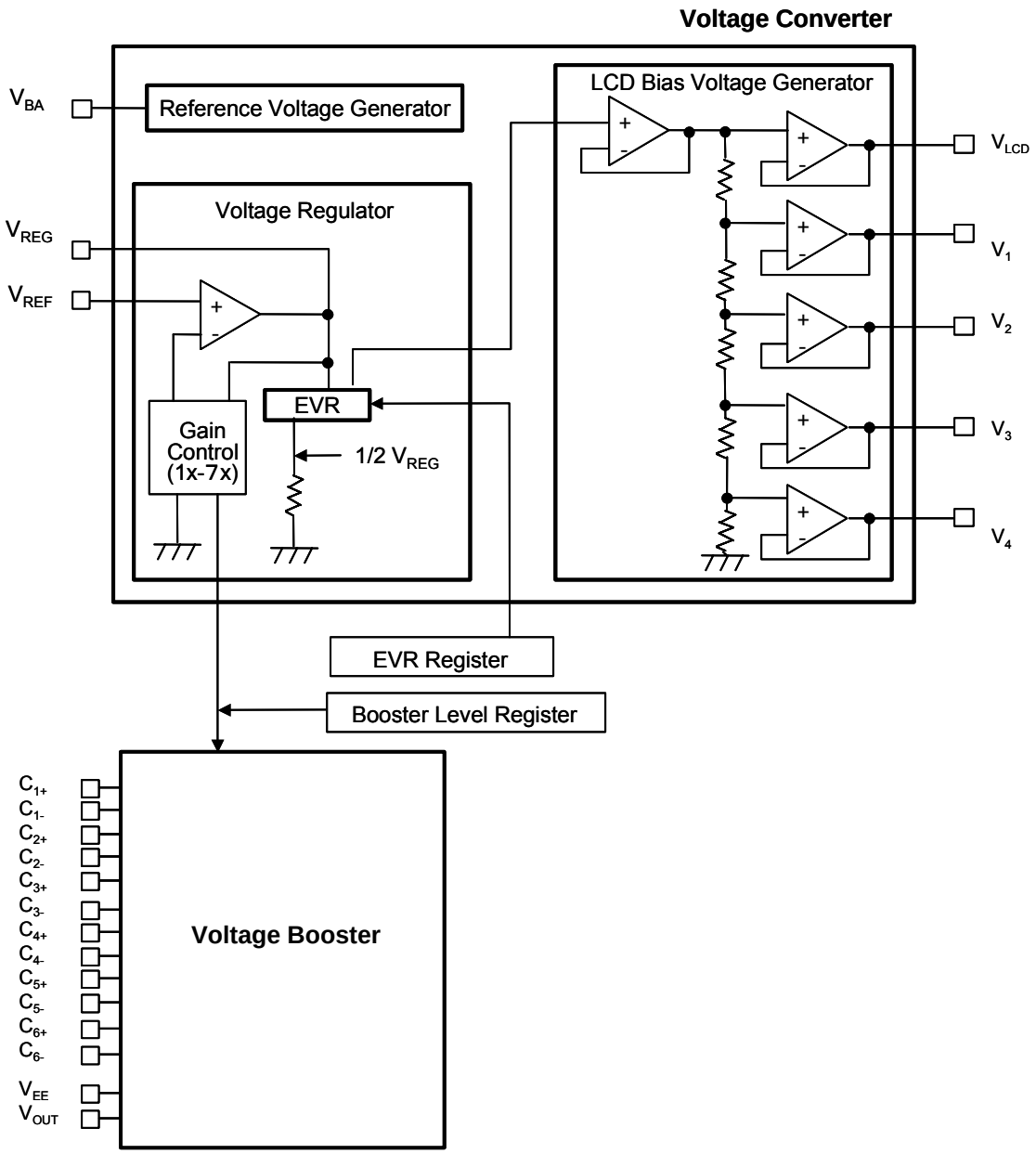
Chip Size 20000μm x 3130μm (Chip Center 0μm x 0μm)

No.	PAD NAME	X (um)	Y (um)
766	COM_{130}	-9831	-225
767	COM_{131}	-9831	-270
768	COM_{132}	-9831	-315
769	COM_{133}	-9831	-360
770	COM_{134}	-9831	-405
771	COM_{135}	-9831	-450
772	COM_{136}	-9831	-495
773	COM_{137}	-9831	-540
774	COM_{138}	-9831	-585
775	COM_{139}	-9831	-630
776	COM_{140}	-9831	-675
777	COM_{141}	-9831	-720
778	COM_{142}	-9831	-765
779	COM_{143}	-9831	-810
780	COM_{144}	-9831	-855
781	COM_{145}	-9831	-900
782	COM_{146}	-9831	-945
783	COM_{147}	-9831	-990
784	COM_{148}	-9831	-1035
785	COM_{149}	-9831	-1080
786	DMY_{115}	-9831	-1144

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function
30~32, 83-85	V_{DD}	Power	Power Supply for Logic Circuits
50-52, 120-122	V_{SS}	Power	GND for Logic Circuits
143~145 185~187	V_{SSH}	Power	GND for High Voltage Circuits
58~60	V_{DDA}	Power	V_{DDA} is internally connected to V_{DD} to fix SEL68 or P/S to "H" if necessary, and cannot be used as main power supply. • V_{DDA} should be open if not used.
16~18, 70~72	V_{SSA}	Power	V_{SSA} is internally connected to V_{SS} to fix SEL68 or P/S to "L" if necessary, and cannot be used as main GND. • V_{SSA} should be open if not used.
148-150, 151-153, 155-157, 158-160, 162-164	V_{LCD} V_1 V_2 V_3 V_4	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V_{LCD} and V_1-V_4) are activated by the "Power Control" instruction. Stabilizing capacitors are required between each bias voltage and V_{SS}. • When the external LCD power supply is used, LCD bias voltages are externally supplied on V_{LCD}, V_1, V_2, V_3 and V_4 individually, with the following relation maintained: $V_{SSH}<V_4<V_3<V_2<V_1<V_{LCD}$
190-192, 194-196	C_{1+} C_{1-}	Power	Capacitor Connection for Voltage Booster
198-200, 202-204	C_{2+} C_{2-}	Power	Capacitor Connection for Voltage Booster
206-208, 210-212	C_{3+} C_{3-}	Power	Capacitor Connection for Voltage Booster
214-216, 218-220	C_{4+} C_{4-}	Power	Capacitor Connection for Voltage Booster
222-224, 226-228	C_{5+} C_{5-}	Power	Capacitor Connection for Voltage Booster
230-232, 234-236	C_6+ C_{6-}	Power	Capacitor Connection for Voltage Booster
174-176	V_{BA}	Power	Reference-Voltage Generator Output
170-172	V_{REF}	Power	Voltage Regulator Input
180-182	V_{EE}	Power	Voltage Booster Input • V_{EE} is normally connected to V_{DD}.
242-244	V_{OUT}	Power	Voltage Booster Output • Input if an external LCD power supply is used.
165-167	V_{REG}	Power	Voltage Regulator Output
39	RESb	I	Reset • Active "L"

■ TERMINAL DESCRIPTION 2

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Function</th></tr>
<tr><td>88</td><td>D_0
/SCL</td><td>I/O</td><td rowspan="5">1. Parallel Interface
D_7 to D_0 : 8-bit Bi-directional Bus

• In the parallel interface mode (P/S="H"), D_7-D_0 are connected to 8-bit bi-directional MPU bus.

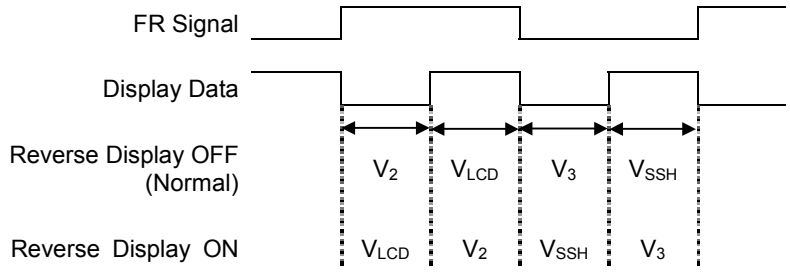
Serial Interface
SDA : Serial Data
SCL : Serial Clock
SMODE : 3-/4-line Serial Mode Select
SPOL : RS Polarity Select (3-line Serial Interface Mode)

• In the 3 or 4-line serial interface mode (P/S="L"), D_0 is assigned to SCL, and D_1 to SDA.
• In the 3-line serial interface mode, D_4 is assigned to SPOL.
• Serial data on SDA is latched at the rising edge of SCL signal in order of D_7, D_6,… and D_0, and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL.
• SCL should be set to "L" right after data transmission or during non-access.</td></tr>
<tr><td>90</td><td>D_1
/SDA</td><td>I/O</td></tr>
<tr><td>94</td><td>D_3
/SMODE</td><td>I/O</td></tr>
<tr><td>96</td><td>D_4
/SPOL</td><td>I/O</td></tr>
<tr><td>92, 98,
100,102</td><td>D_2
D_5
D_6
D_7</td><td>I/O</td></tr>
<tr><td>104,106,108,
110,112,114,
116,118</td><td>D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}</td><td>I/O</td><td>8-bit Bi-directional Bus
• In the 16-bit bus length mode, D_{15}-D_8 are assigned to upper 8-bit data bus.
• In the serial interface mode or the 8-bit parallel interface mode, D_{15}-D_8 should be fixed to "H" or "L".</td></tr>
<tr><td>43</td><td>CSb</td><td>I</td><td>Chip Select
• Active "L"</td></tr>
<tr><td>47</td><td>RS</td><td>I</td><td>Register Select
• This signal interprets transferred data as display data or instruction.
<table><tr><th>RS</th><th>H</th><th>L</th></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table></td></tr>
<tr><td>79</td><td>RDb (E)</td><td>I</td><td>80-series MPU Interface (P/S="H", SEL68="L")
Data Read (RDb) Signal
• Active "L"
68-series MPU Interface (P/S="H", SEL68="H")
Enable Signal
• Active "H"</td></tr>
<tr><td>75</td><td>WRb (R/W)</td><td>I</td><td>80-series MPU Interface (P/S="H", SEL68="L")
Data Write (WRb) Signal
• Active "L"
68-series MPU Interface (P/S="H", SEL68="H")
Data Read or Write (R/W) Signal
<table><tr><th>R/W</th><th>H</th><th>L</th></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table></td></tr>
<tr><td>24</td><td>$TEST_1$</td><td>I</td><td>Maker test terminal
This terminal must be fixed to "L" in the user's application.</td></tr>
<tr><td>55</td><td>$TEST_2$</td><td>I</td><td>Maker test terminal
This terminal must be fixed to "H" in the user's application.</td></tr>
</table>

■ TERMINAL DESCRIPTION 3

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Function</th></tr>
<tr><td>67</td><td>SEL68</td><td>I</td><td>MPU Mode Select
<table><tr><td>SEL86</td><td>H</td><td>L</td></tr><tr><td>MPU</td><td>68-series</td><td>80-series</td></tr></table></td></tr>
<tr><td>63</td><td>P/S</td><td>I</td><td>Parallel/Serial Interface Mode Select
<table><tr><td>P/S</td><td>Chip Select</td><td>Display / Instruction</td><td>Data</td><td>Read /Write</td><td>Serial Clock</td></tr><tr><td>H</td><td>CSb</td><td>RS</td><td>D_0 ~ D_7</td><td>RDb, WRb</td><td>-</td></tr><tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D_1)</td><td>Write Only</td><td>SCL (D_0)</td></tr></table>• In the serial interface mode (P/S=“L”), RDb, WRb, D_2 and D_5-D_{15} should be fixed to “H” or “L”,.</td></tr>
<tr><td>124</td><td>CL</td><td>O</td><td>Line Clock
• CL is normally open.</td></tr>
<tr><td>127</td><td>FLM</td><td>O</td><td>First Line Maker
• FLM is normally open.</td></tr>
<tr><td>130</td><td>FR</td><td>O</td><td>Frame Rate
• FR is normally open.</td></tr>
<tr><td>133</td><td>CLK</td><td>O</td><td>Clock Output
• CLK is normally open.</td></tr>
<tr><td>137,
140</td><td>OSC1
OSC2</td><td>I
O</td><td>OSC
• When the internal oscillator is used, fix OSC1 to “H” or “L” and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor.
• When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.</td></tr>
<tr><td>331-714</td><td>$SEGA_0$
~$SEGA_{127}$

$SEGB_0$
~$SEGB_{127}$

$SEGC_0$
~$SEGC_{127}$</td><td>O</td><td>Segment Drivers
<table><tr><td>REV Register</td><td>OFF</td><td>ON</td></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>• Segment drivers output the following voltage levels.
<u>B/W Mode (Example)</u>
  </td></tr>
<tr><td>311-330,
260-308,
246-257,
715-734,
737-785,
2-13</td><td>COM_0 ~
COM_{161}</td><td>O</td><td>Common Drivers
• Common drivers output the following voltage levels.
<table><tr><td>Data</td><td>FR</td><td>Output Levels</td></tr><tr><td>H</td><td>H</td><td>V_{SSH}</td></tr><tr><td>L</td><td>H</td><td>V_1</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V_4</td></tr></table></td></tr>
</table>

NOTE) DUMMY PADs: No. 14, 15, 20-23, 25-29, 33-38, 40-42, 44-46, 48, 49, 53, 54, 56, 57, 61, 62, 64-66, 68, 69, 73, 74, 76-78, 80-82, 86, 87, 89, 91, 93, 95, 97, 99, 101, 103, 105, 107, 109, 111, 113, 115, 117, 119, 123, 125, 126, 128, 129, 131, 132, 134-136, 138, 139, 141, 142, 146, 147, 154, 161, 168, 169, 173, 177-179, 183, 184, 188, 189, 193, 197, 201, 205, 209, 213, 217, 221, 225, 229, 233, 237-241, 245, 258, 259, 309, 310, 735, 736, and 786.

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) " -" : Fix to "H" or "L".

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D_7-D_0 (D_{15}-D_0)
L	80-series MPU	CSb	RS	RDb	WRb	D_7-D_0 (D_{15}-D_0)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is inactive (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D_7, D_6,…, and D_0, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb="H") temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

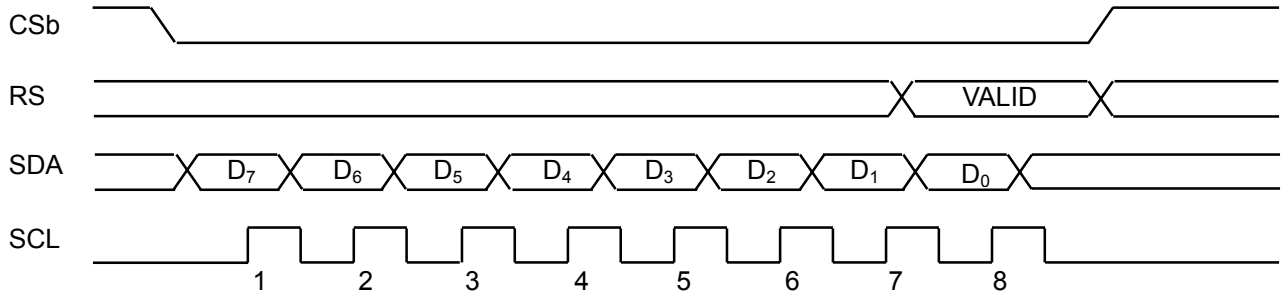


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is not active (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D_7, D_6,…, and D_0, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9th SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb="H") temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

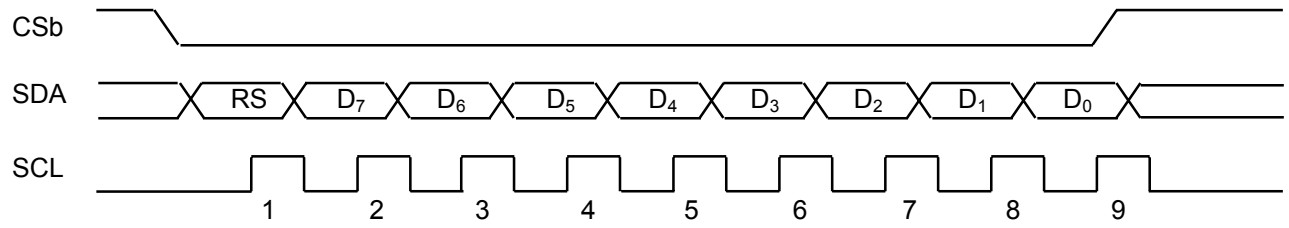


Fig 2 3-line Serial Interface Timing

(1-7) Accessing DDRAM

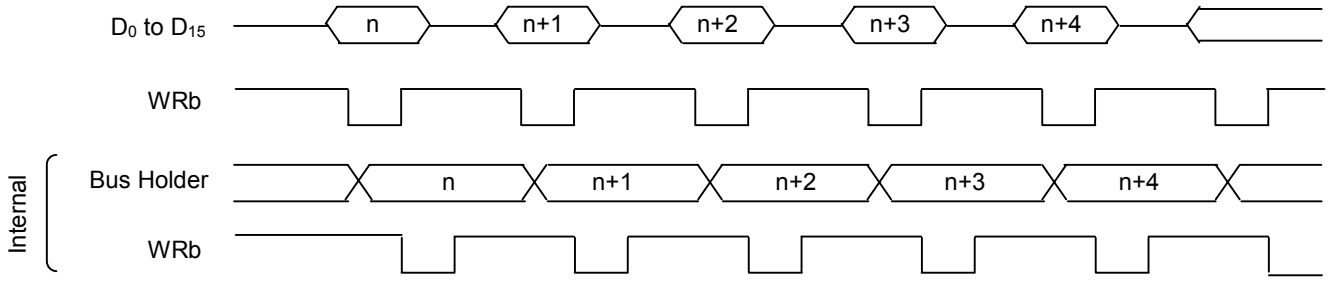
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

Display Data Write Operation



Display Data Read Operation

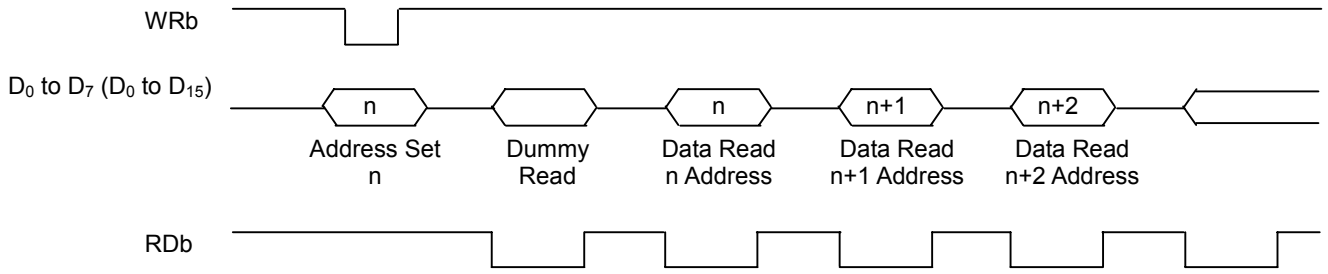


Fig 3 Internal-signal Timing of Display Data Read/Write Operations

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

(1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the "Register Address" and "Register Read" instructions. For more information, refer to "(14-23) Register Address" and "(14-24) Register Read".

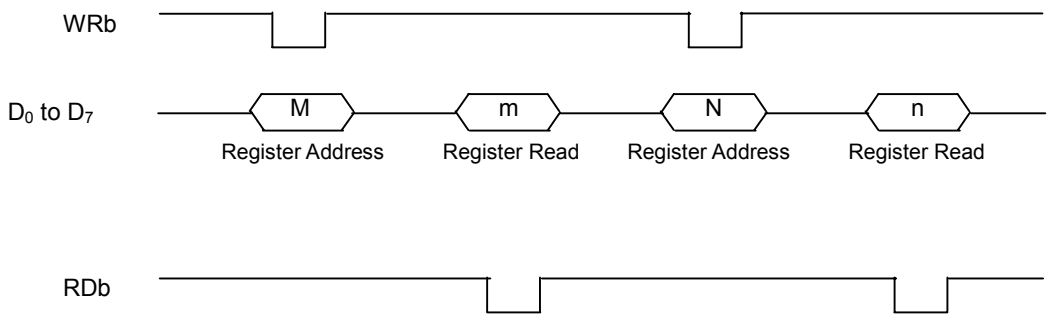


Fig 4 Access Timing of Instruction Register

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D_0 (WLS) bit of the "Bus Length" instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D_{15} to D_0). However, only lower 8 bits (D_7 to D_0) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D_{15} to D_0) are transmitted for DDRAM access. For more information, refer to "(4-4) Bit Assignment of Display Data".

Table 8 Selection of 8-/16-bit Bus Length Mode

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

(2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the "Initial COM" instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes "H". At the rising edge of the CL signal, the line counter is counted-up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers Ai, Bi and Ci (i=0 to 127) generate LCD waveforms.

(3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

(4) DDRAM

(4-1) DDRAM Address Range

The DDRAM is capable of 162 bits for row address and 1,536 bits (12-bit x 128-segment) for column address. The range of the column address is varied depending on the settings as follows, and the row address is from (00H) to (A1H). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

8-bit Bus Length

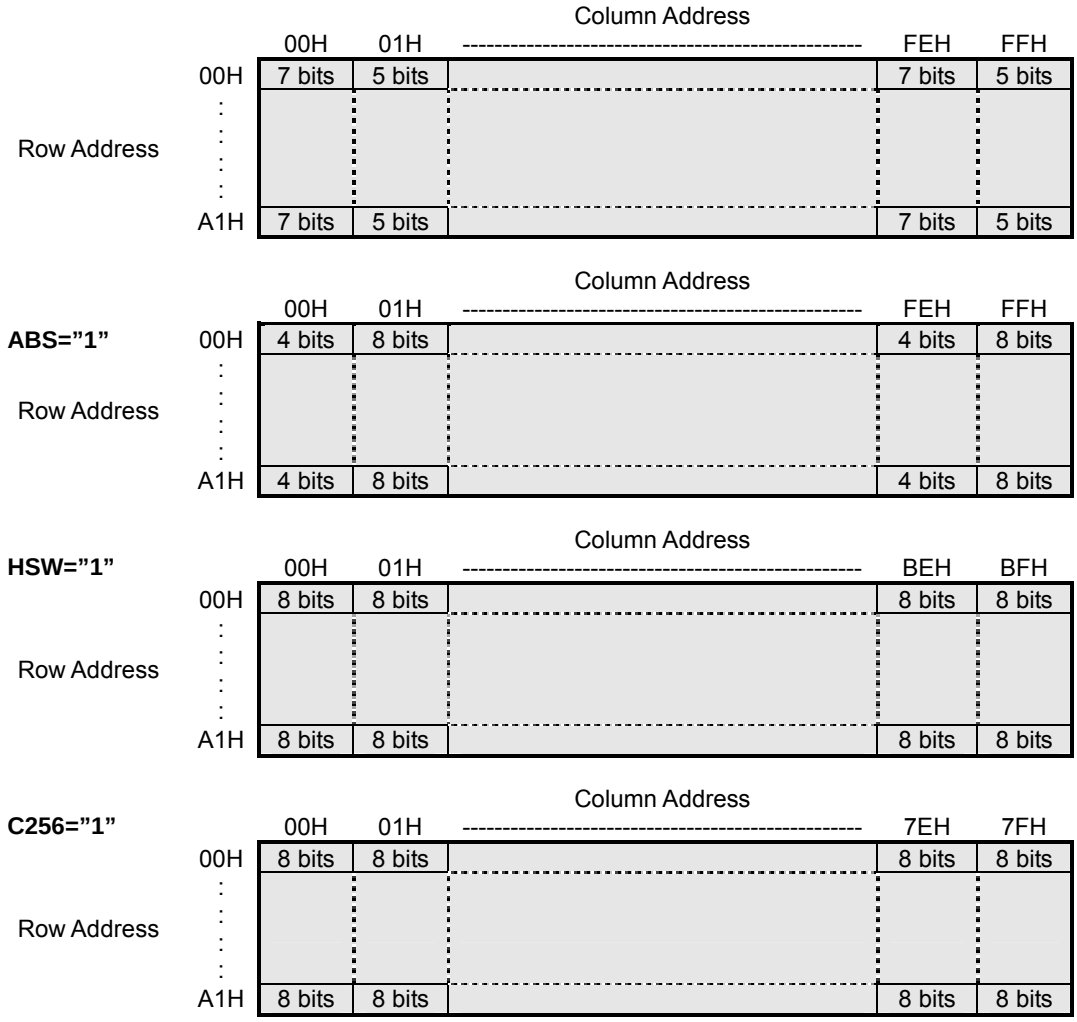


Fig 5 Range of Column Address in 8-bit Bus Length

16-bit Bus Length

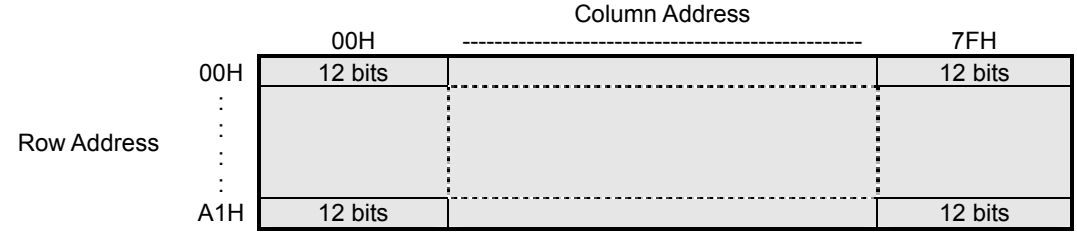


Fig 6 Range of Column Address in 16-bit Bus Length

(4-2) Window Area for DDRAM Access

In addition to the normal DDRAM access discussed previously, the window area access can be used. This area is set by the "Increment Control" instruction and the designation of the start point and the end point.

By the "Increment Control", auto-increment is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up , whenever the DDRAM is accessed. And, the start point is specified by the "Column Address" and "Row Address" instructions, and the end point by the "Window End Column Address" and "Window End Row Address" instructions. For more information, refer to "(14-9) Increment Control", "(14-25) Window End Column Address" and "(14-26)Window End Row Address". The typical sequence of the window area setting is listed below.

1. Set "1" at D_3 (WIN), D_1 (AYI) and D_0 (AXI) of "Increment Control" instruction.
2. Set start point by "Column Address" and "Row Address" instructions.
3. Set end point by "Window End Column Address" and "Window End Row Address" instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.

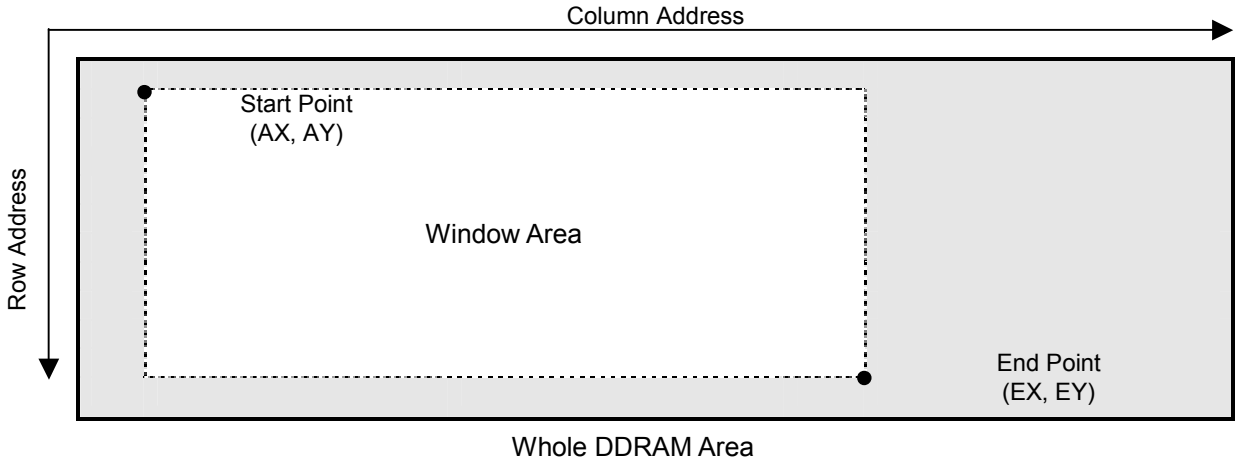
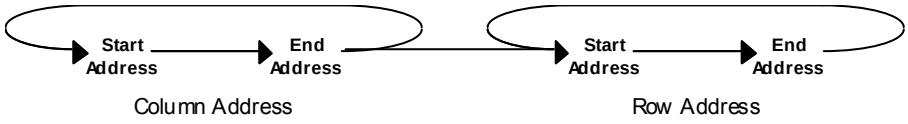


Fig 7 Window Area

NOTE1) The following relation should be maintained to avoid malfunctions.
- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE3) Auto-increment in the window area



NOTE2) A read-modify-write operation is enabled by setting "1" at the D_2 (AIM) of the "Increment Control" instruction. Refer to the description about "AIM" bit in "(14-9) Increment Control".

(4-3) Segment Direction

The DDRAM access direction is controlled by the D_0 (REF) bit of the "Display Control (2)" instruction. This function is used to reverse the segment direction for reducing the restrictions on the IC position of an LCD module.

(4-4) Bit Assignment of Display Data

(4-4-1) Bit Assignment Overview

These maps is used for grasping general outlines of the variations in the bit assignment of display data.

Table 9-1 RAM MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	HSW	REF	C256	SEG_0												SEG_1											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
16bit	1	0	x	0	0	X=00H												X=01H											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	0	x	1	0	X=7FH												X=7EH											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	1	x	0	0	X=00H												X=01H											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	1	1	x	1	0	X=7FH												X=7EH											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
8bit	0	0	0	0	0	X=00H							X=01H					X=02H							X=03H				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	0	0	1	0	X=FEH							X=FFH					X=FCH							X=FDH				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	1	0	0	0	X=00H				X=01H								X=02H				X=03H							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	1	0	1	0	X=FEH				X=FFH								X=FCH				X=FDH							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	0	0	X=00H								X=01H								X=02H							
						D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	1	0	X=BEH(L)				X=BFH								X=BDH								X=BEH(H)			
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4

Mode	WLS	ABS	HSW	REF	C256	SEG_{126}												SEG_{127}											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
16bit	1	0	x	0	0	X=7EH												X=7FH											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	0	x	1	0	X=01H												X=00H											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	1	x	0	0	X=7EH												X=7FH											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	1	1	x	1	0	X=01H												X=00H											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
8bit	0	0	0	0	0	X=FCH							X=FDH					X=FEH							X=FFH				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	0	0	1	0	X=02H							X=03H					X=00H							X=01H				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	1	0	0	0	X=FCH				X=FDH								X=FEH				X=FFH							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	1	0	1	0	X=02H				X=03H								X=00H				X=01H							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	0	0	X=BDH								X=BEH								X=BFH							
						D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	1	0	X=01H(L)				X=02H								X=00H								X=01H(H)			
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4

Table 9-2 RAM MAP 2 (Variable 8-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	HSW	REF	C256	SEG_0												SEG_1											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
8 bit	0	x	x	0	1	X=00H												X=01H											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	x	1	1	X=7FH												X=7EH											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Mode	WLS	ABS	HSW	REF	C256	SEG_{126}												SEG_{127}											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
8 bit	0	x	x	0	1	X=7EH												X=7FH											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	x	1	1	X=01H												X=00H											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Table 10 SWAP

SWAP	SWAP	Palette A				Palette B				Palette C			
		A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
0	0	SEGAx				SEGBx				SEGCx			
1	1												
0	1	SEGCx				SEGBx				SEGAx			
1	0												

NOTE1) On the RAM MAP 2, A_0, B_0, C_1 and C_0 bits are fixed to “1”.
NOTE2) The functions of the variable 8-grayscale mode are different from those of the fixed 8-grayscale mode.
NOTE3) The contents of the DDRAM at “C256=0” are not compatible with the contents at “C256=1”.
NOTE4) “C256=1” can be used in the 8-bit bus length mode, but not in the 16-bit bus length mode.

(4-4-2) Bit Assignment in Variable 16-grayscale Mode

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	0	X=00H	←→	X=7FH
*	0	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	1	X=00H	←→	X=7FH
*	0	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	0	X=00H	←→	X=7FH
*	1	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	1	X=00H	←→	X=7FH
*	1	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	0	0	0	X=00H							X=01H					←→	X=FEH							X=FFH							
0	0	1	1	X=FEH							X=FFH					←→	X=00H							X=01H							
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
Grayscale Palette				Palette A				Palette B			Palette C					←→	Palette A				Palette B			Palette C								
Segment Driver				$SEGA_0$				$SEGB_0$			$SEGC_0$					←→	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	0	0	1	X=00H							X=01H					←→	X=FEH							X=FFH							
0	0	1	0	X=FEH							X=FFH					←→	X=00H							X=01H							
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
Grayscale Palette				Palette A				Palette B			Palette C					←→	Palette A				Palette B			Palette C								
Segment Driver				$SEGC_0$				$SEGB_0$			$SEGA_0$					←→	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	1	0	0	X=00H							X=01H					←→	X=FEH							X=FFH							
0	1	1	1	X=FEH							X=FFH					←→	X=00H							X=01H							
Display Data in DDRAM				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
Grayscale Palette				Palette A				Palette B			Palette C					←→	Palette A				Palette B			Palette C								
Segment Driver				$SEGA_0$				$SEGB_0$			$SEGC_0$					←→	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	1	0	1	X=00H							X=01H					←→	X=FEH							X=FFH							
0	1	1	0	X=FEH							X=FFH					←→	X=00H							X=01H							
Display Data in DDRAM				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
Grayscale Palette				Palette A				Palette B			Palette C					←→	Palette A				Palette B			Palette C								
Segment Driver				$SEGC_0$				$SEGB_0$			$SEGA_0$					←→	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

HSW	ABS	REF	SWAP
1	*	0	0

Column Address / Display Data / Segment Driver																																
	X=00H								X=01H								X=02H								..								
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…								
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…								

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP
1	*	0	1

Column Address / Display Data / Segment Driver																																
	X=00H								X=01H								X=02H								..								
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…								
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…								

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	0

Column Address / Display Data / Segment Driver																																
	X=BEH								X=BFH								X=BDH								X=BEH								..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…								
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…								

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H							
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	1

Column Address / Display Data / Segment Driver																																
	X=BEH								X=BFH								X=BDH								X=BEH								..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…								
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…								

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H							
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

(4-4-3) Bit Assignment in Variable 8-level Gradation Mode

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
*	*	0	0	X=00H								←→	X=7FH						
*	*	1	1	X=7FH								←→	X=00H						
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
*	*	0	1	X=00H								←→	X=7FH						
*	*	1	0	X=7FH								←→	X=00H						
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

(4-4-4) Bit Assignment in Fixed 8-level Gradation Mode

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	0	X=00H	←→	X=7FH
*	0	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	1	X=00H	←→	X=7FH
*	0	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	0	X=00H	←→	X=7FH
*	1	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	1	X=00H	←→	X=7FH
*	1	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	0	0	0	X=00H							X=01H				⟷	X=FEH							X=FFH								
0	0	1	1	X=FEH							X=FFH				⟷	X=00H							X=01H								
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	⟷	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
Grayscale Palette				Palette A				Palette B			Palette C				⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGA_0$				$SEGB_0$			$SEGC_0$				⟷	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	0	0	1	X=00H							X=01H				⟷	X=FEH							X=FFH								
0	0	1	0	X=FEH							X=FFH				⟷	X=00H							X=01H								
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	⟷	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
Grayscale Palette				Palette A				Palette B			Palette C				⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGC_0$				$SEGB_0$			$SEGA_0$				⟷	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	1	0	0	X=00H							X=01H				⟷	X=FEH							X=FFH								
0	1	1	1	X=FEH							X=FFH				⟷	X=00H							X=01H								
Display Data in DDRAM				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	⟷	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					
Grayscale Palette				Palette A				Palette B			Palette C				⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGA_0$				$SEGB_0$			$SEGC_0$				⟷	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	1	0	1	X=00H							X=01H				⟷	X=FEH							X=FFH								
0	1	1	0	X=FEH							X=FFH				⟷	X=00H							X=01H								
Display Data in DDRAM				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	⟷	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					
Grayscale Palette				Palette A				Palette B			Palette C				⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGC_0$				$SEGB_0$			$SEGA_0$				⟷	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP
1	*	0	0

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP
1	*	0	1

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	0

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$				

HSW	ABS	REF	SWAP
1	*	1	1

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$				

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	0	X=00H								←→	X=7FH								
*	*	1	1	X=7FH								←→	X=00H								
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C		
Segment Driver				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H								←→	X=7FH								
*	*	1	0	X=7FH								←→	X=00H								
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C		
Segment Driver				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$		

(4-4-5) Bit Assignment in B&W Mode

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	0	0	0	X=00H	⟷	X=7FH				
*	0	1	1	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1	⟷	D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	⟷	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	0	0	1	X=00H	⟷	X=7FH				
*	0	1	0	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1	⟷	D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	⟷	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	1	0	0	X=00H	⟷	X=7FH				
*	1	1	1	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0	⟷	D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	⟷	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	1	0	1	X=00H	⟷	X=7FH				
*	1	1	0	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0	⟷	D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	⟷	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
0	0	0	0	X=00H	X=01H	←→	X=FEH	X=FFH		
0	0	1	1	X=FEH	X=FFH	←→	X=00H	X=01H		
Display Data in DDRAM				D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1	←→	D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1		
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	←→	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
0	0	0	1	X=00H	X=01H	←→	X=FEH	X=FFH		
0	0	1	0	X=FEH	X=FFH	←→	X=00H	X=01H		
Display Data in DDRAM				D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1	←→	D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1		
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	←→	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
0	1	0	0	X=00H	X=01H	←→	X=FEH	X=FFH		
0	1	1	1	X=FEH	X=FFH	←→	X=00H	X=01H		
Display Data in DDRAM				D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0	←→	D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0		
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	←→	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
0	1	0	1	X=00H	X=01H	←→	X=FEH	X=FFH		
0	1	1	0	X=FEH	X=FFH	←→	X=00H	X=01H		
Display Data in DDRAM				D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0	←→	D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0		
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	←→	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

HSW	ABS	REF	SWAP
1	*	0	0

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP
1	*	0	1

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	0

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$				

HSW	ABS	REF	SWAP
1	*	1	1

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$				

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	0	X=00H									←→	X=7FH							
*	*	1	1	X=7FH									←→	X=00H							
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C			←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGA_0$			$SEGB_0$			$SEGC_0$			←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H									←→	X=7FH							
*	*	1	0	X=7FH									←→	X=00H							
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C			←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGC_0$			$SEGB_0$			$SEGA_0$			←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(4-5) Write Data and Read Data

16-bit Bus Length

ABS=0

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓															↓
Read Data	D_{15}	D_{14}	D_{13}	D_{12}	*	D_{10}	D_9	D_8	D_7	*	*	D_4	D_3	D_2	D_1	*

ABS=1

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓															↓
Read Data	*	*	*	*	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

8-bit Bus Length

ABS=0, HSW=0, C256=0 (Column Address: 00H, 02H, …FCH, FEH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	*	D_2	D_1	D_0

ABS=0, HSW=0, C256=0 (Column Address: 01H, 03H, …FDH, FFH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	*	*	D_4	D_3	D_2	D_1	*

ABS=1, HSW=0, C256=0 (Column Address: 00H, 02H, …FCH, FEH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	*	*	*	*	D_3	D_2	D_1	D_0

ABS=1, HSW=0, C256=0 (Column Address: 01H, 03H, …FDH, FFH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ABS=0, HSW=1, C256=0 (Column Address: 00H, 01H, …BEH, BFH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ABS=0, HSW=0, C256=1 (Column Address: 00H, 01H, …7EH, 7FH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

NOTE) * : Invalid Data

(5) GRAYSCALE CONTROL CIRCUIT

(5-1) Display Mode Selection

A display mode is selected by the combination of the D_2 (MON) bit of the "Display Control (1)" instruction and the D_3 (PWM) and D_2 (C256) bits of the "Display Mode Control" instruction, as shown below.

Table 11 Display Mode Selection

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f_{OSC1}
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f_{OSC2}
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f_{OSC3}
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, "C256" bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256="0" (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256="1" (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the "C256" bit is usually "1". For more information how the display data is assigned, refer to "(4-4) Bit Assignment of Display Data".

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the "Frequency Control" Instruction. Refer to "(10) OSCILLATOR" and "OSCILLATION FREQUENCY AND FRAME FREQUENCY".

(5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes Aj, Bj and Cj (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEGAi, SEGBi and SEGCi (i=0 to 127) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

(5-1-2) Variable 8-grayscale Mode

Each of the palettes Aj, Bj and Cj (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEGAi, SEGBi and SEGCi (i=0 to 127)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

(5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes Aj, Bj and Cj (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEGAi, SEGBi and SEGCi (i=0 to 127)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

(5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.

(6) GRAYSCALE PALETTE

(6-1) Grayscale Selection in Variable 16-grayscale Mode

Table 12-1 Grayscale selection

(Palette Aj, Bj, and Cj)

Display Data MSB----LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

Table 12-2 Grayscale Palette

(Palette Aj, Bj, and Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) “MON=0”, “PWM=0”, “C256=0”
NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

(6-2) Grayscale Selection in Variable 8-grayscale Mode

Table 13-1 Grayscale selection

(Palette Aj and Bj)

Display Data MSB----LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

Table 13-2 Grayscale Palette

(Palette Aj and Bj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) “MON=0”, “PWM=0”, “C256=1”.
NOTE2) Applied to palette Aj and Bj (j=0 to 15)
NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

Table 13-3 Grayscale selection

(Palette Cj)

Display Data MSB----LSB	Palette Name
0 0 * *	Palette A3/B3/C3
0 1 * *	Palette A7/B7/C7
1 0 * *	Palette A11/B11/C11
1 1 * *	Palette A15/B15/C15

Table 13-4 Grayscale Palette

(Palette Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) “MON=0”, “PWM=0”, “C256=1”
NOTE2) Applied to palette Cj (j=0 to 15)
NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

(6-3) Grayscale Selection in Fixed 8-grayscale Mode

Table 14-1 Grayscale Selection

(Palette Aj and Bj)

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

Table 14-2 Grayscale Palette

(Palette Cj)

Display Data MSB- - - -LSB	Grayscale
0 0 * *	0/7
0 1 * *	3/7
1 0 * *	5/7
1 1 * *	7/7

NOTE1) “MON=0”, “PWM=1”, “C256=0 or 1”

(6-4) Grayscale Selection in B&W Mode

Table 15 Grayscale Selection

Display Data MSB- - - -LSB	Grayscale
0 * * *	0
1 * * *	1

NOTE1) “MON=1”, “PWM=0 or 1” and “C256=0 or 1”

(7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting "1" at the D_0 (SON) bit of the "Duty-1 /Display Clock ON/OFF" instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers Ai, Bi and Ci (i=0 to 127) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes "H".

(8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The "All Pixels ON/OFF", "Display ON/OFF" and "Reverse Display ON/OFF" instructions control the data in this circuit, but does not change the data in the DDRAM.

(9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 162-common drivers and 384-segment drivers. The common drivers generate LCD driving waveforms formed on the V_{LCD}, V_1, V_4 and V_{SSH} levels. The segment drivers generate waveforms formed on the V_{LCD}, V_2, V_3 and V_{SSH} levels.

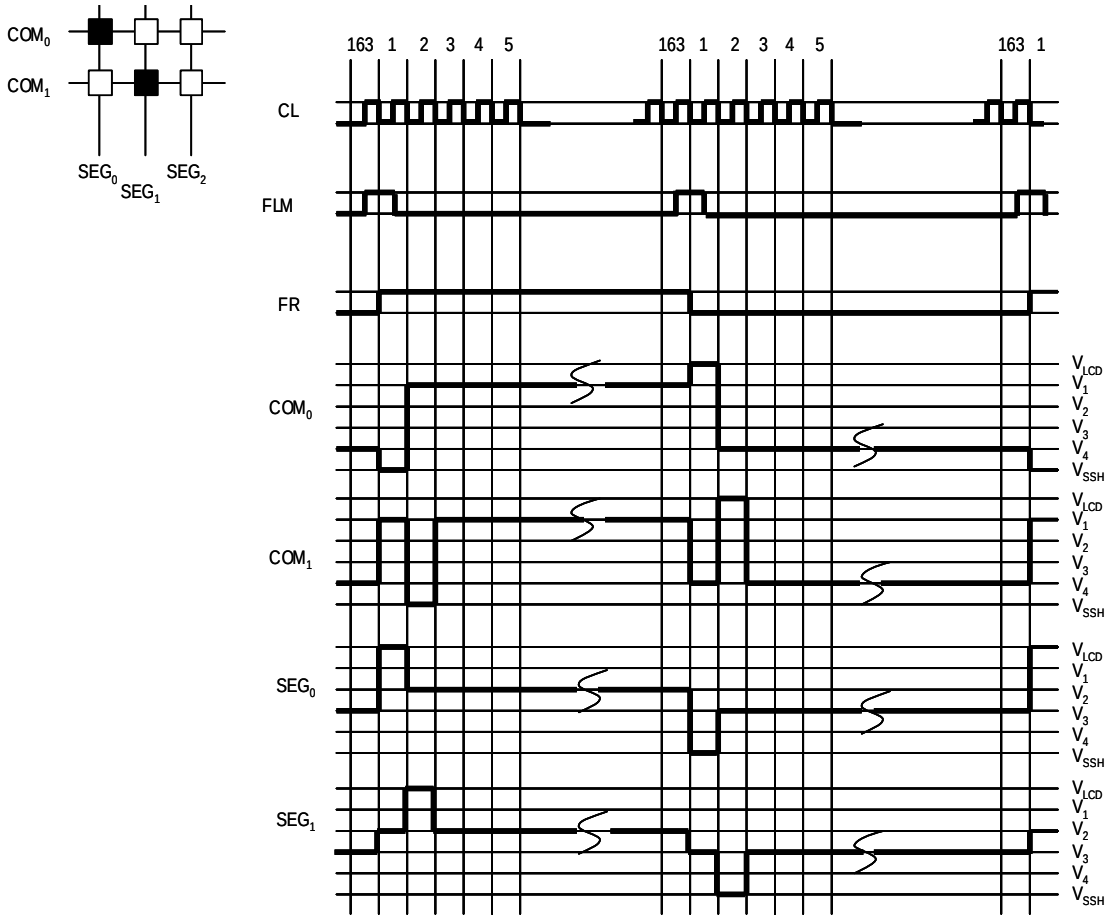


Fig 8 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/163 Duty)

(10) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting "0" at the D_1 (CKS) bit of the "Bus Length" instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D_2-D_0 (RF2-RF0) bits of the "Frequency Control" instruction. For more safety, make sure what is the best frequency in the particular application.

(10-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at "H" or "L" and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

Table 16 Oscillation Frequency vs. Display Mode

Symbol	MON	PWM	Display Mode
f_{OSC1}	0	0	Variable 8-/16-grayscale Mode
f_{OSC2}	0	1	Fixed 8-grayscale Mode
f_{OSC3}	1	*	B&W Mode

*: Don't care

(10-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

(10-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

(11) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D_3 (AMPON) and D_1 (DCON) bits of the "Power Control" instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 17.

Table 17 Configuration of LCD Power Supply

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4	1, 3, 4
0	1	Inactive	Active	V_{OUT}	2, 3, 4
1	1	Active	Active	–	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C_{1+}, C_{1-}, C_{2+}, C_{2-}, C_{3+}, C_{3-}, C_{4+}, C_{4-}, C_{5+}, C_{5-}, C_{6+}, C_{6-}, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) Only the voltage converter is used. The V_{OUT} is externally supplied, and the C_{1+}, C_{1-}, C_{2+}, C_{2-}, C_{3+}, C_{3-}, C_{4+}, C_{4-}, C_{5+}, C_{5-}, C_{6+}, C_{6-}, and V_{EE} are open. The reference voltage is supplied on the V_{REF}.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

(11-1) Voltage Booster

The internal voltage booster generates up to $7xV_{EE}$ voltage. The boost level is selected from 2x, 3x, 4x, 5x, 6xor7x by setting the D_2-D_0 (VU2-VU0) bits of the "Boost Level" instruction. The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

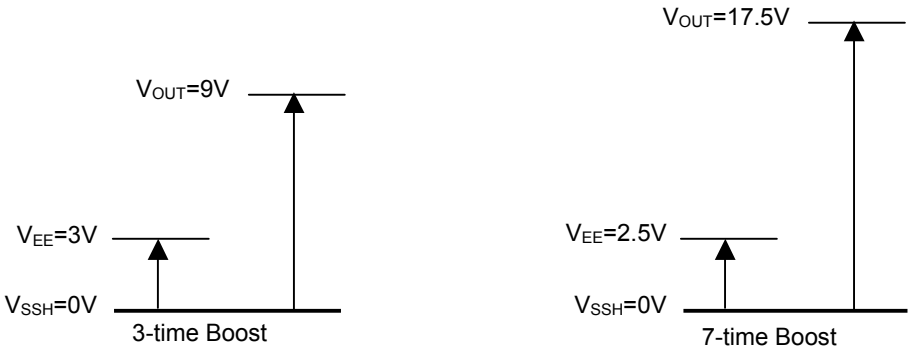


Fig 9 Boost Voltage

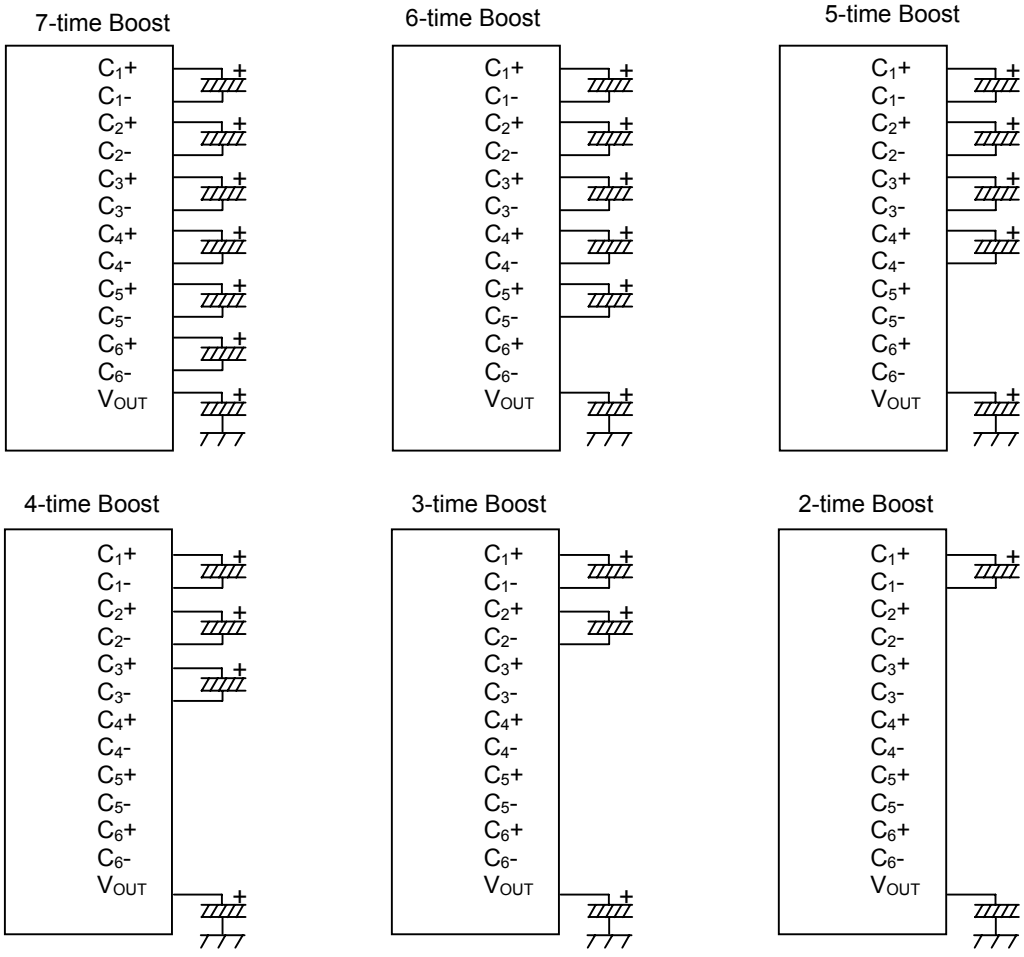


Fig 10 External Capacitor Connection of Voltage Booster

(11-2) Voltage Converter

(11-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage (V_{BA}=0.9xV_{EE}). When using the internal LCD power supply, connect the V_{BA} and the V_{REF}, or supply 0.9xV_{EE} or lower voltage on the V_{REF}. When using an external LCD power supply, the V_{BA} should be open.

(11-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and its multiple (boost level) is set by the D_2-D_0 (VU2-VU0) bits of the "Boost Level" instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \qquad \text{(N: Boost Level)}$$

(11-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the V_{LCD} voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D_2-D_0 (DV_2-DV0) bits of the "EVR Control" instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \qquad \text{(M: EVR Value)}$$

(11-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the V_{LCD}, V_1, V_2, V_3 and V_4, and its bias ratio is selected from1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 or 1/12.

As shown in Fig 11, when using only the internal LCD power supply, the capacitors CA2 are connected to the V_{LCD}, V_1, V_2, V_3 and V_4 respectively.

As shown in Fig 12, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the V_{LCD}, V_1, V_2, V_3 and V_4, and the internal LCD power supply should be turned off by setting "0" at the "DCON" and "AMPON" bits. And the C_{1+}, C_1-, C_{2+}, C_{2-}, C_{3+}, C_3-, C_{4+}, C_4-, C_{5+}, C_5-, C_{6+}, C_6-, V_{EE}, V_{REF} and V_{REG} are open.

Fig 13 and 14 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 15 shows the circuit when partially using the LCD power supply without the voltage booster.

(11-3) External Components for LCD Power Supply

Using Only Internal LCD Power Supply (7x boost)

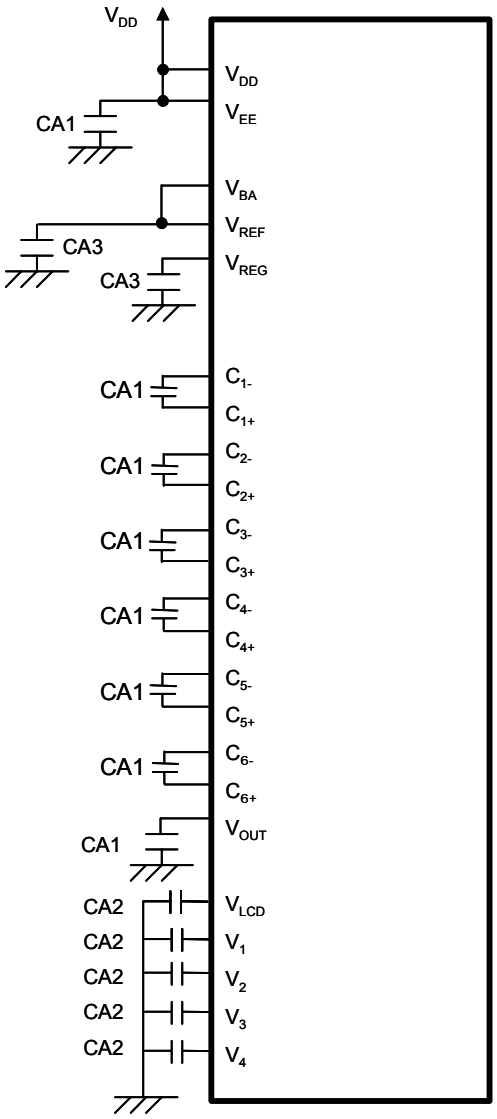


Fig 11

Using Only External LCD Power Supply

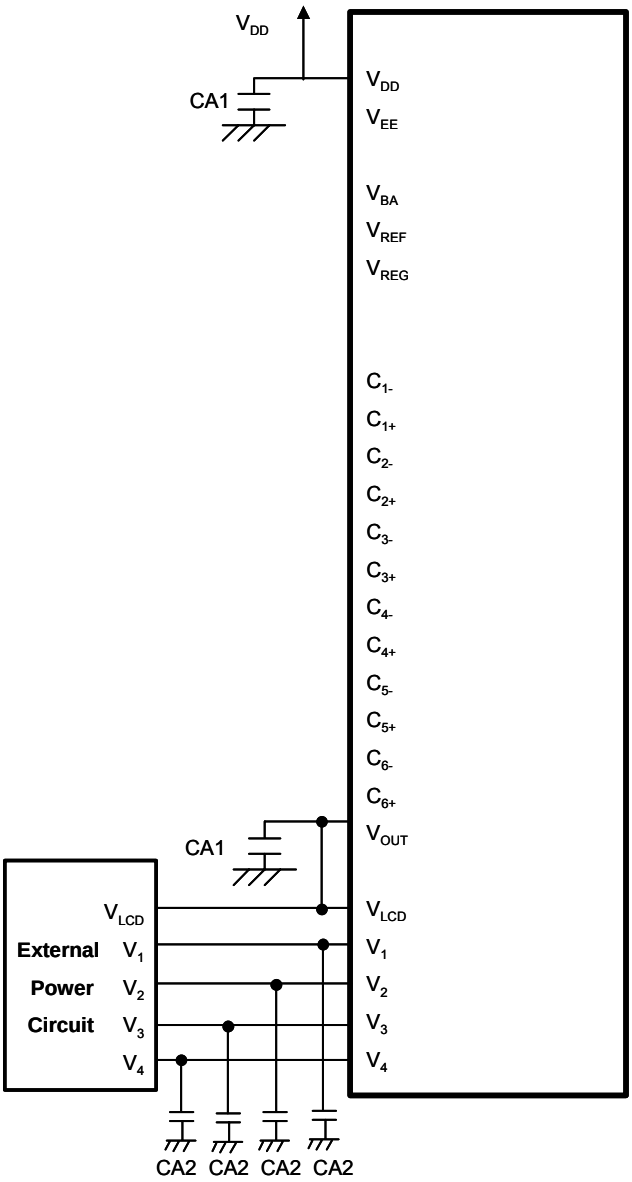


Fig 12

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply
Without Reference Voltage generator (1)
(7x boost)

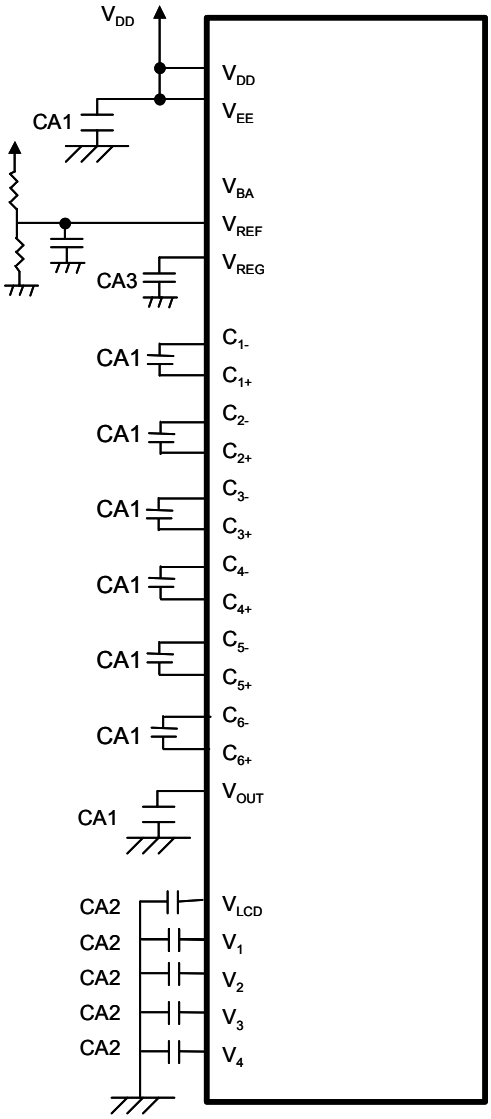


Fig 13

Using Internal LCD Power Supply
Without Reference Voltage generator (2)
(7x boost)

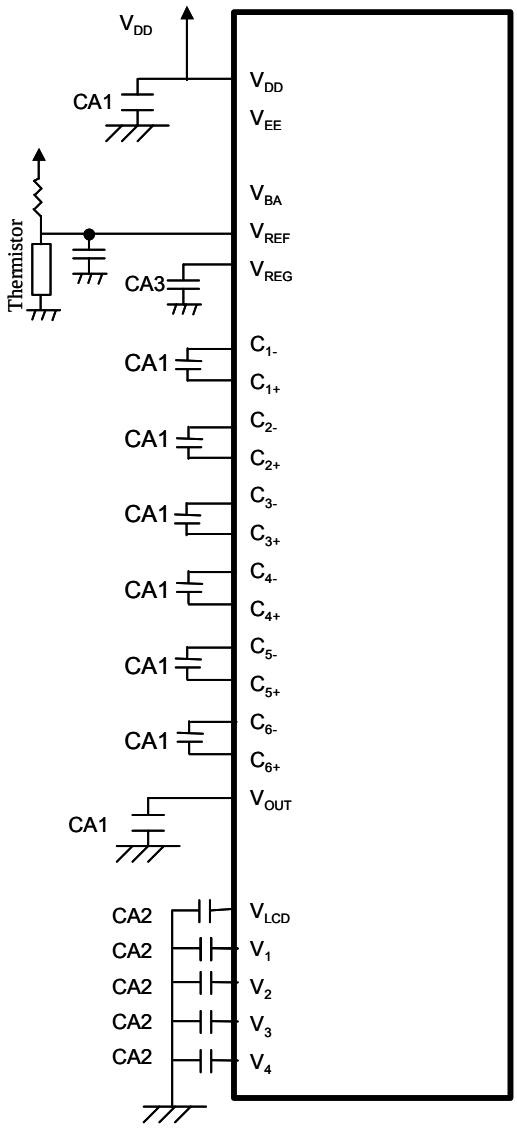


Fig 14

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply
Without Voltage Booster

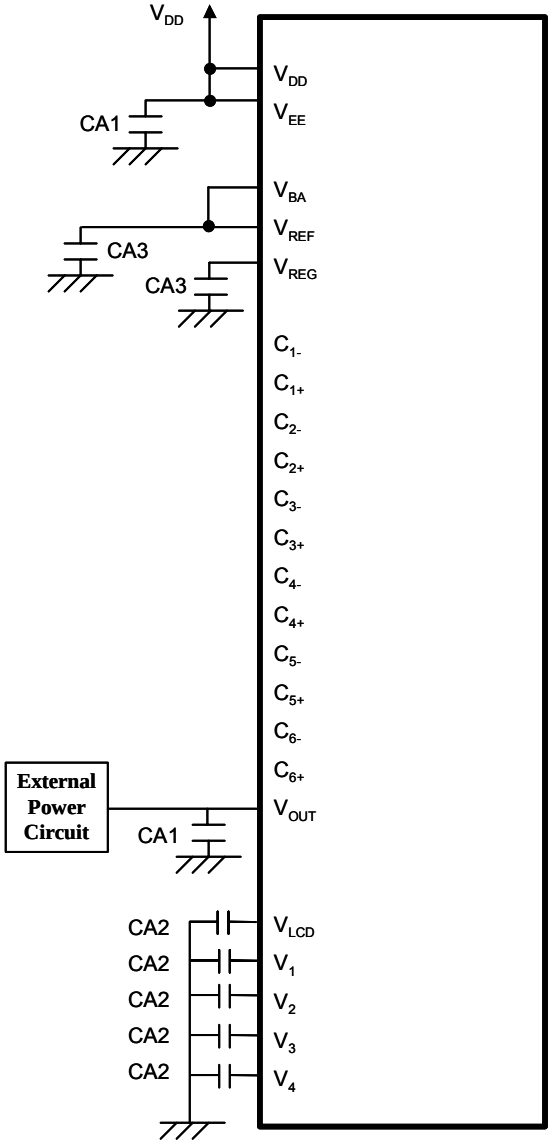


Fig 15

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(11-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the V_{LCD} and V_1-V_4 and for the V_{OUT}. The V_{LCD} and V_1-V_4 are discharged by setting "1" at the D_0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to “(14-22) Discharge ON/OFF”.

(11-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to “(18) TYPICAL INSTRUCTION SEQUENCES”.

(11-5-1) Power ON/OFF in Using Internal LCD Power Supply

Power ON

First “V_{DD} and V_{EE} ON”, next “Reset by RESb”, then “Internal LCD power supply ON”. Be sure to execute the “Display ON” instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First “Reset by RESb or “HALT” instruction”, next “V_{DD} and V_{EE} OFF”. If using different power sources for the V_{DD} and the V_{EE} individually, the V_{EE} must be turned off after the reset or the “HALT”. After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_{LCD}, V_1, V_2, V_3 and V_4) drop below the threshold level of LCD pixels.

(11-5-2) Power ON/OFF in Using External LCD Power Supply

Power ON

First “V_{DD} and V_{EE} ON”, next “Reset by RESb”, then “External LCD power supply ON”. When using only external V_{OUT}, first “V_{DD} ON”, next “Reset by RESb”, then “External V_{OUT} ON”, as well.

Power OFF

First “Reset by RESb or “HALT” instruction” to isolate external LCD bias voltages, next “V_{DD} OFF”. For more safety, placing a resistor in series on the V_{LCD} line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50Ω and 100Ω.

(12) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to “L”. Connecting the RESb with MPU’s reset is recommended so that the LSI and MPU is initialized at a time.

Default Status

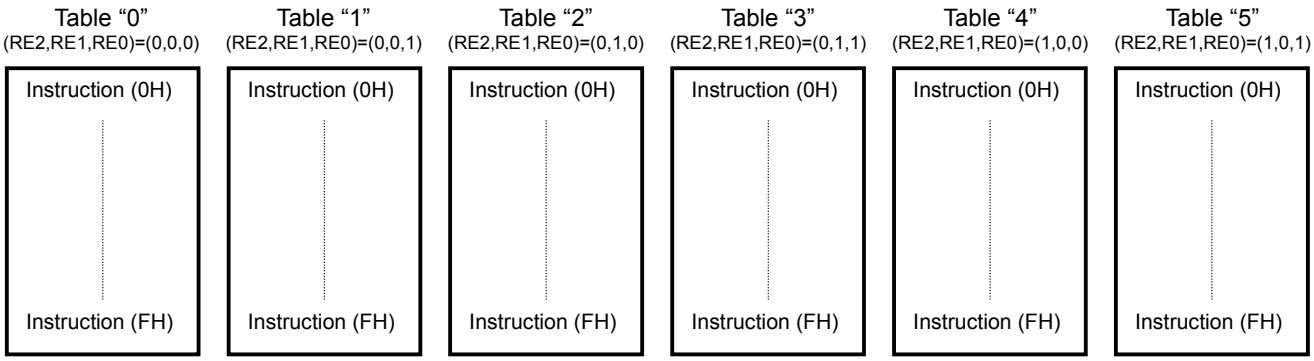
1. Display Data in DDRAM :Undefined
2. Column Address :(00)H
3. Row Address :(00)H
4. Initial Display Line :(0)H (1st line)
5. Display ON/OFF :OFF
6. Reverse Display ON/OFF :OFF (Normal)
7. Duty Cycle Ratio :1/163 Duty (DSE=0)
8. N-line Inversion ON/OFF :OFF
9. COM Scan Direction :$COM_0 \rightarrow COM_{161}$
10. Increment Control :Auto-increment OFF (AIM, AXI, AYI)=(0, 0, 0)
11. REF :REF=0 (Normal)
12. Swap :OFF (Normal)
13. EVR Value :(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply :OFF
15. Display Mode :Grayscale Mode
16. LCD Bias Ratio :1/9 Bias
17. Palette 0 :(0, 0, 0, 0, 0)
18. Palette 1 :(0, 0, 0, 1, 1)
19. Palette 2 :(0, 0, 1, 0, 1)
20. Palette 3 :(0, 0, 1, 1, 1)
21. Palette 4 :(0, 1, 0, 0, 1)
22. Palette 5 :(0, 1, 0, 1, 1)
23. Palette 6 :(0, 1, 1, 0, 1)
24. Palette 7 :(0, 1, 1, 1, 1)
25. Palette 8 :(1, 0, 0, 0, 1)
26. Palette 9 :(1, 0, 0, 1, 1)
27. Palette 10 :(1, 0, 1, 0, 1)
28. Palette 11 :(1, 0, 1, 1, 1)
29. Palette 12 :(1, 1, 0, 0, 1)
30. Palette 13 :(1, 1, 0, 1, 1)
31. Palette 14 :(1, 1, 1, 0, 1)
32. Palette 15 :(1, 1, 1, 1, 1)
33. Display Mode Control :Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length :8-bit Bus Length
35. Discharge ON/OFF :OFF (DIS)=(0)

(13) INSTRUCTION TABLES

(13-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 16, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 17 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 16 Instruction Table Overview

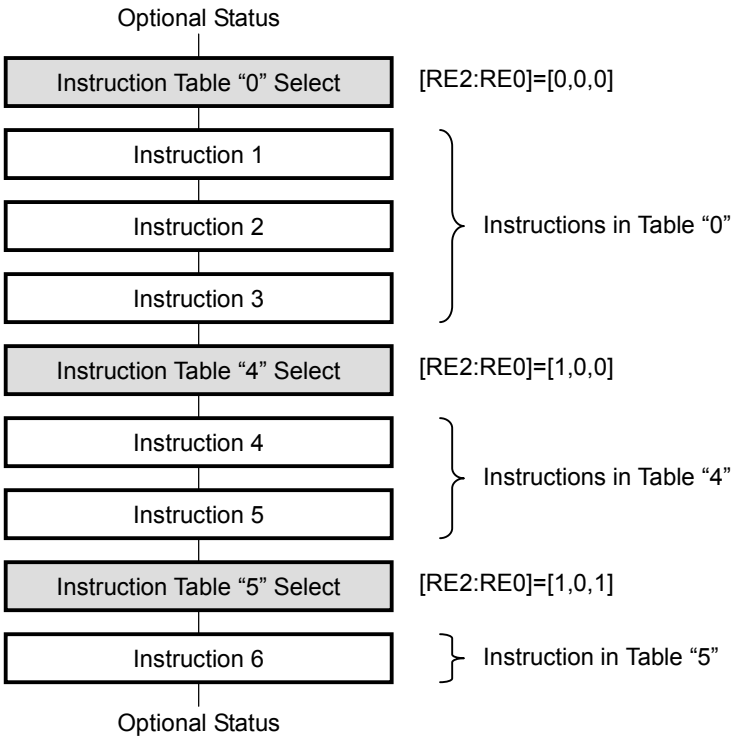


Fig 17 Outline of Instruction Sequence

(13-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

	Instructions/ Register Address [NH]	Code (80 Series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data
3	Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point
	Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point
4	Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point
	Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	Setting Row Address for start point
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	LA7	LA6	LA5	LA4	Setting Row Address for Initial COM
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	N7	N6	N5	N4	Setting the Number of N-line Inversion
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF REF : Segment Direction
9	Increment Control [AH]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN : Window Area ON/OFF AIM : Read-Modify-Write ON/OFF AYI : Row Increment AXI : Column Increment
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio
12	Boost Level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	VU2-0 : Setting Boost Level
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
	Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)
	Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)
	Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)
	Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PG84	Setting Palette Data : B0(PS=0) /B8(PS=1)
	Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)
	Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)
	Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)
	Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)
	Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)
	Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)
	Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)
	Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)
	Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)
	Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
	Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Setting Palette Data : C4(PS=0) /C12(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
	Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16	Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17	Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18	Display Mode Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : Variable/Fixed Grayscale Mode C256 : 256-color Mode ON/OFF. FDC : Boost clock
19	Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High Speed Writing ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20	EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
	EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21	Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22	Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	Discharge ON/OFF
23	Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24	Register Read	0	1	0	1	0/1	0/1	0/1					Read Data				Reading Instruction
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Upper/Lower Palette Register
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWM S	PWM A	PWM B	PWM C	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

(14-1) Display Data Write

The "Display Data Write" instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display Data							

(14-2) Display Data Read

The "Display Data Read" instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display Data							

(14-3) Column Address

The "Column Address" instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

(14-4) Row Address

The "Row Address" instruction specifies the row address of the start point. Available setting range is from (00H) to (A1H), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	AY7	AY6	AY5	AY4

(Default: AY7-AY4=0H / Register Address: 3H)

(14-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to "(14-16) Initial COM". The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	LA7	LA6	LA5	LA4

(Default: LA7-LA4=0H / Register Address: 5H)

Table 18 Initial Display Line Address

LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	Row Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	1	0	0	0	0	1	161

(14-6) N-line Inversion

The number of N line is selected in between "2" and "162". When the N-line inversion is enabled by setting "1" at the D_2 (NLIN) bit of the "Display Control (2)" instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting "0" at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	N7	N6	N5	N4

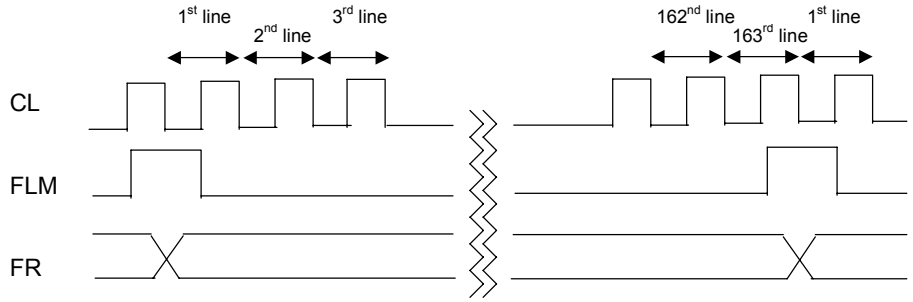
(Default: N7-N4=0H / Register Address: 7H)

Table 19 N-line Inversion

N7	N6	N5	N4	N3	N2	N1	N0	N Line
0	0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	0	1	2
				:				:
1	0	1	0	0	0	0	1	162

NOTE1) N Line=(N Value)+1

N-line inversion OFF



N-line inversion ON

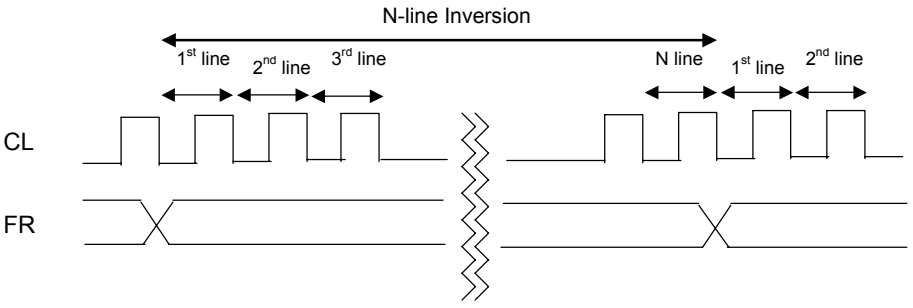


Fig 18 N-line Inversion Timing (1/163 Duty)

(14-7) Display Control (1)

The “Display Control (1)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

D_0 (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V_{SSH} level)
ON/OFF=1 : Display ON

D_1 (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the “REV” bit of the “Display Control (2)” instruction.

ALLON=0 : Normal
ALLON=1 : All pixels ON

D_2 (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)
MON=1 : B&W Mode

D_3 (SHIFT)

SHIFT=0 : $COM_0 \rightarrow COM_{161}$
SHIFT=1 : $COM_0 \leftarrow COM_{161}$

(14-8) Display Control (2)

The "Display Control (2)" instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

(Default: [REV,NLIN,SWAP,REF]=0H / Register Address: 9H)

D_0 (REF)

This bit controls the DDRAM access direction which reverses the segment direction for reducing the restrictions on the IC position of an LCD module. For more information, refer to "(17) SWAP FUNCTION".

D_1 (SWAP)

This bit swaps palettes Aj and palettes Cj (j=0-15). This function reduces the restrictions on the IC position of an LCD module. Refer to "(16) SWAP FUNCTION".

SWAP=0 : SWAP OFF
SWAP=1 : SWAP ON

D_2 (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)
NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

D_3 (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)
REV=1 : Reverse Display ON

Table 20 Reverse Display ON/OFF

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(14-9) Increment Control

The "AIM", "AYI" and "AXI" bits set an auto-increment operation to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. The "WIN" bits enables/disables the window area access.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	WIN	AIM	AYI	AXI

(Default: [WIN,AIM,AYI,AXI]=0H / Register Address: AH)

D_2 (AIM)

Table 21 Read-modify-write ON/OFF

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

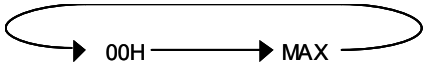
NOTE1) Increment in writing and reading display data
NOTE2) Increment in writing display data only

D_1, D_0 (AYI, AXI)

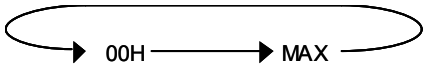
Table 22 Column/Row Increment

AYI	AXI	Column/Row Increment	NOTE
0	0	Non Increment	1
0	1	Column Address Increment	2
1	0	Row Address Increment	3
1	1	Column & Row Addresses Increment	4

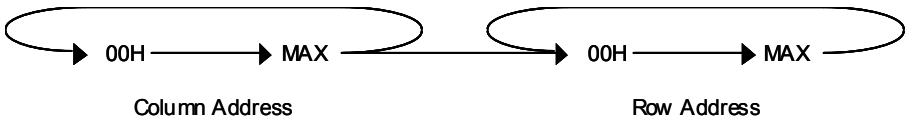
NOTE1) Non increment. The "AIM" bit is disabled.
NOTE2) Increment operation of column address. The "AIM" bit is enabled.



NOTE3) Row address increment. The "AIM" bit is enabled.



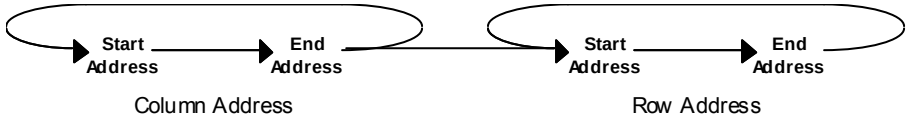
NOTE4) Column & row addresses increment. The "AIM" bit is enabled.



D_3 (WIN)

The window access should be enabled (WIN=1) in combination with the auto-increment operation (AXI=1, AYI=1). The typical sequence of the window area setting is discussed in "(4-2) Window Area for DDRAM Access".

WIN=0 : Window Area Access OFF (Normal DDRAM Access)
WIN=1 : Window Area Access ON



(14-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

D_0 (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)
ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

D_1 (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF
DCON=1 : Voltage Booster ON

D_2 (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)
HALT=1 : Power Save ON

Internal State in Power Save Mode (HALT="1")
- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V_{SSH} level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V_{LCD}, V_1, V_2, V_3 and V_4 are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

D_3 (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF
AMPON=1 : Voltage Converter ON

(14-11) Duty Cycle Ratio

The "Duty Cycle Ratio" instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the "Boost Level", the "LCD Bias Ratio" and the "EVR Control".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

Table 23 Duty Cycle Ratio

DS3	DS2	DS1	DS0	Duty Cycle Ratio		# of Commons
				DSE=0	DES=1	
0	0	0	0	1/163	1/162	162 commons
0	0	0	1	1/161	1/160	160 commons
0	0	1	0	1/145	1/144	144 commons
0	0	1	1	1/133	1/132	132 commons
0	1	0	0	1/129	1/128	128 commons
0	1	0	1	1/113	1/112	112 commons
0	1	1	0	1/97	1/96	96 commons
0	1	1	1	1/81	1/80	80 commons
1	0	0	0	1/73	1/72	72 commons
1	0	0	1	1/65	1/64	64 commons
1	0	1	0	1/57	1/56	56 commons
1	0	1	1	1/49	1/48	48 commons
1	1	0	0	1/41	1/40	40 commons
1	1	0	1	1/33	1/32	32 commons
1	1	1	0	1/25	1/24	24 commons
1	1	1	1	1/17	1/16	16 commons

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting "1" at the D_1 (DSE) bit of the "Duty-1 ON/OFF" instruction. Refer to "(14-17) Duty-1 /Display Clock ON/OFF".

(14-12) Boost Level

The "Boost Level" selects the multiple of the voltage booster.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU2	VU1	VU0

(Default:VU2-VU0=0H / Register Address: DH)

D_2, D_1, D_0 (VU2, VU1, VU0)

Table 24 Boost Level

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	6 times
1	1	0	7 times
1	1	1	Inhibited

.

(14-13) LCD Bias Ratio

The “LCD bias ratio” selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

Table 25 LCD Bias Ratio

B2	B1	B0	LCD Bias Ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(14-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

Table 26 Instruction Table Select

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) “TST0” bit must be “0”. This is used for maker tests only.

(14-15) Palette A / B / C

Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in "(6) GRAYSCALE PALETTE" for default setting.

Palette A5 (PS=0) / Palette A13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

Palette A6 (PS=0) / Palette A14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

Palette A7 (PS=0) / Palette A15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B5 (PS=0) / Palette B13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

Palette B6 (PS=0) / Palette B14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

Palette B7 (PS=0) / Palette B15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C5 (PS=0) / Palette C13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

Palette C6 (PS=0) / Palette C14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

Palette C7 (PS=0) / Palette C15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

(14-16) Initial COM

The "Initial COM" instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

Table 27 Initial COM

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM_0	COM_{161}
0	0	0	1	COM_1	COM_{160}
0	0	1	0	COM_9	COM_{152}
0	0	1	1	COM_{14}	COM_{146}
0	1	0	0	COM_{17}	COM_{144}
0	1	0	1	COM_{25}	COM_{136}
0	1	1	0	COM_{33}	COM_{128}
0	1	1	1	COM_{41}	COM_{120}
1	0	0	0	COM_{49}	COM_{112}
1	0	0	1	COM_{57}	COM_{104}
1	0	1	0	COM_{65}	COM_{96}
1	0	1	1	COM_{73}	COM_{88}
1	1	0	0	COM_{122}	COM_{39}
1	1	0	1	COM_{130}	COM_{31}
1	1	1	0	COM_{138}	COM_{23}
1	1	1	1	COM_{146}	COM_{15}

(14-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

D_0 (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at "L" level.
SON=1 : CL, FLM, FR, and CLK are enabled.

D_1 (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting "1" at the "DSE" bit.

DSE=0 : OFF (Duty-0)
DSE=1 : ON (Duty-1)

NOTE) For the last common timing at "DSE=0", all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/163 duty cycle, the segment waveforms for 163rd common timing are the same as for 162nd common timing (last line).

(14-18) Display Mode Control

The "Display Mode Control" instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D_2 (MON) bit of the "Display Control (1)" is used in combination. Refer to "(5) GRAY SCALE CONTROL CIRCUIT" and "(14-7) Display Control (1)."

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	C256	FDC1	FDC2

(Default: PWM,C256=0H / Register Address: 8H)

D_3 (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)
PWM=1 : Fixed 8-grayscale Mode

D_2 (C256)

C256=0 : Variable 16-grayscale Mode at "PWM=0" (4096 colors)
C256=1 : Variable 8-grayscale Mode at "PWM=0" (256 colors)

D_1(FDC1), D_0(FDC2)

These bits are used to select clock multiply for voltage booster.

FDC1	FDC2	Boost Clock
0	0	×1
0	1	×2
1	0	×4
1	1	×1/2

(14-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration, ABS mode ON/OFF and high speed writing ON/OFF as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	HSW	ABS	CKS	WLS

(Default: HSW,ABS,CKS,WLS=0H / Register Address: 9H)

D_0 (WLS)

WLS=0: 8-bit Bus Length
WLS=1: 16-bit Bus Length

D_1 (CKS)

CKS =0: Internal Oscillator using an internal resistor
CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to "(10) OSCILLATOR".

D_2 (ABS)

ABS=0: ABS Mode OFF (Normal)
ABS=1: ABS Mode ON

D_3 (HSW)

HSW=0: High Speed Writing OFF (Normal)
HSW=1: High Speed Writing ON

(14-20) EVR Control

The "EVR Control" instruction adjusts V_{LCD} to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V_{LCD}. The setting order is upper byte first, then lower byte. Refer to "(11-2-3) Electrical Variable Resistor (EVR)".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV0

(Default: DV_3-DV0=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV6	DV_5	DV_4

(Default: DV6-DV_4=0H / Register Address: BH)

Table 28 EVR Control

DV6	DV_5	DV_4	DV_3	DV_2	DV_1	DV0	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

Formula of VLCD

VLCD [V] = 0.5x VREG + M (VREG – 0.5x VREG) / 127

VBA = VEE x 0.9
VREG = VREF x N

VBA : Output of the reference voltage generator
VREF : Input of the voltage regulator
VREG : Output of the voltage regulator
N : Boost level
M : EVR Value

(14-21) Frequency Control

The "Frequency Control" instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV_3-DV0=0H / Register Address: DH)

Table 29 Frequency Control

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(14-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V_{LCD}, V_1, V_2, V_3,V_4 and V_{OUT}. Refer to "(11-4) Discharge Circuit".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	*	DIS

(Default: DIS2,DIS1=0H / Register Address: EH)

D_0 (DIS)

DIS=0 : Discharge OFF
DIS=1 : Discharge ON (Discharge from V_{LCD}, V_1, V_2, V_3 and V_4)

NOTE) Resistance is 100KΩ typical.

(14-23) Register Address

The "Register Address" instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

(14-24) Register Read

The "Register Read" instruction reads out instruction data from the register which address is specified by the "Register Address" instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data			

(14-25) Window End Column Address

The "Window End Column Address" instruction specifies the column address of the end point. Refer to "(4-2) Window Area for DDRAM Access". The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

(14-26) Window End Row Address

The "Window End Row Address" instruction specifies the row address of the end point. Refer to "(4-2) Window Area for DDRAM Access". The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	EY7	EY6	EY5	EY4

(Default: EY7-EY4=0H / Register Address: 3H)

(14-27) Initial Line-reverse Address

The "Initial Line-reverse Address" instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	LS7	LS6	LS5	LS4

(Default: LS7-LS4=0H / Register Address: 5H)

(14-28) Last Line-reverse Address

The "Last Line-reverse Address" instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	LE7	LE6	LE5	LE4

(Default: LE7-LE4=0H / Register Address: 7H)

(14-29) Line Reverse ON/OFF

The "Line Reverse ON/OFF" instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D_3 (REV) bit of the "Display Control (2)" instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

D_0 (LREV)

LREV =0 : Line Reverse OFF (Normal)
LREV =1 : Line Reverse ON

D_1 (BT)

BT =0 : No Blink
BT =1 : Blink once every 32 frames

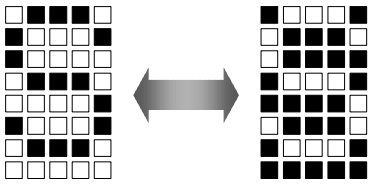


Fig 19 On-screen Image in Using Line-reverse Display and Blink Function

(14-30) Upper/Lower Palette Select

The "Upper/Lower Palette Select" instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PS

(Default: PS=0 / Register Address: 9H)

D_0 (PS)

PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, …, PC74)
PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, …, PC154)

(14-31) PWM Control

The "PWM control" instruction selects PWM type, as shown in Fig 20.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

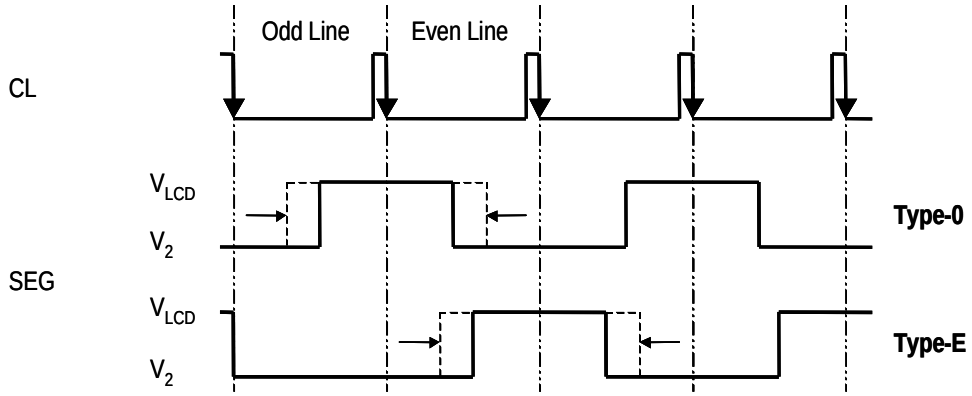
D_3 (PWMS)

PWMS=0 : Type 1
PWMS=1 : Type 2

D_2 (PWMA), D_1 (PWMB), D_0 (PWMC)

PWMZ=0 (Z=A, B and C): Type 1-O
PWMZ=1 (Z=A, B and C): Type 1-E

PWM Type 1 (PWMS=0)



PWM Type 2 (PWMS=1)

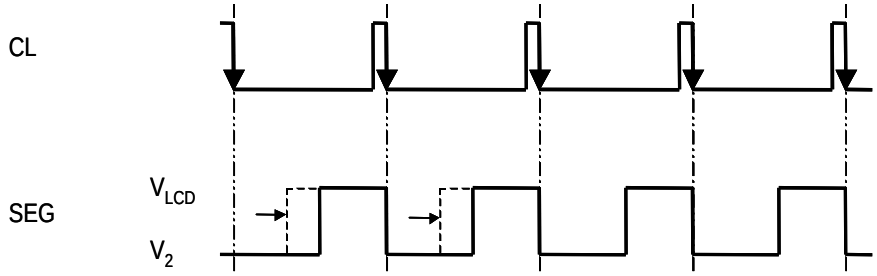


Fig 20 PWM Control

(15) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(14-11) Duty Cycle Ratio”, “(14-12) Boost Level”, “(14-13) LCD Bias Ratio” and “(14-20) EVR Control”. Typical setting sequence is shown in “(18-4) Partial Display Sequence”.

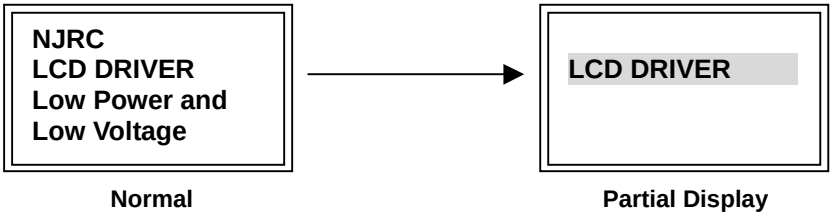


Fig 21 On-screen Image in Using Partial Display Function

(16) SWAP FUNCTION

The swap function switches the palettes Aj and the palettes Cj (j=0-15), and is controlled by the D_1 (SWAP) bit of the "Display Control (2)" instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 22 "Overview of Swap Function" illustrates general outlines of internal operations, and (16-1-1) through (16-1-4) show each configuration on a mode-by-mode basis.

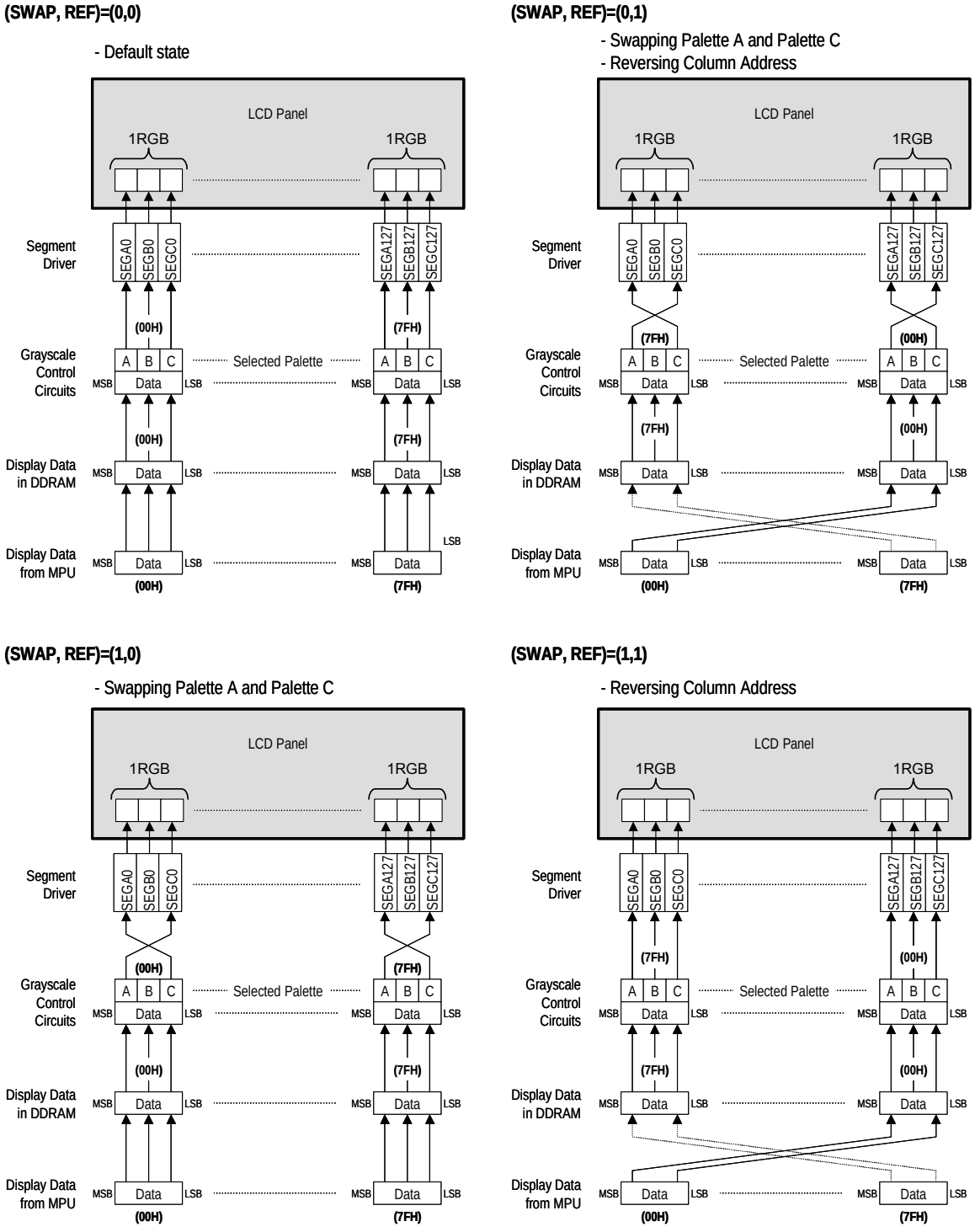
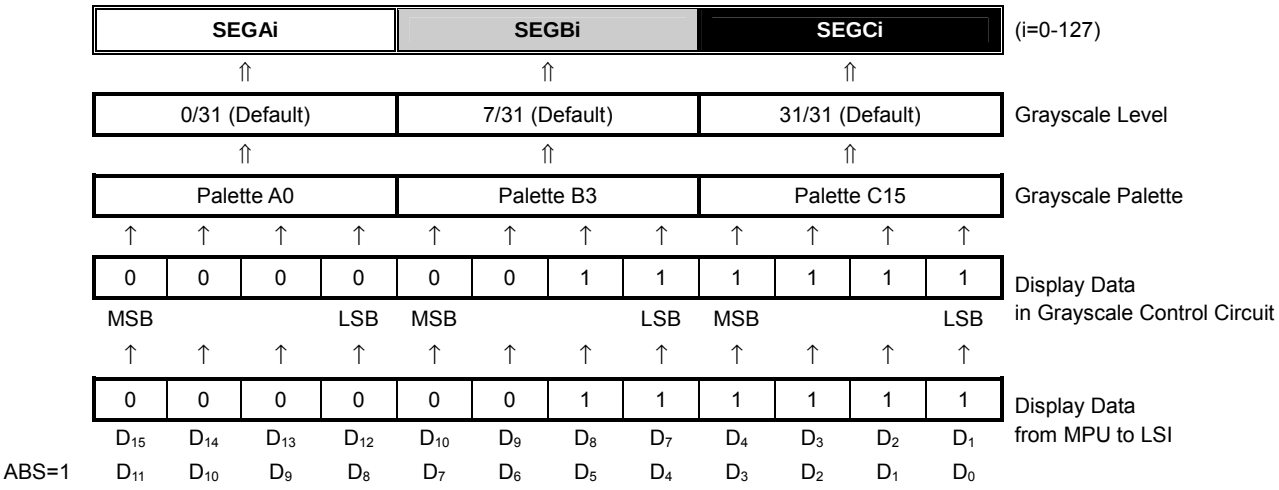


Fig 22 Overview of SWAP Function

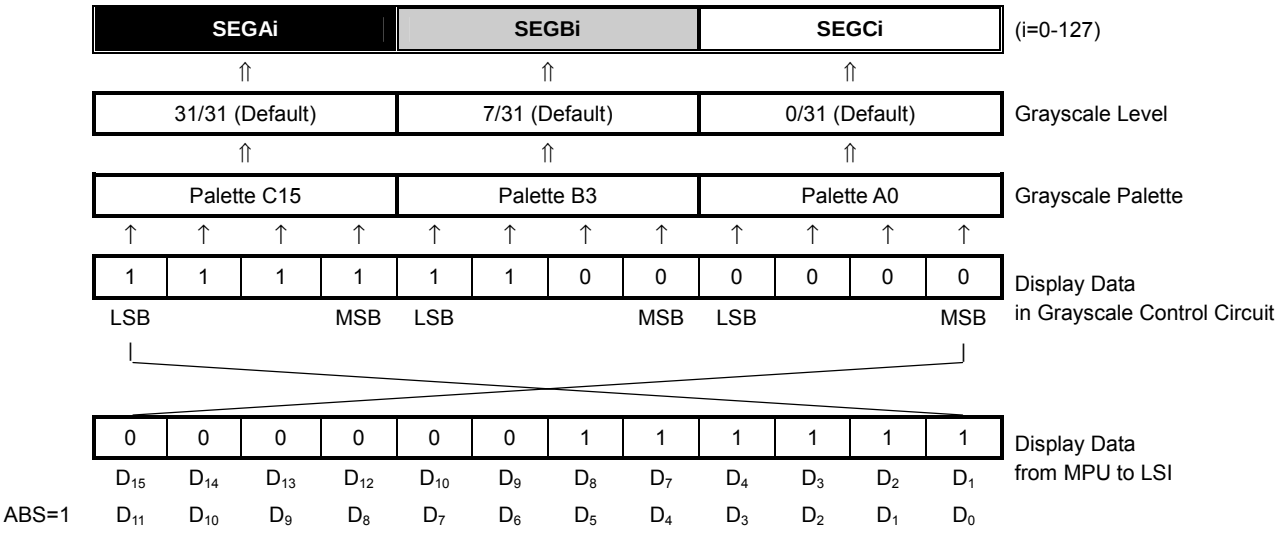
(16-1) Swap Function in Variable 16-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



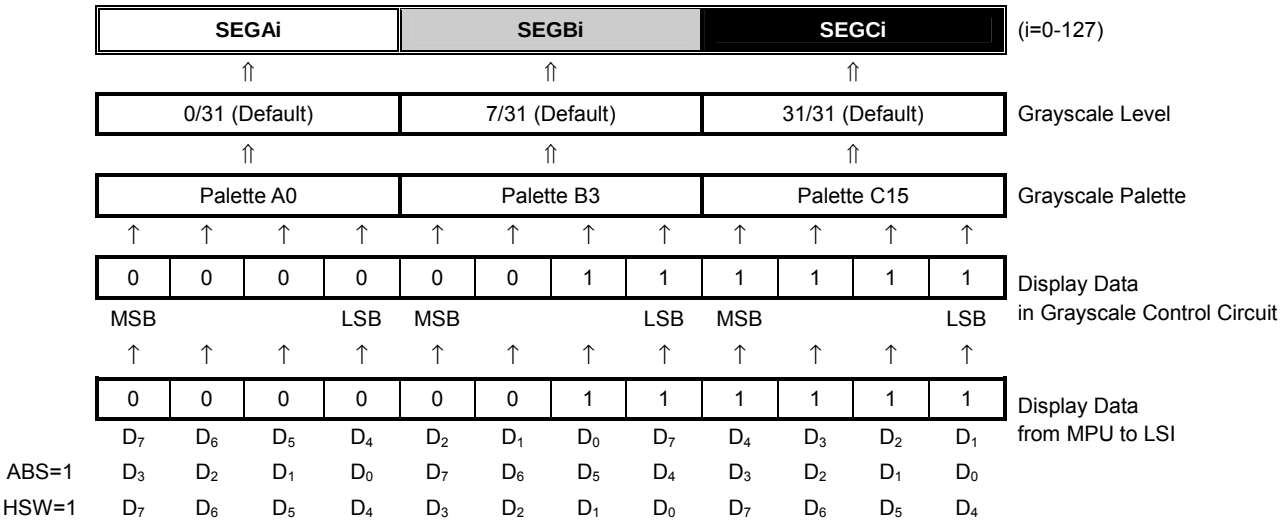
(REF, SWAP)=(0,1) or (1,0)



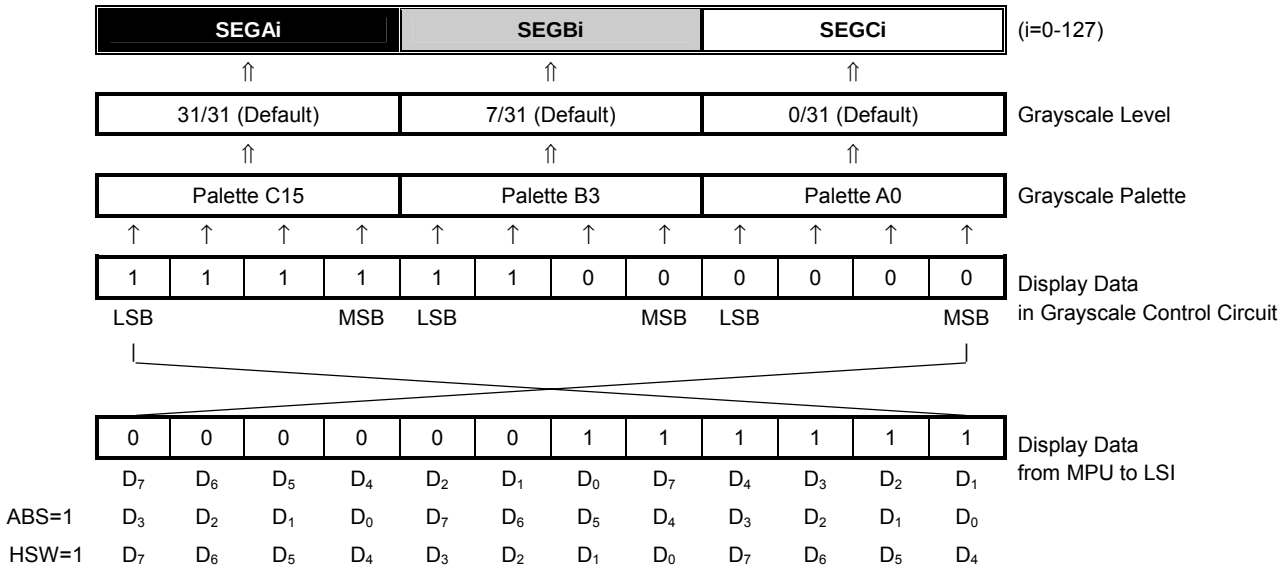
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

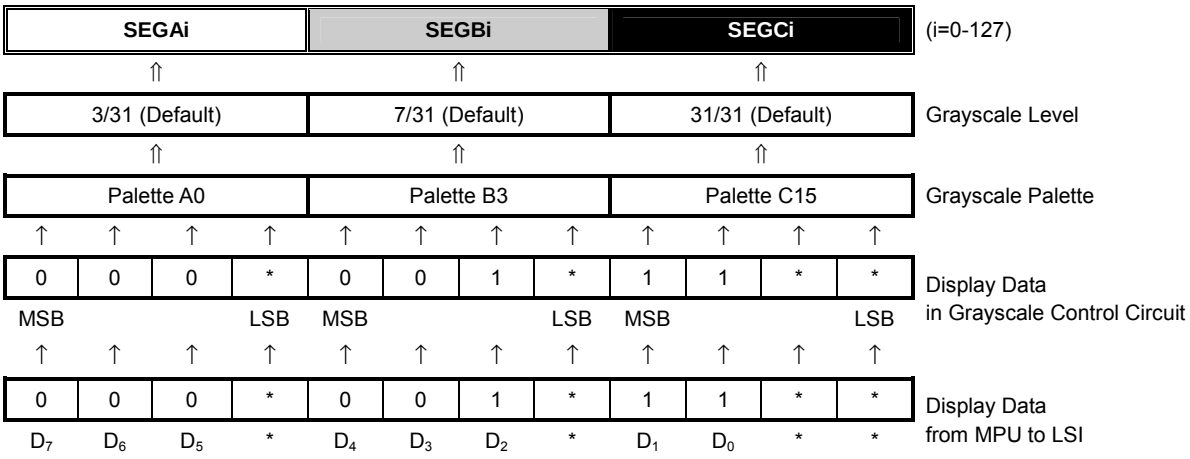


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

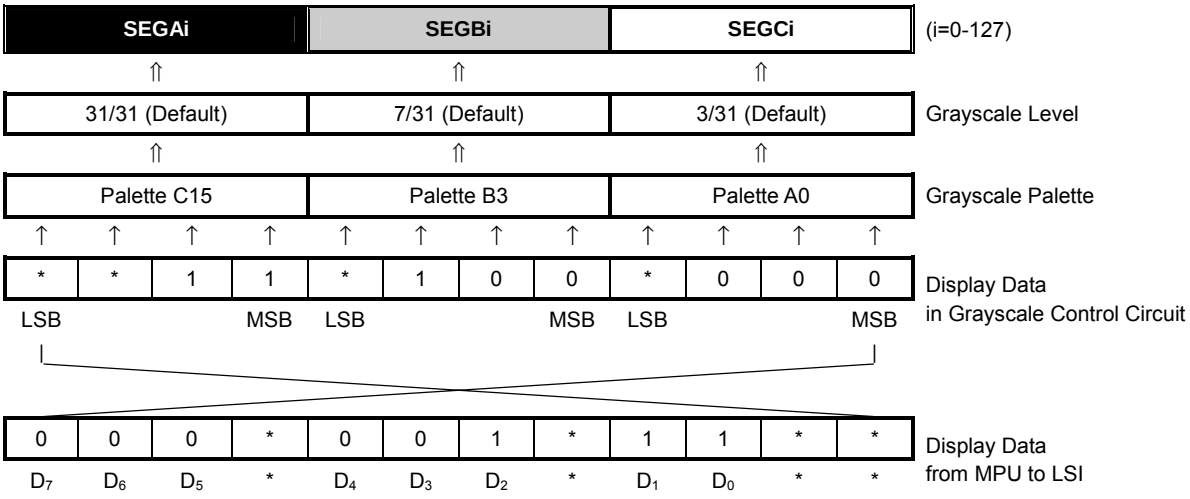
(16-2) Swap Function in Variable 8-grayscale Mode

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

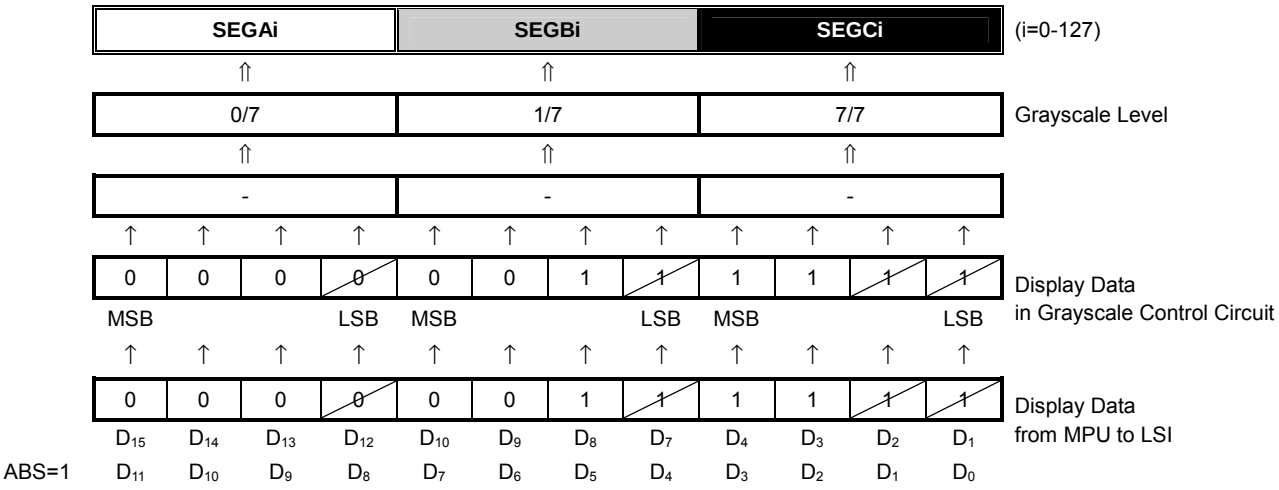


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

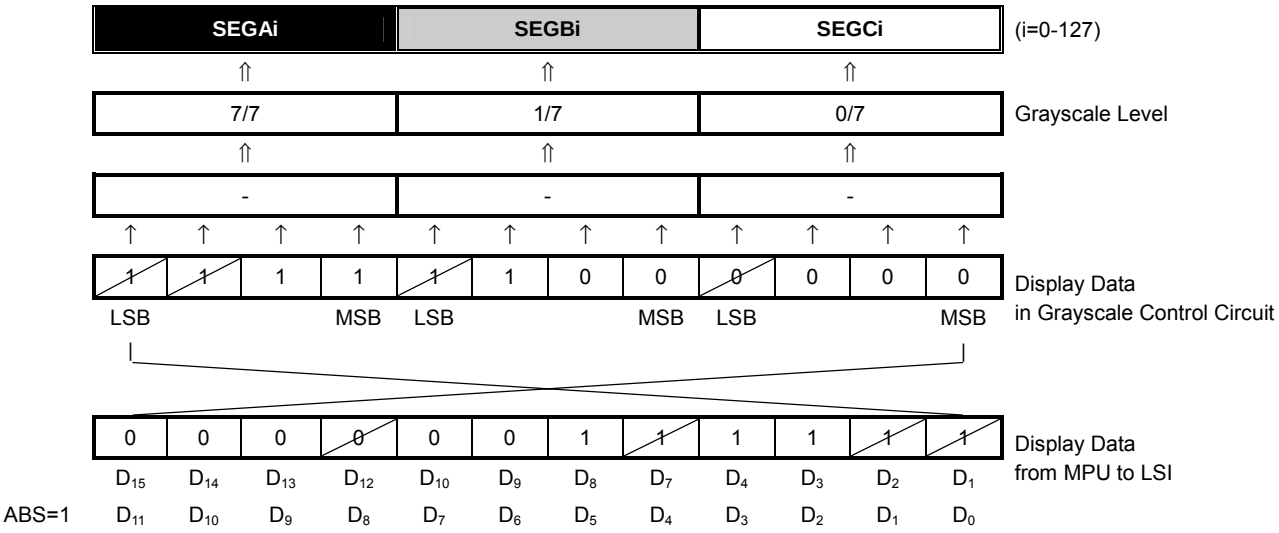
(16-3) Swap Function in Fixed 8-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



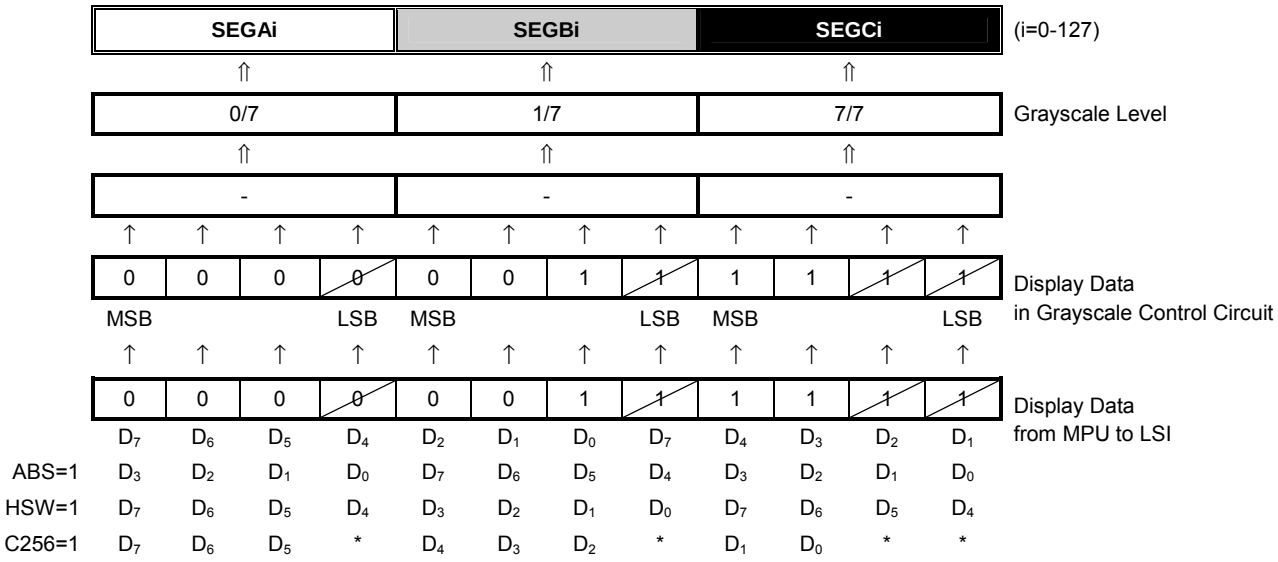
(REF, SWAP)=(0,1) or (1,0)



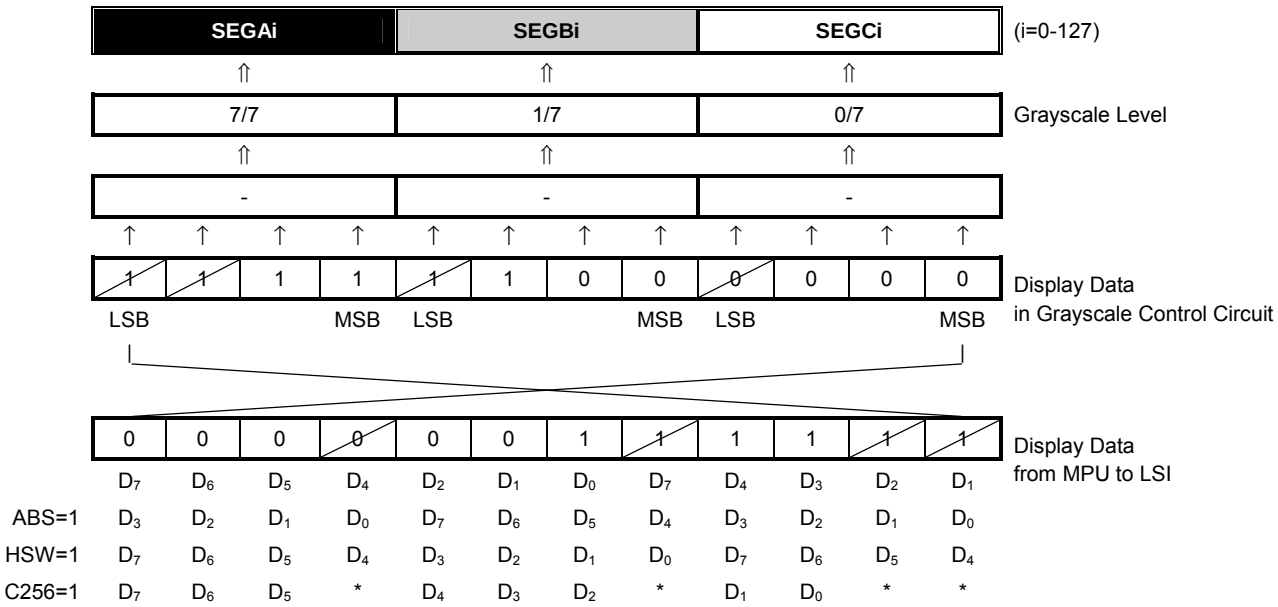
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

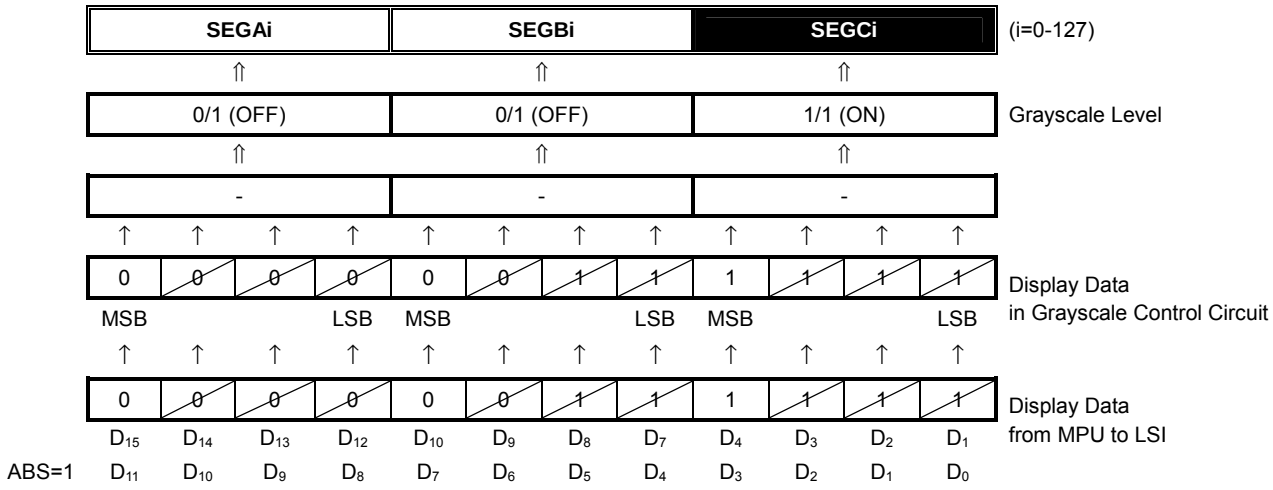


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.
NOTE2) The data indicated with a slash mark (/) is invalid.

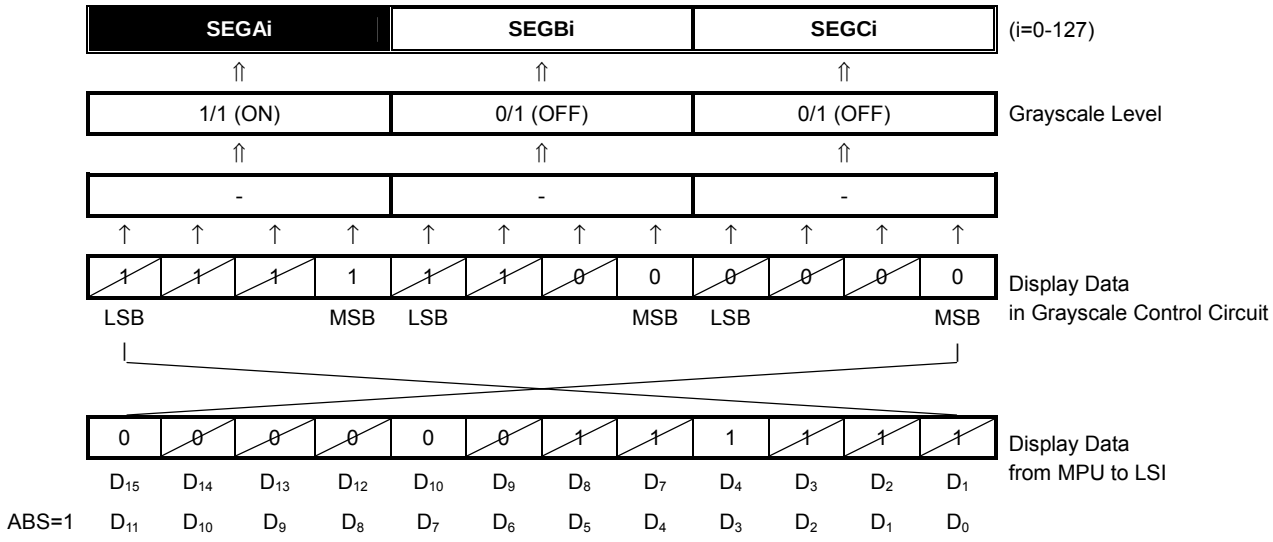
(16-4) Swap Function in B&W Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



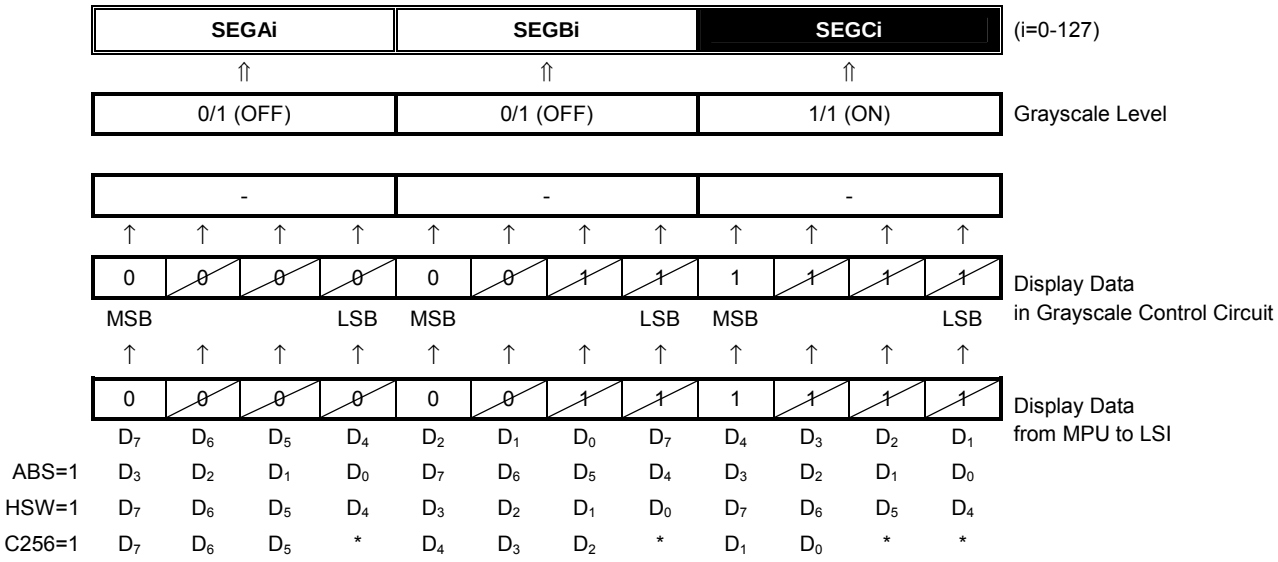
(REF, SWAP)=(0,1) or (1,0)



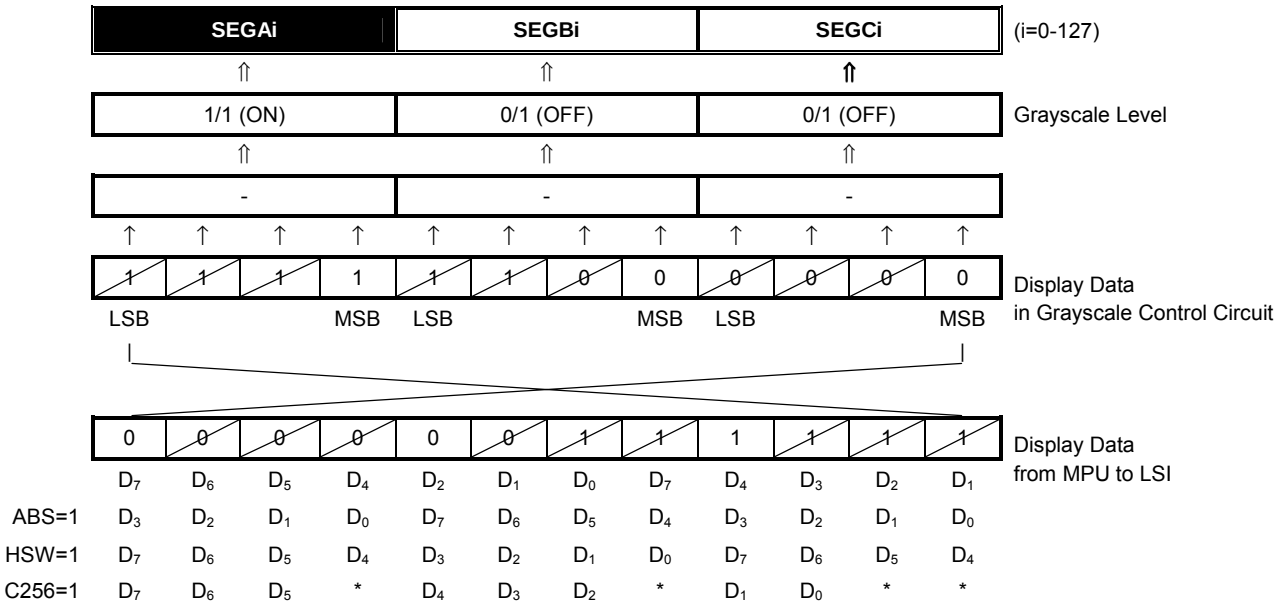
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

(17) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D_3 (SHIFT) bit of the "Display Control (1)" and the "Duty Cycle Ratio", "Initial Display Line" and "Initial COM" instructions.

When the "Initial Display Line" is set to (LA7:LA0=00H: Address "0"), the row address corresponding to an initial COM is "0". However, if the "Initial Display Line" is other than "0", the row address is shifted from "0" by just that address. For instance, when the initial display line address is (LA7:LA0=05H: Address "5") and the initial COM is (SC3:SC0=1H), the row address on the initial COM is "5" and the initial COM is "COM_1".

(17-1) through (17-5) illustrate the examples of the relation between row address and common driver.

(17-1) SHIFT=0, Initial Display Line “0”, Duty Cycle Ratio “1/163”

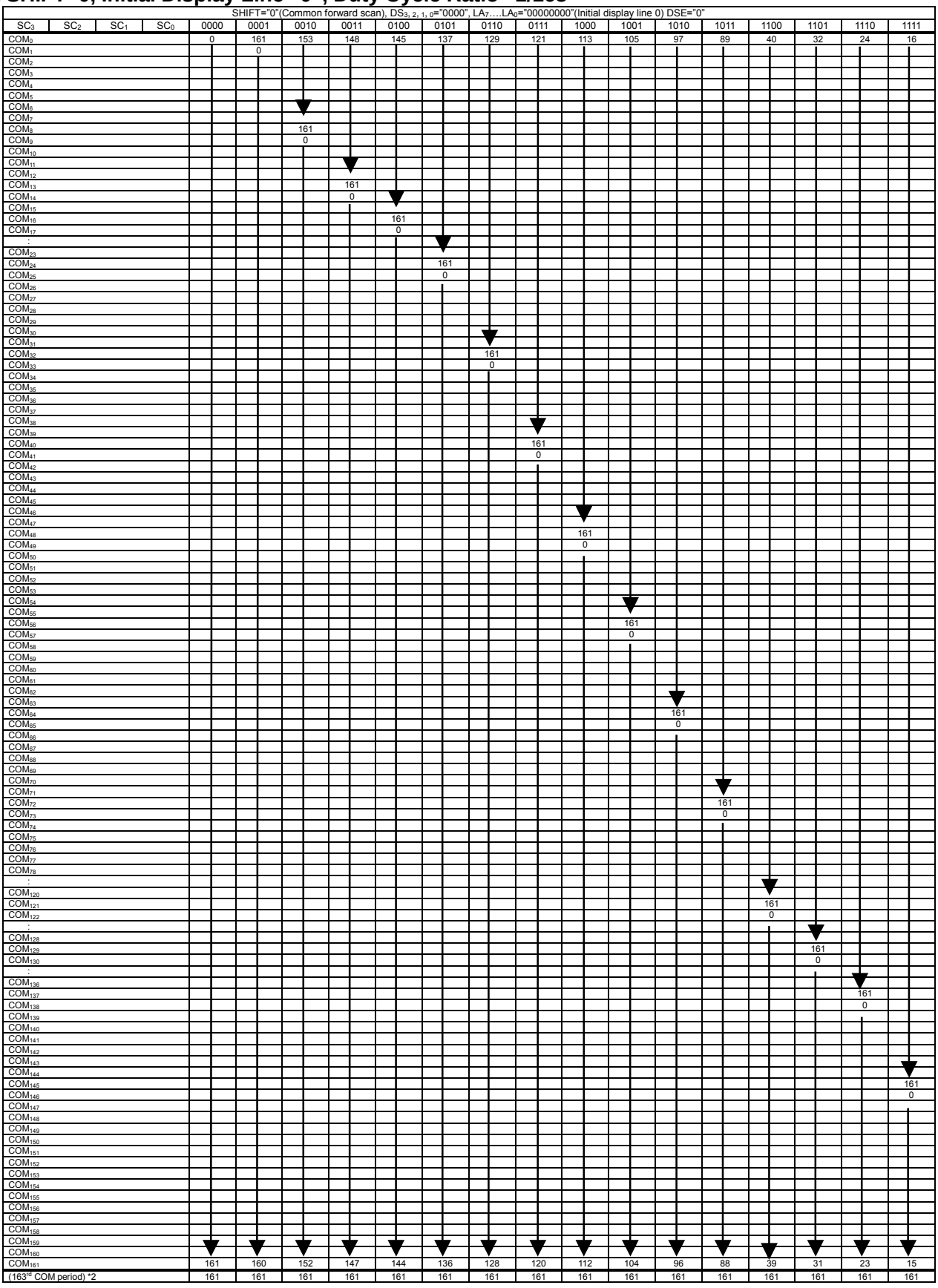


Fig 23 Relation between Row address and Common Driver (1)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 163rd COM timing are the same as for 162nd COM timing (Row address “A1H”).

(17-2) SHIFT=1, Initial Display Line “0”, Duty Cycle Ratio “1/163”

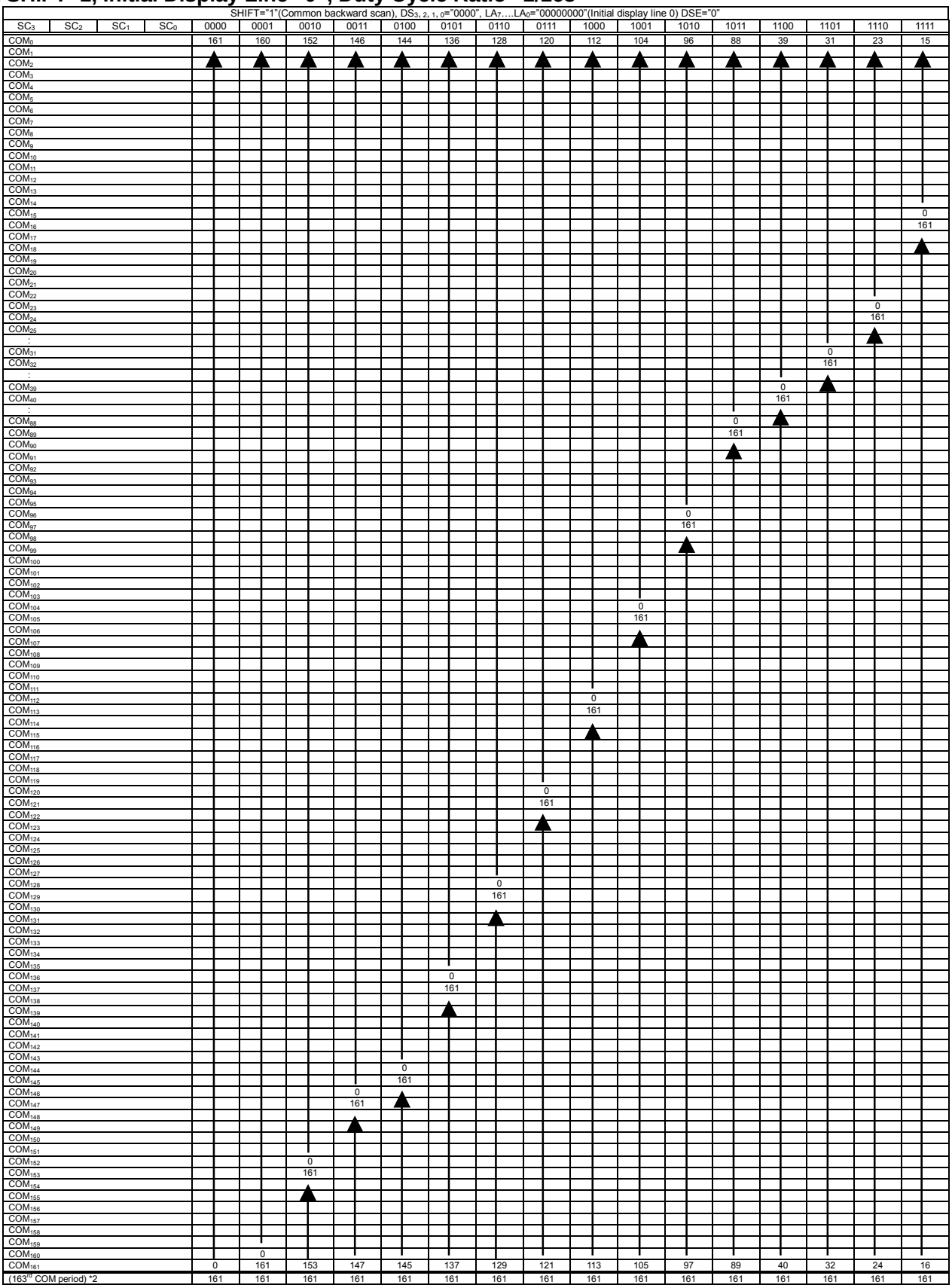


Fig 24 Relation between Row address and Common Driver (2)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 163rd COM timing are the same as for 162nd COM timing (Row address “A1H”).

(17-3) SHIFT=0, Initial Display Line “0”, Duty Cycle Ratio “1/16”

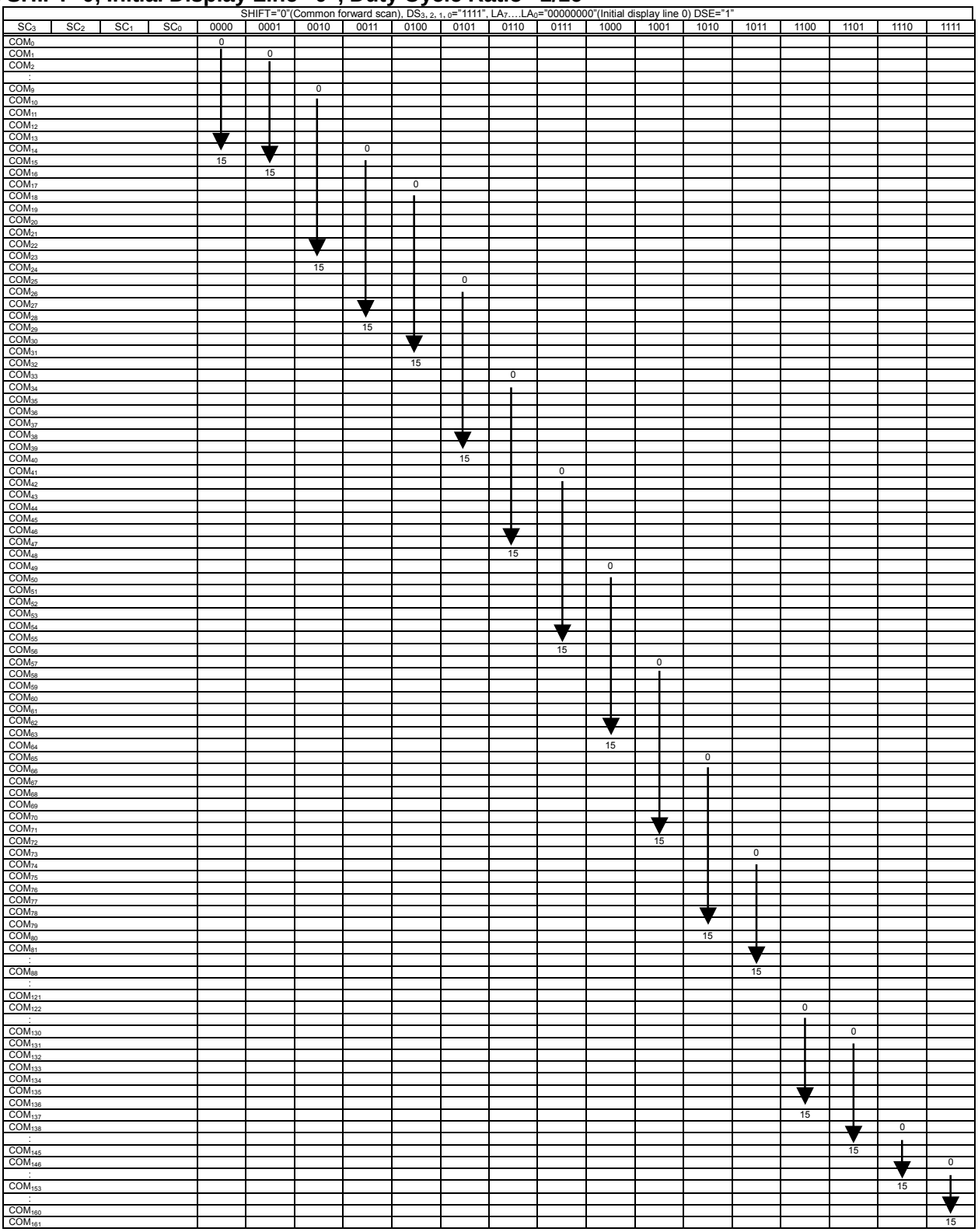


Fig 25 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

(17-4) SHIFT=0, Initial Display Line “5”, Duty Cycle Ratio “1/163”

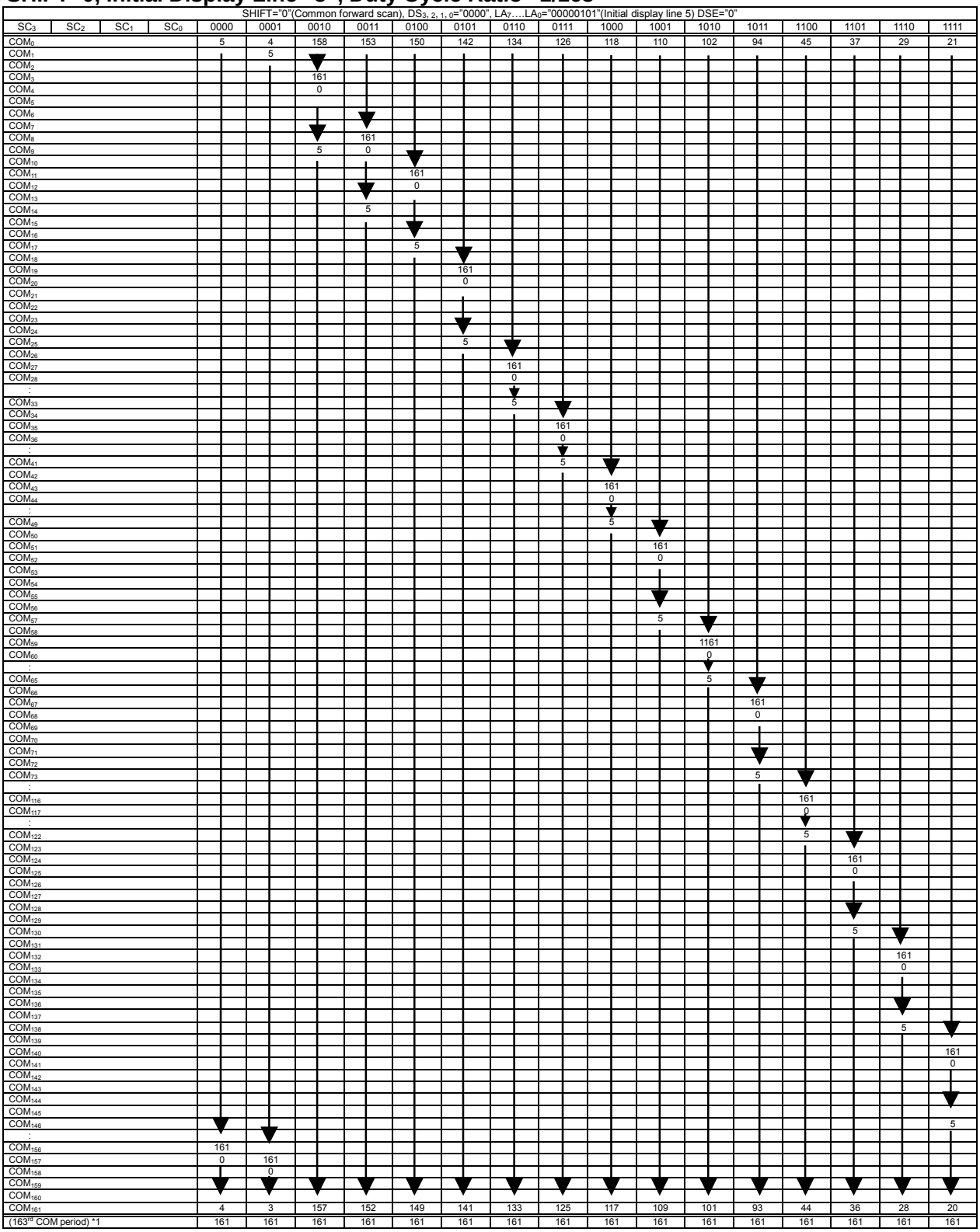


Fig 26 Relation between Row address and Common Driver (4)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

(17-5) SHIFT=0, Initial Display Line “0”, Duty Cycle Ratio “1/162”

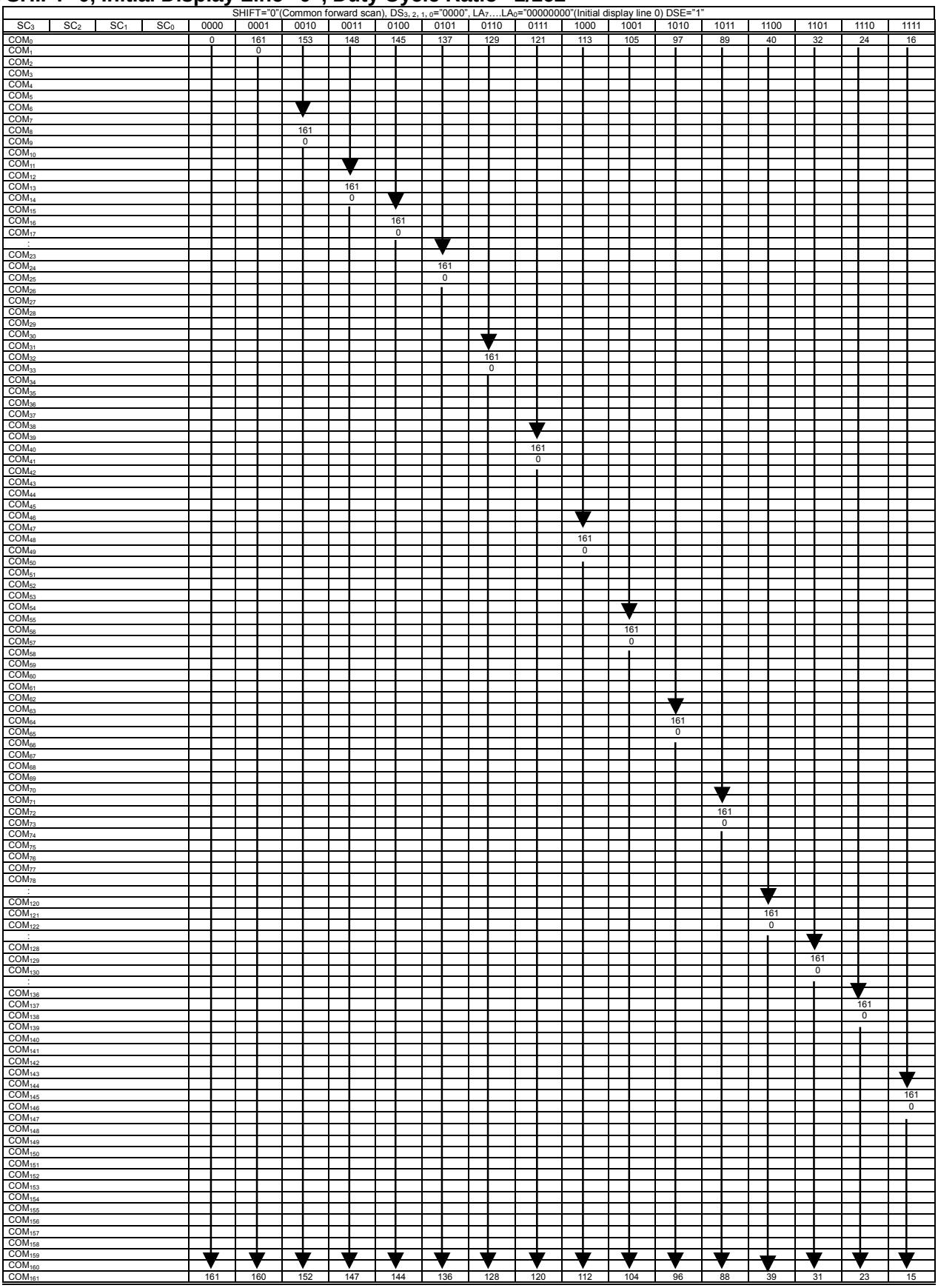
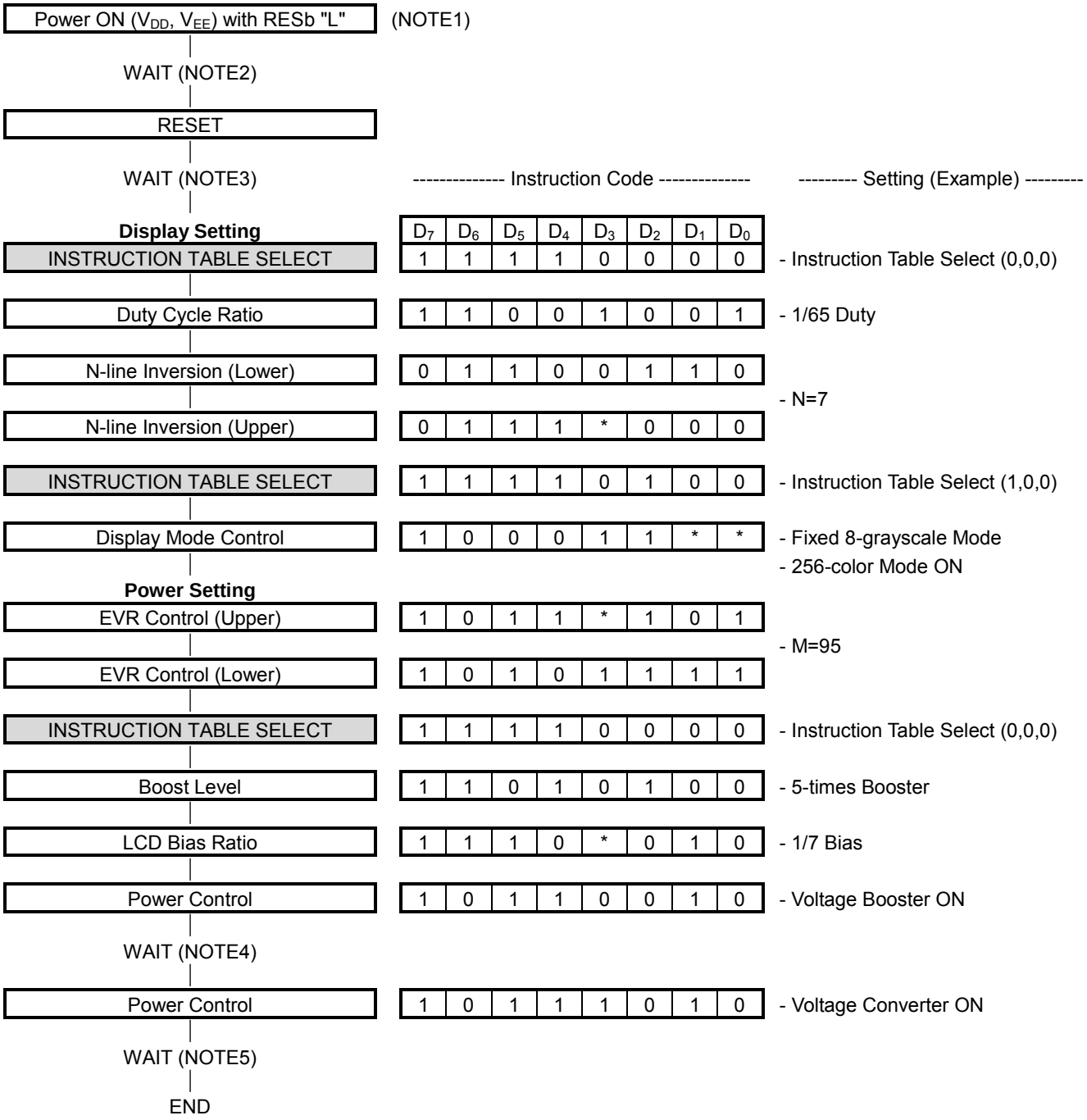


Fig 27 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

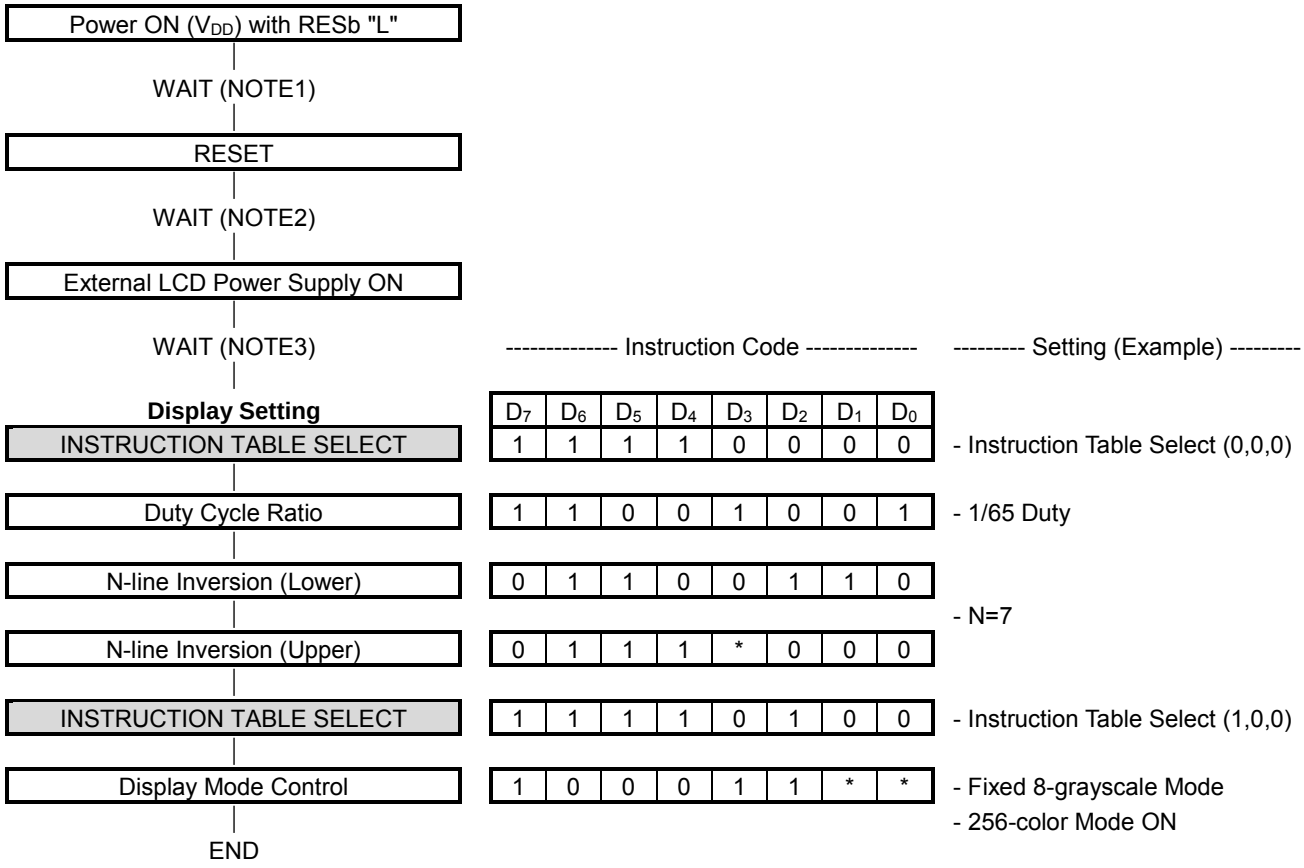
(18) TYPICAL INSTRUCTION SEQUENCES

(18-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the V_{DD} and the V_{EE}, turn on the V_{DD} first.
NOTE2) Wait until the V_{DD} and V_{EE} are stabilized.
NOTE3) Wait 10 [us] or more.
NOTE4) Wait until the V_{OUT} is stabilized.
NOTE5) Wait until the V_{LCD} and V_1-V_4 are stabilized.

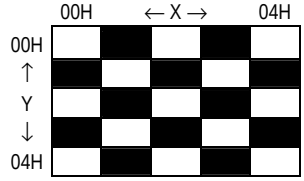
(18-2) Initialization Sequence in Using External LCD Power Supply



NOTE1) Wait until the V_{DD} is stabilized.
NOTE2) Wait 10 [us] or more.
NOTE3) Wait until the external LCD power supply (V_{OUT}, V_{LCD}, V_1-V_4) are stabilized.

(18-3) Display Data Write Sequence

	Instruction Code								Setting (Example)
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Optional Status									
INSTRUCTION TABLE SELECT	1	1	1	1	0	0	0	0	- Instruction Table Select (0,0,0)
Initial Display Line (Lower)	0	1	0	0	0	0	0	0	
Initial Display Line (Upper)	0	1	0	1	*	0	0	0	-Initial Display Line (00)H
Increment Control	1	0	1	0	1	1	1	1	- Window Area Access ON - Read-modify-write ON - Column & Row Increment
Column Address (Lower)	0	0	0	0	0	0	0	0	
Column Address (Upper)	0	0	0	1	0	0	0	0	- Window Start Column Address (00)H
Row Address (Lower)	0	0	1	0	0	0	0	0	
Row Address (Upper)	0	0	1	1	0	0	0	0	- Window Start Row Address (00)H
INSTRUCTION TABLE SELECT	1	1	1	1	0	1	0	1	- Instruction Table Select (1,0,1)
Window End Column Address (Lower)	0	0	0	0	0	1	0	0	
Window End Column Address (Upper)	0	0	0	1	0	0	0	0	-Window End Column Address (04)H
Window End Row Address (Lower)	0	0	1	0	0	1	0	0	
Window End Row Address (Upper)	0	0	1	1	0	0	0	0	- Window End Row Address (04)H
Display Data Write	0	0	0	0	0	0	0	0	- Writing Display Data on the DDRAM for Checker Flag in B&W Mode (Example)
:	1	1	1	1	1	1	1	1	
:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	
:	Repeating All “0” and All “1” Alternately								
:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	
:	1	1	1	1	1	1	1	1	
Display Data Write	0	0	0	0	0	0	0	0	
INSTRUCTION TABLE SELECT	1	1	1	1	0	0	0	0	- Instruction Table Select (0,0,0)
Display Control (1)	1	0	0	0	0	0	0	1	- Display ON
END									

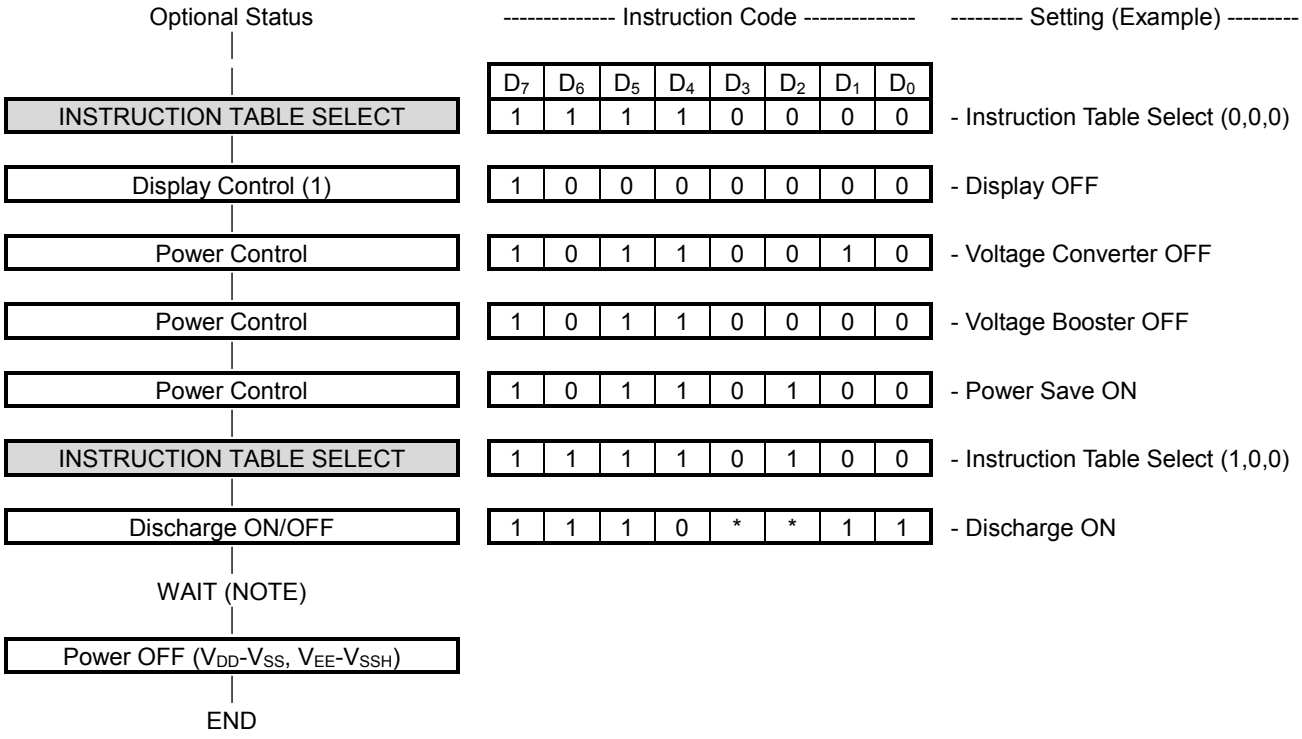


(18-4) Partial Display Sequence

Optional Status	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting (Example)
INSTRUCTION TABLE SELECT	1	1	1	1	0	0	0	0	- Instruction Table Select (0,0,0)
Display Control (1)	1	0	0	0	0	0	0	0	- Display OFF
Power Control	1	0	1	1	0	0	1	0	- Voltage Converter OFF
Power Control	1	0	1	1	0	0	0	0	- Voltage Booster OFF
WAIT (NOTE1)									
Display Setting									
Duty Cycle Ratio	1	1	0	0	1	1	0	1	- 1/33 Duty
Initial Display Line (Lower)	0	1	0	0	0	0	0	0	- Initial Display Line (00)H
Initial Display Line (Upper)	0	1	0	1	*	0	0	0	
INSTRUCTION TABLE SELECT	1	1	1	1	0	1	0	0	- Instruction Table Select (1,0,0)
Initial COM	0	1	1	0	0	0	0	0	- Initial COM: COM0
Power Setting									
EVR Control (Upper)	1	0	1	1	*	0	1	1	- M=60
EVR Control (Lower)	1	0	1	0	1	1	0	0	
INSTRUCTION TABLE SELECT	1	1	1	1	0	0	0	0	- Instruction Table Select (0,0,0)
Boost Level	1	1	0	1	*	0	1	0	- 3-times Booster
LCD Bias Ratio	1	1	1	0	*	1	0	0	- 1/5 Bias
Power Control	1	0	1	1	0	0	1	0	- Voltage Booster ON
WAIT (NOTE2)									
Power Control	1	0	1	1	1	0	1	0	- Voltage Converter ON
WAIT (NOTE3)									
Display Control (1)	1	0	0	0	0	0	0	1	- Display ON
END									

NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.
NOTE2) Wait until the V_{OUT} is stabilized.
NOTE3) Wait until the V_{LCD} and V_1-V_4 are stabilized.

(18-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	Tstg			-45 to +125	°C

NOTE1) D_0 to D_{15}, CSb, RS, RDb, WRb, OSC1, RESb, TEST1, and TEST2
NOTE2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS} and between V_{EE} and V_{SSH}.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	1
	V_{DD2}		2.4		3.3	V	2
	V_{EE}	V_{EE}	2.4		3.3	V	3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	5
Operating Temperature	Topr		-30		85	°C	

NOTE1) Applied to the condition when the reference voltage generator is not used.
NOTE2) Applied to the condition when the reference voltage generator is used.
NOTE3) Applied to the condition when the voltage booster is used.
NOTE4) The following relation among the LCD bias voltages must be maintained.
$V_{SSH}<V_4<V_3<V_2<V_1<V_{LCD}<V_{OUT}$
NOTE5) Relation: $V_{REF}<V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CSb=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C		625	763	900	kHz	*8
	f_{OSC2}			141	172	203		*9
	f_{OSC3}			20.5	25	29.5		*10
External oscillation Frequency	f_{r1}	Rf=10kΩ			750		kHz	*11
	f_{r2}	Rf=51kΩ			185			
	f_{r3}	Rf=390kΩ			27.2			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 7) RL = 500kΩ (V_{OUT} - V_{SS})		(N x V_{EE}) x 0.95			V	*12
Supply current (1)	I_{DD1}	V_{DD} = 2.5V, 7-time booster Whole ON pattern			870	1300	µA	*13
Supply current (2)	I_{DD2}	V_{DD} = 2.5V, 7-time booster Checker pattern			1060	1590		
Supply current (3)	I_{DD3}	V_{DD} = 3V, 6-time booster Whole ON pattern			760	1140		
Supply current (4)	I_{DD4}	V_{DD} = 3V, 6-time booster Checker pattern			930	1400		
Supply current (5)	I_{DD5}	V_{DD} = 3V, 5-time booster Whole ON pattern			520	780		
Supply current (6)	I_{DD6}	V_{DD} = 3V, 5-time booster Checker pattern			650	980		
Supply current (7)	I_{DD7}	V_{DD} = 3V, 4-time booster Whole ON pattern			360	540		
Supply current (8)	I_{DD8}	V_{DD} = 3V, 4-time booster Checker pattern			450	680		
V_{BA} Operating voltage	V_{BA}	V_{EE} = 2.4 to 3.3V		(0.9 V_{EE}) x 0.98	0.9 V_{EE}	(0.9 V_{EE}) x 1.02	V	*14
V_{REG} Operating voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 0.9 x V_{EE} N-time booster (N=2 to 7)		(V_{REF} x N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*15
Output Voltage	V_2			-100	0	+100	mV	*16
	V_3			-100	0	+100		
	V_{D12}			-30	0	+30		
	V_{D34}			-30	0	+30		
	V_{D24}			-30	0	+30		

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/163 to 1/97	1/81 to 1/57	1/49 to 1/33	1/25 to 1/17	
Internal clock	f_{OSC}	Variable 8-/16-level Grayscale Mode	f_{OSC} / (62xD)	f_{OSC} / (62xDx2)	f_{OSC} / (62xDx4)	f_{OSC} / (62xDx8)	FLM
		Fixed 8-level Grayscale Mode	f_{OSC} / (14xD)	f_{OSC} / (14xDx2)	f_{OSC} / (14xDx4)	f_{OSC} / (14xDx8)	
		B&W Mode	f_{OSC} / (2xD)	f_{OSC} / (2xDx2)	f_{OSC} / (2xDx4)	f_{OSC} / (2xDx8)	
External clock	f_{CK}	Variable 8-/16-level Grayscale Mode	f_{CK} / (62xD)	f_{CK} / (62xDx2)	f_{CK} / (62xDx4)	f_{CK} / (62xDx8)	
		Fixed 8-level Grayscale Mode	f_{CK} / (14xD)	f_{CK} / (14xDx2)	f_{CK} / (14xDx4)	f_{CK} / (14xDx8)	
		B&W Mode	f_{CK} / (2xD)	f_{CK} / (2xDx2)	f_{CK} / (2xDx4)	f_{CK} / (2xDx8)	

NOTE1) D_0-D_{15}, CSb, RS, RDb, WRb, P/S, SEL68 and RESb

NOTE2) D_0-D_{15}

NOTE3) CL, FLM, FR and CLK

NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1

NOTE5) D_0-D_{15} in high impedance

NOTE6) $SEGA_0$-$SEGA_{127}$, $SEGB_0$-$SEGB_{127}$, $SEGC_0$-$SEGC_{127}$ and COM_0-COM_{161}
This parameter defines the resistance between each COM/SEG and each LCD bias (V_{LCD}, V_1, V_2, V_3 and V_4).
- 0.5V Difference / 1/9 LCD Bias

NOTE7) V_{DD}
Oscillator is halted.
- CSb=1 (Disabled) / No-load on COM/SEG

NOTE8) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)

NOTE9) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)

NOTE10) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.
- (Rf2, Rf1, Rf0)=(0,0,0)

NOTE11) OSC2
- V_{DD}=3V / Ta=25°C

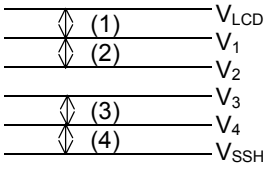
NOTE12) V_{OUT}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- V_{EE}=2.4V to 3.3V / EVR= (1,1,1,1,1,1,1,1) / 1/5 to 1/12 LCD Bias / 1/163 Duty Cycle / No-load on COM/SEG / RL=500kΩ between V_{OUT} and V_{SSH} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"

NOTE13) V_{SS}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- EVR= (1,1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU / V_{DD}=V_{EE} / V_{REF}=0.9V_{EE} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/163 Duty cycle / Ta=25°C

NOTE14) V_{BA}
- V_{BA}=V_{REF} / Boost Level (N)="1",/ DCON="0" / V_{OUT}=13.5V

NOTE15) V_{REG}
- V_{EE}=2.4V to 3.3V / V_{REF}=0.9V_{EE} / VOUT=18V / 1/5 to 1/12 LCD bias ratio / 1/163 duty cycle / EVR=(1,1,1,1,1,1,1,1) / Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "7" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NLIN="0"

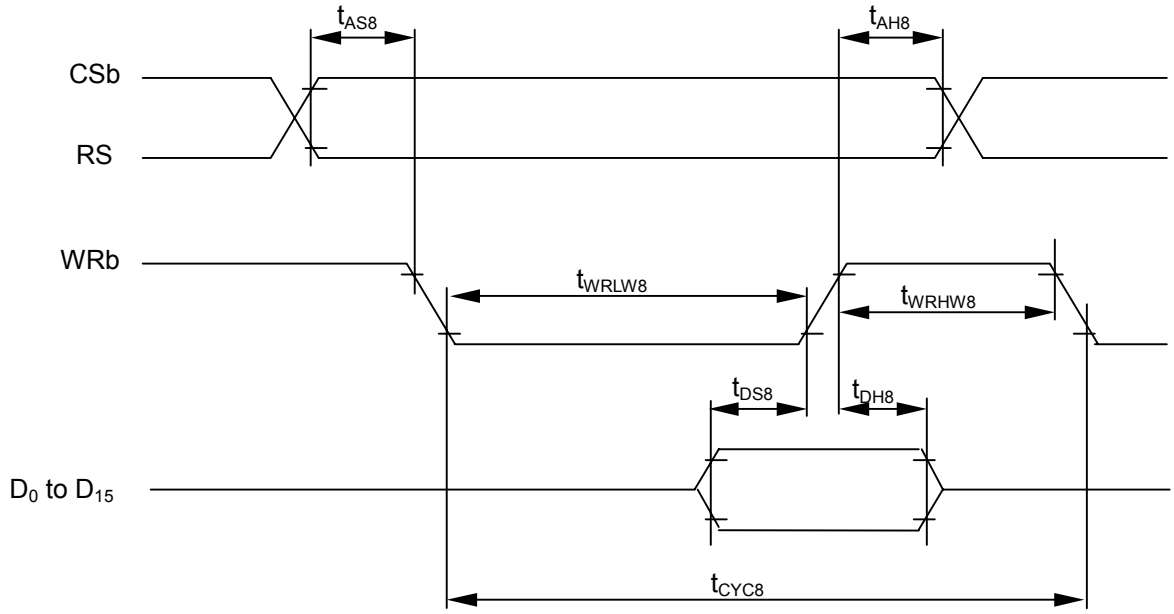
NOTE16) V_{LCD}, V_1, V_2, V_3 and V_4
- V_{EE}=3.0V / V_{REF}=0.9V_{EE} / V_{OUT}=15V/ 1/5 to 1/12 LCD Bias / EVR= (1,1,1,1,1,1,1,1) / Display OFF / No-load on COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



V_{D12}: (1)-(2)
V_{D34}: (3)-(4)
V_{D24}: (2)-(4)

■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

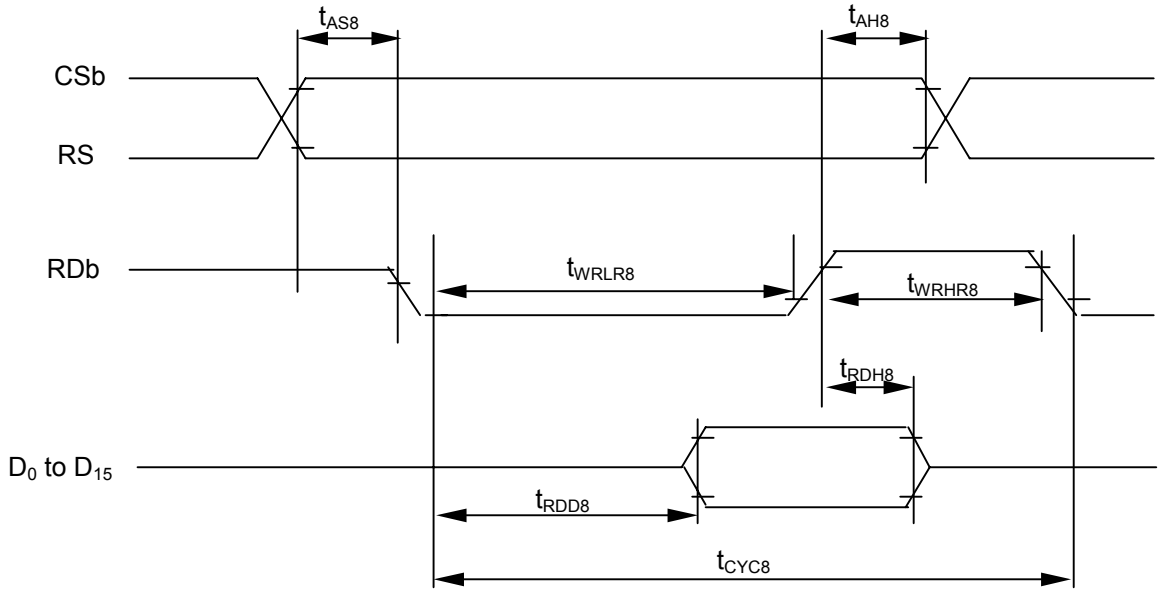
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(2) Read Operation (Parallel Interface / 80-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	0	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

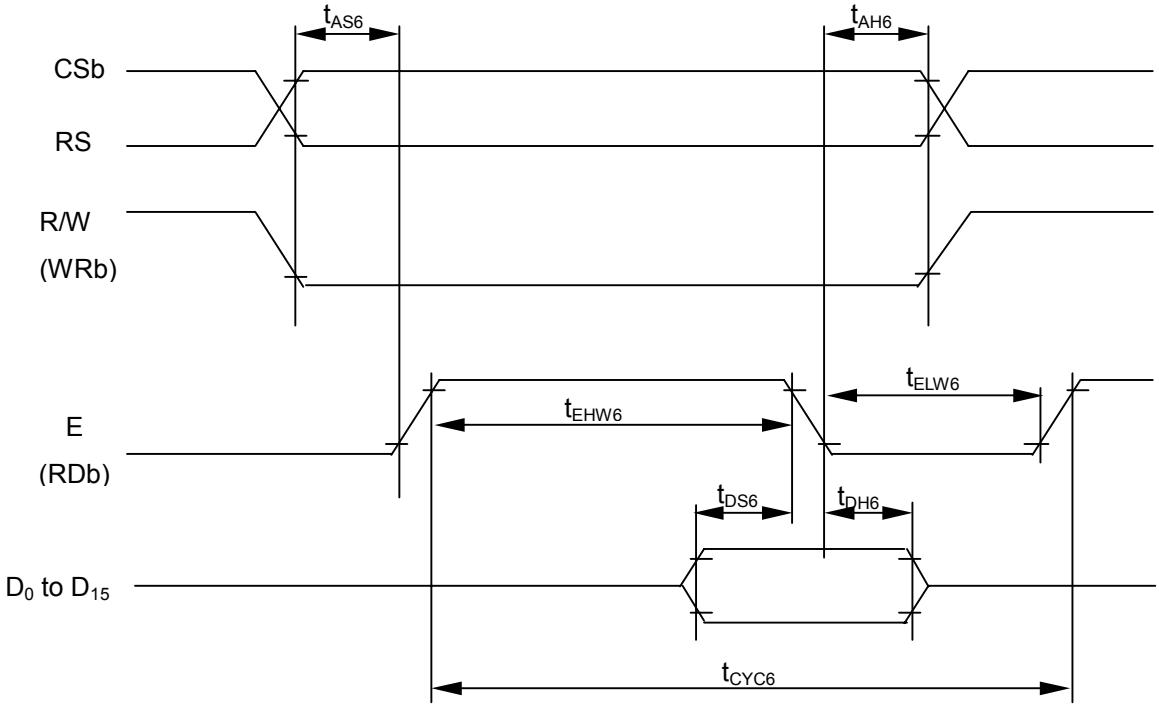
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	0	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	0	110	ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(3) Write Operation (Parallel Interface / 68-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		90 35 35		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

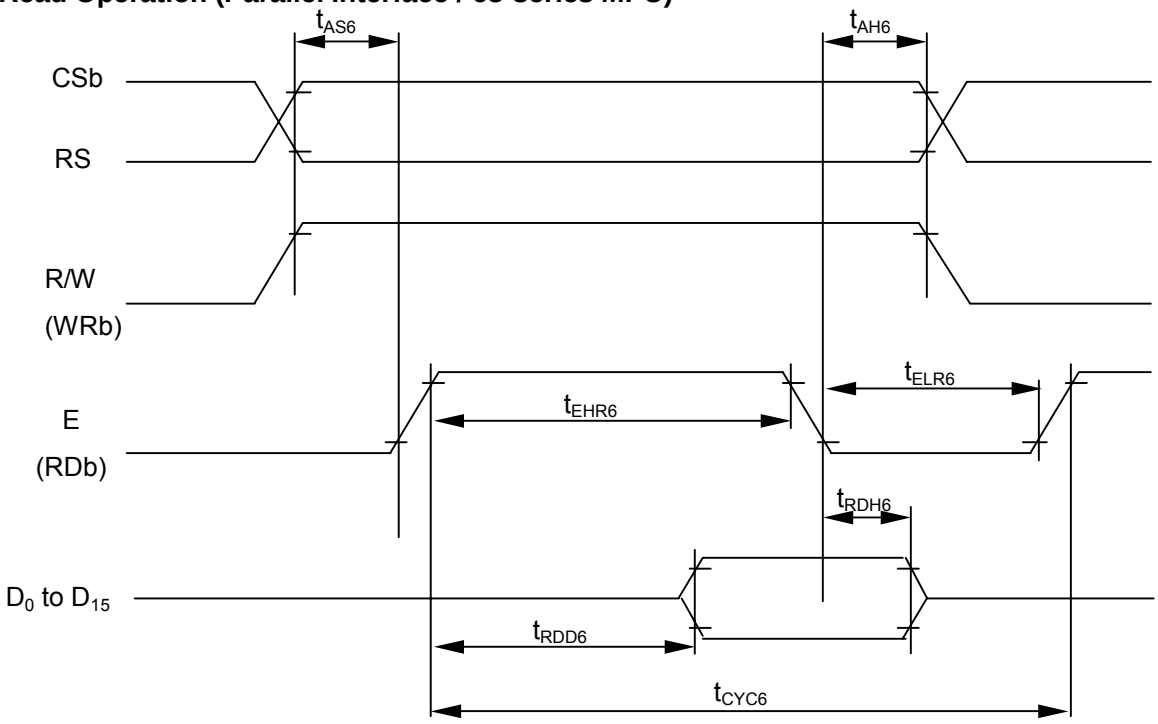
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		160 70 70		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		50 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		180 80 80		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		70 10		ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(4) Read Operation (Parallel Interface / 68-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

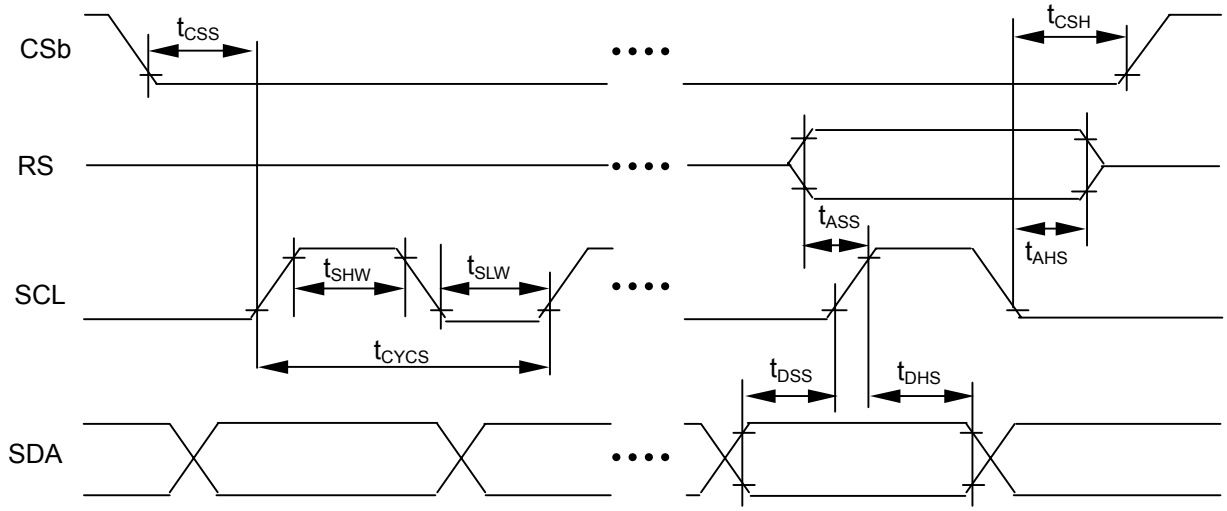
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	110	ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(5) Write Operation (Serial Interface)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

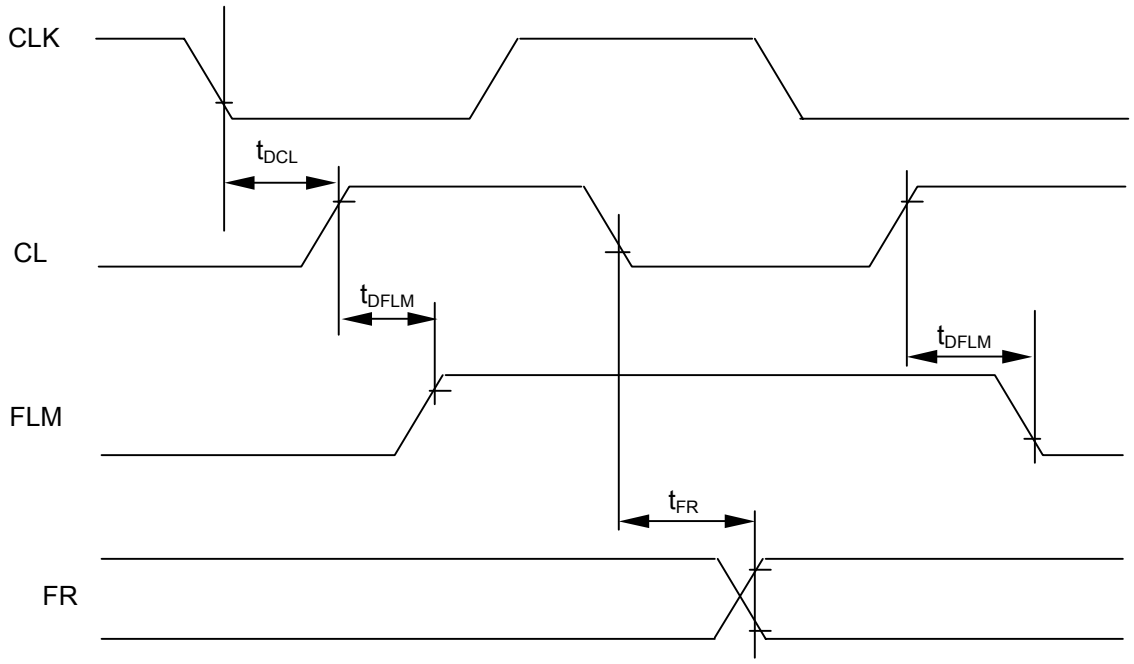
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(6) Display Control Timing



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

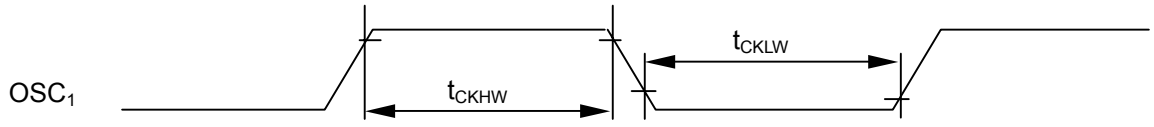
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(7) Input Clock Timing

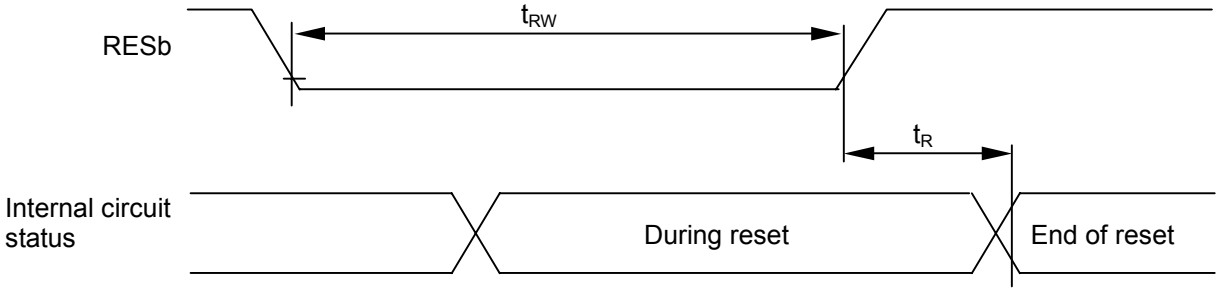


(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 “H” level pulse width (1)	t_{CKHW1}		0.555	0.800	µs	OSC1 (NOTE2)
OSC1 “L” level pulse width (1)	t_{CKLW1}		0.555	0.800	µs	
OSC1 “H” level pulse width (2)	t_{CKHW2}		2.46	3.54	µs	OSC1 (NOTE3)
OSC1 “L” level pulse width (2)	t_{CKLW2}		2.46	3.54	µs	
OSC1 “H” level pulse width (3)	t_{CKHW3}		16.9	24.4	µs	OSC1 (NOTE4)
OSC1 “L” level pulse width (3)	t_{CKLW3}		16.9	24.4	µs	

NOTE1) Each timing is specified based on 20% and 80% of V_{DD}.
NOTE2) Applied to Variable 8-/16-level grayscale mode (MON=”0”,PWM=”0”)
NOTE3) Applied to fixed 8-level grayscale mode (MON=”0”,PWM=”1”)
NOTE4) Applied to B&W mode (MON=”1”)

(8) Reset Input Timing



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb “L” level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb “L” level pulse width	t_{RW}		10.0		µs	RESb

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

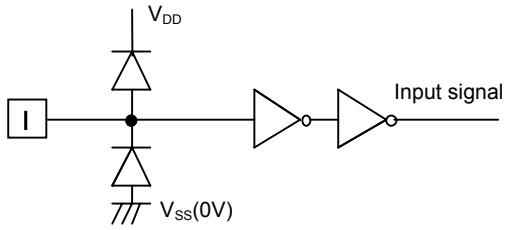
(9) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

■ INPUT/OUTPUT BLOCK DIAGRAMS

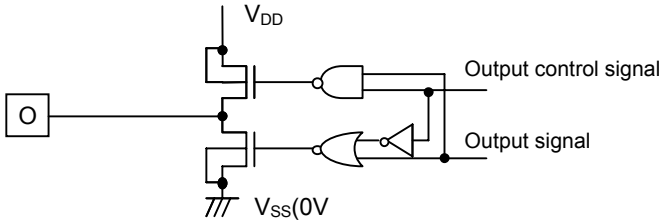
Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



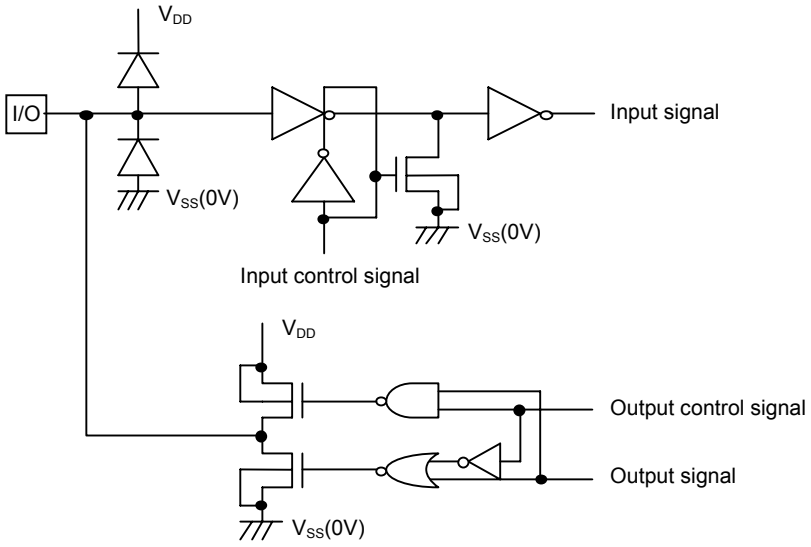
Output Block Diagram

Terminals : FLM, CL, FR, CLK



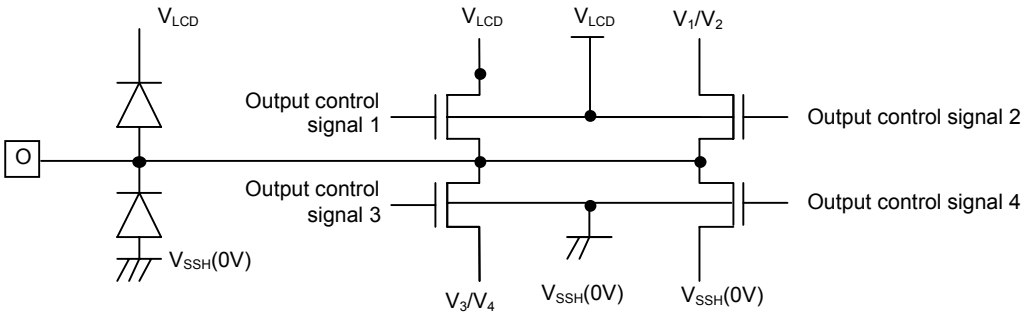
Input/Output Block Diagram

Terminals : D_0 - D_{15}



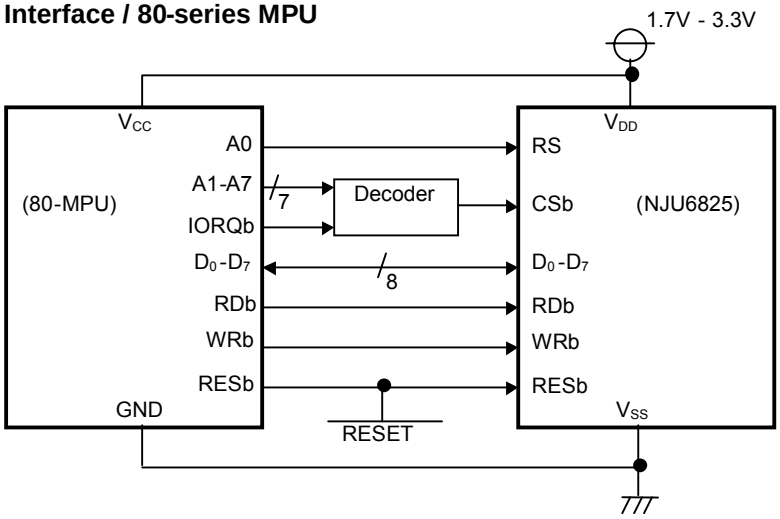
COM/SEG Driver Block Diagram

Terminals : $SEGA_0/B_0/C_0$ – $SEGA_{127}/B_{127}/C_{127}$, COM_0 – COM_{161}

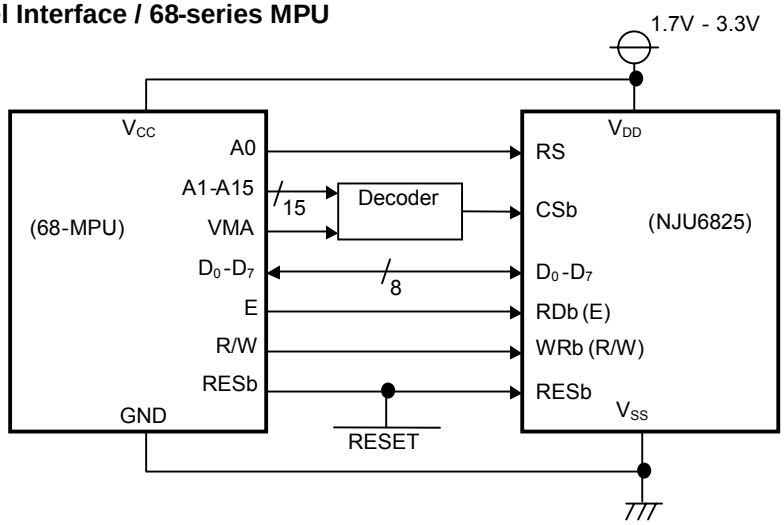


■ MPU CONNECTIONS

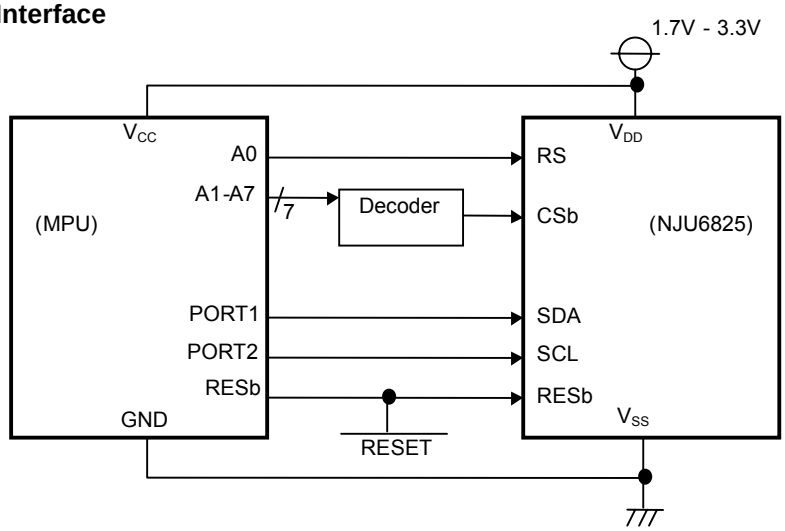
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



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