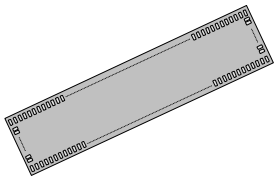
40COMMON x 128RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6820** is a 40COMMON x 128RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 61,440-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16).

In addition, the **NJU6820** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



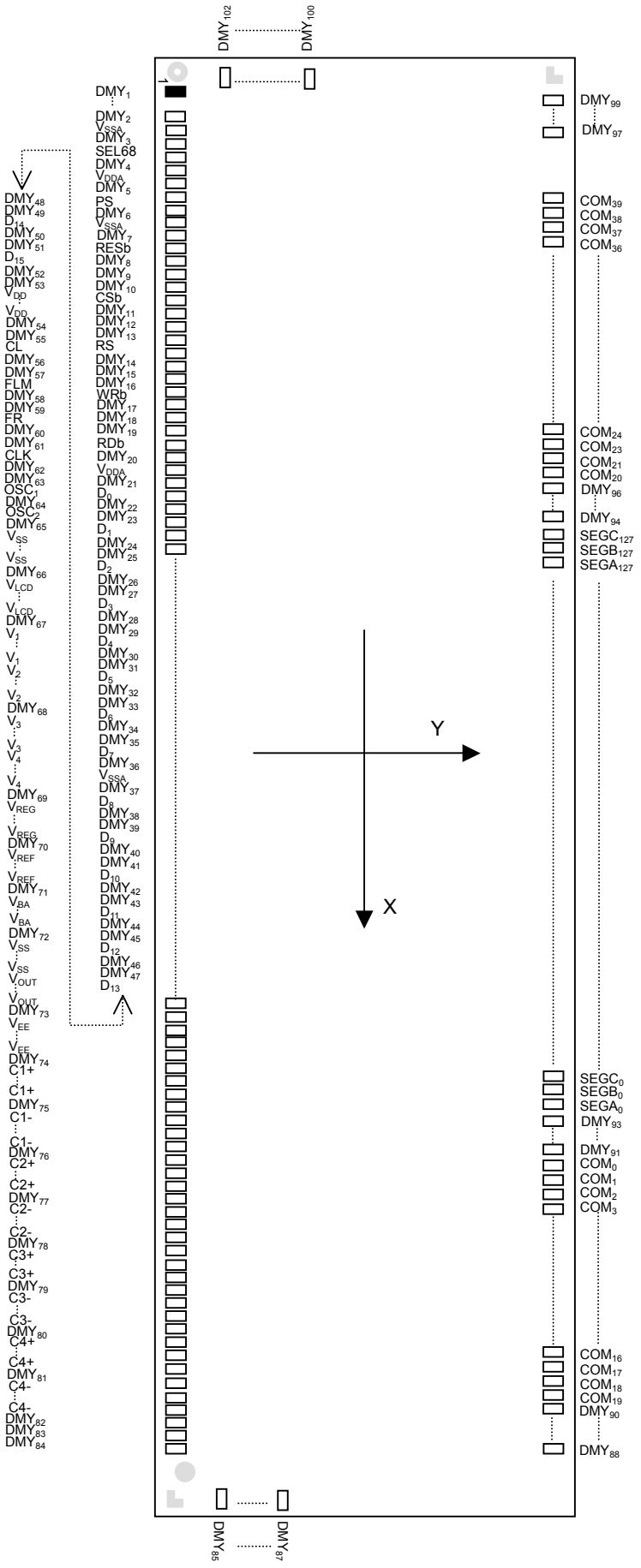
BUMP CHIP

■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 40 common Drivers x 128RGB Drivers (384-segment Drivers in B&W)
- Built-in Display Data RAM (DDRAM) : 61,440 bits for Graphic Display
- Programmable Display Mode
  - Variable 16-grayscale Mode : 4,096 Colors
  - Variable 8-grayscale Mode : 256 Colors
  - Fixed 8-grayscale Mode : 256 Colors
  - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 5 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- Various Useful Instructions
- Low Operating Current : 450uA Typical at V_{DD}=3V, 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

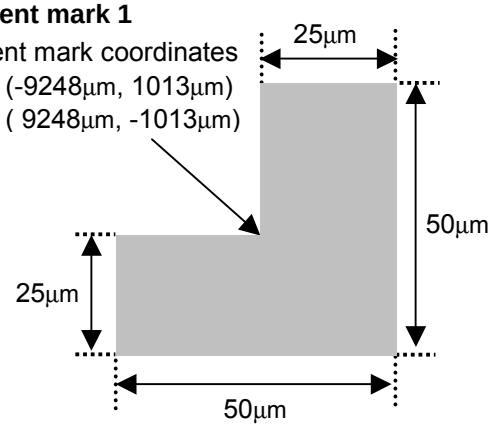
TABLE OF CONTENTS

■ PAD LOCATION



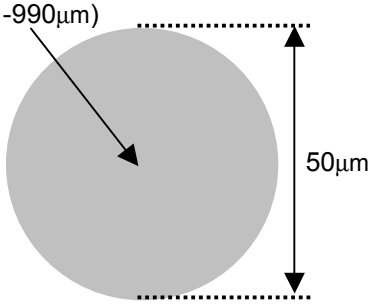
Alignment mark 1

Alignment mark coordinates
(-9248μm, 1013μm)
(9248μm, -1013μm)



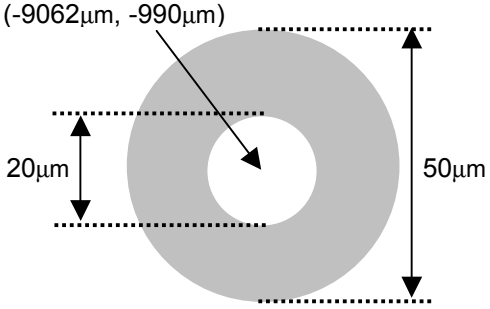
Alignment mark 2

Alignment mark coordinates
(9062μm, -990μm)



Alignment mark 3

Alignment mark coordinates
(-9062μm, -990μm)



Chip Center	:X=0um, Y=0um
Chip Size	:X=18.86mm, Y= 2.39mm
Chip Thickness	:625um ± 25um
Bump Pitch	:42um(Min)
Bump Space	:18um
Bump Size	:24um x 140um
Bump hight	:17.5um(Typ)
Bump Material	:Au

■ PAD COORDINATES 1

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
1	DMY_0	-8967	-990	51	DMY_{24}	-6699	-990	101	DMY_{48}	-3507	-990
2	DMY_1	-8925	-990	52	DMY_{25}	-6573	-990	102	DMY_{49}	-3381	-990
3	DMY_2	-8883	-990	53	D_2	-6531	-990	103	D_{14}	-3339	-990
4	V_{SSA}	-8841	-990	54	D_2	-6489	-990	104	D_{14}	-3297	-990
5	V_{SSA}	-8799	-990	55	DMY_{26}	-6447	-990	105	DMY_{50}	-3255	-990
6	DMY_3	-8757	-990	56	DMY_{27}	-6321	-990	106	DMY_{51}	-3129	-990
7	SEL68	-8715	-990	57	D_3	-6279	-990	107	D_{15}	-3087	-990
8	SEL68	-8673	-990	58	D_3	-6237	-990	108	D_{15}	-3045	-990
9	DMY_4	-8631	-990	59	DMY_{28}	-6195	-990	109	DMY_{52}	-3003	-990
10	V_{DDA}	-8589	-990	60	DMY_{29}	-6069	-990	110	DMY_{53}	-2877	-990
11	V_{DDA}	-8547	-990	61	D_4	-6027	-990	111	V_{DD}	-2835	-990
12	DMY_5	-8505	-990	62	D_4	-5985	-990	112	V_{DD}	-2793	-990
13	PS	-8463	-990	63	DMY_{30}	-5943	-990	113	V_{DD}	-2751	-990
14	PS	-8421	-990	64	DMY_{31}	-5817	-990	114	V_{DD}	-2709	-990
15	DMY_6	-8379	-990	65	D_5	-5775	-990	115	V_{DD}	-2667	-990
16	V_{SSA}	-8337	-990	66	D_5	-5733	-990	116	V_{DD}	-2625	-990
17	V_{SSA}	-8295	-990	67	DMY_{32}	-5691	-990	117	V_{DD}	-2583	-990
18	DMY_7	-8253	-990	68	DMY_{33}	-5565	-990	118	V_{DD}	-2541	-990
19	RESb	-8211	-990	69	D_6	-5523	-990	119	V_{DD}	-2499	-990
20	RESb	-8169	-990	70	D_6	-5481	-990	120	V_{DD}	-2457	-990
21	DMY_8	-8127	-990	71	DMY_{34}	-5439	-990	121	V_{DD}	-2415	-990
22	DMY_9	-8085	-990	72	DMY_{35}	-5313	-990	122	DMY_{54}	-2289	-990
23	DMY_{10}	-8043	-990	73	D_7	-5271	-990	123	DMY_{55}	-2163	-990
24	CSb	-8001	-990	74	D_7	-5229	-990	124	CL	-2121	-990
25	CSb	-7959	-990	75	DMY_{36}	-5187	-990	125	CL	-2079	-990
26	DMY_{11}	-7917	-990	76	V_{SSA}	-5061	-990	126	DMY_{56}	-2037	-990
27	DMY_{12}	-7875	-990	77	V_{SSA}	-5019	-990	127	DMY_{57}	-1911	-990
28	DMY_{13}	-7833	-990	78	DMY_{37}	-4893	-990	128	FLM	-1869	-990
29	RS	-7791	-990	79	D_8	-4851	-990	129	FLM	-1827	-990
30	RS	-7749	-990	80	D_8	-4809	-990	130	DMY_{58}	-1785	-990
31	DMY_{14}	-7707	-990	81	DMY_{38}	-4767	-990	131	DMY_{59}	-1659	-990
32	DMY_{15}	-7665	-990	82	DMY_{39}	-4641	-990	132	FR	-1617	-990
33	DMY_{16}	-7623	-990	83	D_9	-4599	-990	133	FR	-1575	-990
34	WRb	-7581	-990	84	D_9	-4557	-990	134	DMY_{60}	-1533	-990
35	WRb	-7539	-990	85	DMY_{40}	-4515	-990	135	DMY_{61}	-1407	-990
36	DMY_{17}	-7497	-990	86	DMY_{41}	-4389	-990	136	CLK	-1365	-990
37	DMY_{18}	-7455	-990	87	D_{10}	-4347	-990	137	CLK	-1323	-990
38	DMY_{19}	-7413	-990	88	D_{10}	-4305	-990	138	DMY_{62}	-1281	-990
39	RDb	-7371	-990	89	DMY_{42}	-4263	-990	139	DMY_{63}	-1155	-990
40	RDb	-7329	-990	90	DMY_{43}	-4137	-990	140	OSC_1	-1113	-990
41	DMY_{20}	-7287	-990	91	D_{11}	-4095	-990	141	OSC_1	-1071	-990
42	V_{DDA}	-7245	-990	92	D_{11}	-4053	-990	142	DMY_{64}	-1029	-990
43	V_{DDA}	-7203	-990	93	DMY_{44}	-4011	-990	143	OSC_2	-903	-990
44	DMY_{21}	-7077	-990	94	DMY_{45}	-3885	-990	144	OSC_2	-861	-990
45	D_0	-7035	-990	95	D_{12}	-3843	-990	145	DMY_{65}	-735	-990
46	D_0	-6993	-990	96	D_{12}	-3801	-990	146	V_{SS}	-693	-990
47	DMY_{22}	-6951	-990	97	DMY_{46}	-3759	-990	147	V_{SS}	-651	-990
48	DMY_{23}	-6825	-990	98	DMY_{47}	-3633	-990	148	V_{SS}	-609	-990
49	D_1	-6783	-990	99	D_{13}	-3591	-990	149	V_{SS}	-567	-990
50	D_1	-6741	-990	100	D_{13}	-3549	-990	150	V_{SS}	-525	-990

■ PAD COORDINATES 2

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
151	V_{SS}	-483	-990	201	V_4	1953	-990	251	V_{OUT}	4179	-990
152	V_{SS}	-441	-990	202	V_4	1995	-990	252	V_{OUT}	4221	-990
153	V_{SS}	-399	-990	203	V_4	2037	-990	253	V_{OUT}	4263	-990
154	V_{SS}	-357	-990	204	V_4	2079	-990	254	V_{OUT}	4305	-990
155	V_{SS}	-315	-990	205	DMY_{69}	2121	-990	255	V_{OUT}	4347	-990
156	V_{SS}	-273	-990	206	V_{REG}	2163	-990	256	V_{OUT}	4389	-990
157	DMY_{66}	-147	-990	207	V_{REG}	2205	-990	257	V_{OUT}	4431	-990
158	V_{LCD}	-21	-990	208	V_{REG}	2247	-990	258	V_{OUT}	4473	-990
159	V_{LCD}	21	-990	209	V_{REG}	2289	-990	259	DMY_{73}	4641	-990
160	V_{LCD}	63	-990	210	V_{REG}	2331	-990	260	V_{EE}	4683	-990
161	V_{LCD}	105	-990	211	V_{REG}	2373	-990	261	V_{EE}	4725	-990
162	V_{LCD}	147	-990	212	V_{REG}	2415	-990	262	V_{EE}	4767	-990
163	V_{LCD}	189	-990	213	V_{REG}	2457	-990	263	V_{EE}	4809	-990
164	V_{LCD}	231	-990	214	V_{REG}	2499	-990	264	V_{EE}	4851	-990
165	V_{LCD}	273	-990	215	V_{REG}	2541	-990	265	V_{EE}	4893	-990
166	V_{LCD}	315	-990	216	DMY_{70}	2583	-990	266	V_{EE}	4935	-990
167	DMY_{67}	357	-990	217	V_{REF}	2625	-990	267	V_{EE}	4977	-990
168	V_1	399	-990	218	V_{REF}	2667	-990	268	V_{EE}	5019	-990
169	V_1	441	-990	219	V_{REF}	2709	-990	269	V_{EE}	5061	-990
170	V_1	483	-990	220	V_{REF}	2751	-990	270	DMY_{74}	5187	-990
171	V_1	525	-990	221	V_{REF}	2793	-990	271	C1+	5229	-990
172	V_1	567	-990	222	V_{REF}	2835	-990	272	C1+	5271	-990
173	V_1	609	-990	223	V_{REF}	2877	-990	273	C1+	5313	-990
174	V_1	651	-990	224	V_{REF}	2919	-990	274	C1+	5355	-990
175	V_1	693	-990	225	V_{REF}	2961	-990	275	C1+	5397	-990
176	V_1	735	-990	226	V_{REF}	3003	-990	276	C1+	5439	-990
177	V_2	861	-990	227	DMY_{71}	3045	-990	277	C1+	5481	-990
178	V_2	903	-990	228	V_{BA}	3087	-990	278	C1+	5523	-990
179	V_2	945	-990	229	V_{BA}	3129	-990	279	C1+	5565	-990
180	V_2	987	-990	230	V_{BA}	3171	-990	280	C1+	5607	-990
181	V_2	1029	-990	231	V_{BA}	3213	-990	281	DMY_{75}	5649	-990
182	V_2	1071	-990	232	V_{BA}	3255	-990	282	C1-	5691	-990
183	V_2	1113	-990	233	V_{BA}	3297	-990	283	C1-	5733	-990
184	V_2	1155	-990	234	V_{BA}	3339	-990	284	C1-	5775	-990
185	V_2	1197	-990	235	V_{BA}	3381	-990	285	C1-	5817	-990
186	DMY_{68}	1239	-990	236	V_{BA}	3423	-990	286	C1-	5859	-990
187	V_3	1281	-990	237	V_{BA}	3465	-990	287	C1-	5901	-990
188	V_3	1323	-990	238	DMY_{72}	3507	-990	288	C1-	5943	-990
189	V_3	1365	-990	239	V_{SS}	3549	-990	289	C1-	5985	-990
190	V_3	1407	-990	240	V_{SS}	3591	-990	290	C1-	6027	-990
191	V_3	1449	-990	241	V_{SS}	3633	-990	291	C1-	6069	-990
192	V_3	1491	-990	242	V_{SS}	3675	-990	292	DMY_{76}	6111	-990
193	V_3	1533	-990	243	V_{SS}	3717	-990	293	C2+	6153	-990
194	V_3	1575	-990	244	V_{SS}	3759	-990	294	C2+	6195	-990
195	V_3	1617	-990	245	V_{SS}	3801	-990	295	C2+	6237	-990
196	V_4	1743	-990	246	V_{SS}	3843	-990	296	C2+	6279	-990
197	V_4	1785	-990	247	V_{SS}	3885	-990	297	C2+	6321	-990
198	V_4	1827	-990	248	V_{SS}	3927	-990	298	C2+	6363	-990
199	V_4	1869	-990	249	V_{OUT}	4095	-990	299	C2+	6405	-990
200	V_4	1911	-990	250	V_{OUT}	4137	-990	300	C2+	6447	-990

■ PAD COORDINATES 3

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
301	C2+	6489	-990	351	C4-	8589	-990	401	$SEGA_3$	7665	990
302	C2+	6531	-990	352	C4-	8631	-990	402	$SEGB_3$	7623	990
303	DMY_{77}	6573	-990	353	C4-	8673	-990	403	$SEGC_3$	7581	990
304	C2-	6615	-990	354	C4-	8715	-990	404	$SEGA_4$	7539	990
305	C2-	6657	-990	355	C4-	8757	-990	405	$SEGB_4$	7497	990
306	C2-	6699	-990	356	C4-	8799	-990	406	$SEGC_4$	7455	990
307	C2-	6741	-990	357	C4-	8841	-990	407	$SEGA_5$	7413	990
308	C2-	6783	-990	358	DMY_{82}	8883	-990	408	$SEGB_5$	7371	990
309	C2-	6825	-990	359	DMY_{83}	8925	-990	409	$SEGC_5$	7329	990
310	C2-	6867	-990	360	DMY_{84}	8967	-990	410	$SEGA_6$	7287	990
311	C2-	6909	-990	361	DMY_{85}	9225	-910	411	$SEGB_6$	7245	990
312	C2-	6951	-990	362	DMY_{86}	9225	-868	412	$SEGC_6$	7203	990
313	C2-	6993	-990	363	DMY_{86}	9225	-826	413	$SEGA_7$	7161	990
314	DMY_{78}	7035	-990	364	DMY_{86}	9225	-784	414	$SEGB_7$	7119	990
315	C3+	7077	-990	365	DMY_{87}	9225	-742	415	$SEGC_7$	7077	990
316	C3+	7119	-990	366	DMY_{88}	9135	990	416	$SEGA_8$	7035	990
317	C3+	7161	-990	367	DMY_{89}	9093	990	417	$SEGB_8$	6993	990
318	C3+	7203	-990	368	DMY_{90}	9051	990	418	$SEGC_8$	6951	990
319	C3+	7245	-990	369	COM_{19}	9009	990	419	$SEGA_9$	6909	990
320	C3+	7287	-990	370	COM_{18}	8967	990	420	$SEGB_9$	6867	990
321	C3+	7329	-990	371	COM_{17}	8925	990	421	$SEGC_9$	6825	990
322	C3+	7371	-990	372	COM_{16}	8883	990	422	$SEGA_{10}$	6783	990
323	C3+	7413	-990	373	COM_{15}	8841	990	423	$SEGB_{10}$	6741	990
324	C3+	7455	-990	374	COM_{14}	8799	990	424	$SEGC_{10}$	6699	990
325	DMY_{79}	7497	-990	375	COM_{13}	8757	990	425	$SEGA_{11}$	6657	990
326	C3-	7539	-990	376	COM_{12}	8715	990	426	$SEGB_{11}$	6615	990
327	C3-	7581	-990	377	COM_{11}	8673	990	427	$SEGC_{11}$	6573	990
328	C3-	7623	-990	378	COM_{10}	8631	990	428	$SEGA_{12}$	6531	990
329	C3-	7665	-990	379	COM_9	8589	990	429	$SEGB_{12}$	6489	990
330	C3-	7707	-990	380	COM_8	8547	990	430	$SEGC_{12}$	6447	990
331	C3-	7749	-990	381	COM_7	8505	990	431	$SEGA_{13}$	6405	990
332	C3-	7791	-990	382	COM_6	8463	990	432	$SEGB_{13}$	6363	990
333	C3-	7833	-990	383	COM_5	8421	990	433	$SEGC_{13}$	6321	990
334	C3-	7875	-990	384	COM_4	8379	990	434	$SEGA_{14}$	6279	990
335	C3-	7917	-990	385	COM_3	8337	990	435	$SEGB_{14}$	6237	990
336	DMY_{80}	7959	-990	386	COM_2	8295	990	436	$SEGC_{14}$	6195	990
337	C4+	8001	-990	387	COM_1	8253	990	437	$SEGA_{15}$	6153	990
338	C4+	8043	-990	388	COM_0	8211	990	438	$SEGB_{15}$	6111	990
339	C4+	8085	-990	389	DMY_{91}	8169	990	439	$SEGC_{15}$	6069	990
340	C4+	8127	-990	390	DMY_{92}	8127	990	440	$SEGA_{16}$	6027	990
341	C4+	8169	-990	391	DMY_{93}	8085	990	441	$SEGB_{16}$	5985	990
342	C4+	8211	-990	392	$SEGA_0$	8043	990	442	$SEGC_{16}$	5943	990
343	C4+	8253	-990	393	$SEGB_0$	8001	990	443	$SEGA_{17}$	5901	990
344	C4+	8295	-990	394	$SEGC_0$	7959	990	444	$SEGB_{17}$	5859	990
345	C4+	8337	-990	395	$SEGA_1$	7917	990	445	$SEGC_{17}$	5817	990
346	C4+	8379	-990	396	$SEGB_1$	7875	990	446	$SEGA_{18}$	5775	990
347	DMY_{81}	8421	-990	397	$SEGC_1$	7833	990	447	$SEGB_{18}$	5733	990
348	C4-	8463	-990	398	$SEGA_2$	7791	990	448	$SEGC_{18}$	5691	990
349	C4-	8505	-990	399	$SEGB_2$	7749	990	449	$SEGA_{19}$	5649	990
350	C4-	8547	-990	400	$SEGC_2$	7707	990	450	$SEGB_{19}$	5607	990

■ PAD COORDINATES 4

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
451	$SEGC_{19}$	5565	990	501	$SEGB_{36}$	3465	990	551	$SEGA_{53}$	1365	990
452	$SEGA_{20}$	5523	990	502	$SEGC_{36}$	3423	990	552	$SEGB_{53}$	1323	990
453	$SEGB_{20}$	5481	990	503	$SEGA_{37}$	3381	990	553	$SEGC_{53}$	1281	990
454	$SEGC_{20}$	5439	990	504	$SEGB_{37}$	3339	990	554	$SEGA_{54}$	1239	990
455	$SEGA_{21}$	5397	990	505	$SEGC_{37}$	3297	990	555	$SEGB_{54}$	1197	990
456	$SEGB_{21}$	5355	990	506	$SEGA_{38}$	3255	990	556	$SEGC_{54}$	1155	990
457	$SEGC_{21}$	5313	990	507	$SEGB_{38}$	3213	990	557	$SEGA_{55}$	1113	990
458	$SEGA_{22}$	5271	990	508	$SEGC_{38}$	3171	990	558	$SEGB_{55}$	1071	990
459	$SEGB_{22}$	5229	990	509	$SEGA_{39}$	3129	990	559	$SEGC_{55}$	1029	990
460	$SEGC_{22}$	5187	990	510	$SEGB_{39}$	3087	990	560	$SEGA_{56}$	987	990
461	$SEGA_{23}$	5145	990	511	$SEGC_{39}$	3045	990	561	$SEGB_{56}$	945	990
462	$SEGB_{23}$	5103	990	512	$SEGA_{40}$	3003	990	562	$SEGC_{56}$	903	990
463	$SEGC_{23}$	5061	990	513	$SEGB_{40}$	2961	990	563	$SEGA_{57}$	861	990
464	$SEGA_{24}$	5019	990	514	$SEGC_{40}$	2919	990	564	$SEGB_{57}$	819	990
465	$SEGB_{24}$	4977	990	515	$SEGA_{41}$	2877	990	565	$SEGC_{57}$	777	990
466	$SEGC_{24}$	4935	990	516	$SEGB_{41}$	2835	990	566	$SEGA_{58}$	735	990
467	$SEGA_{25}$	4893	990	517	$SEGC_{41}$	2793	990	567	$SEGB_{58}$	693	990
468	$SEGB_{25}$	4851	990	518	$SEGA_{42}$	2751	990	568	$SEGC_{58}$	651	990
469	$SEGC_{25}$	4809	990	519	$SEGB_{42}$	2709	990	569	$SEGA_{59}$	609	990
470	$SEGA_{26}$	4767	990	520	$SEGC_{42}$	2667	990	570	$SEGB_{59}$	567	990
471	$SEGB_{26}$	4725	990	521	$SEGA_{43}$	2625	990	571	$SEGC_{59}$	525	990
472	$SEGC_{26}$	4683	990	522	$SEGB_{43}$	2583	990	572	$SEGA_{60}$	483	990
473	$SEGA_{27}$	4641	990	523	$SEGC_{43}$	2541	990	573	$SEGB_{60}$	441	990
474	$SEGB_{27}$	4599	990	524	$SEGA_{44}$	2499	990	574	$SEGC_{60}$	399	990
475	$SEGC_{27}$	4557	990	525	$SEGB_{44}$	2457	990	575	$SEGA_{61}$	357	990
476	$SEGA_{28}$	4515	990	526	$SEGC_{44}$	2415	990	576	$SEGB_{61}$	315	990
477	$SEGB_{28}$	4473	990	527	$SEGA_{45}$	2373	990	577	$SEGC_{61}$	273	990
478	$SEGC_{28}$	4431	990	528	$SEGB_{45}$	2331	990	578	$SEGA_{62}$	231	990
479	$SEGA_{29}$	4389	990	529	$SEGC_{45}$	2289	990	579	$SEGB_{62}$	189	990
480	$SEGB_{29}$	4347	990	530	$SEGA_{46}$	2247	990	580	$SEGC_{62}$	147	990
481	$SEGC_{29}$	4305	990	531	$SEGB_{46}$	2205	990	581	$SEGA_{63}$	105	990
482	$SEGA_{30}$	4263	990	532	$SEGC_{46}$	2163	990	582	$SEGB_{63}$	63	990
483	$SEGB_{30}$	4221	990	533	$SEGA_{47}$	2121	990	583	$SEGC_{63}$	21	990
484	$SEGC_{30}$	4179	990	534	$SEGB_{47}$	2079	990	584	$SEGA_{64}$	-21	990
485	$SEGA_{31}$	4137	990	535	$SEGC_{47}$	2037	990	585	$SEGB_{64}$	-63	990
486	$SEGB_{31}$	4095	990	536	$SEGA_{48}$	1995	990	586	$SEGC_{64}$	-105	990
487	$SEGC_{31}$	4053	990	537	$SEGB_{48}$	1953	990	587	$SEGA_{65}$	-147	990
488	$SEGA_{32}$	4011	990	538	$SEGC_{48}$	1911	990	588	$SEGB_{65}$	-189	990
489	$SEGB_{32}$	3969	990	539	$SEGA_{49}$	1869	990	589	$SEGC_{65}$	-231	990
490	$SEGC_{32}$	3927	990	540	$SEGB_{49}$	1827	990	590	$SEGA_{66}$	-273	990
491	$SEGA_{33}$	3885	990	541	$SEGC_{49}$	1785	990	591	$SEGB_{66}$	-315	990
492	$SEGB_{33}$	3843	990	542	$SEGA_{50}$	1743	990	592	$SEGC_{66}$	-357	990
493	$SEGC_{33}$	3801	990	543	$SEGB_{50}$	1701	990	593	$SEGA_{67}$	-399	990
494	$SEGA_{34}$	3759	990	544	$SEGC_{50}$	1659	990	594	$SEGB_{67}$	-441	990
495	$SEGB_{34}$	3717	990	545	$SEGA_{51}$	1617	990	595	$SEGC_{67}$	-483	990
496	$SEGC_{34}$	3675	990	546	$SEGB_{51}$	1575	990	596	$SEGA_{68}$	-525	990
497	$SEGA_{35}$	3633	990	547	$SEGC_{51}$	1533	990	597	$SEGB_{68}$	-567	990
498	$SEGB_{35}$	3591	990	548	$SEGA_{52}$	1491	990	598	$SEGC_{68}$	-609	990
499	$SEGC_{35}$	3549	990	549	$SEGB_{52}$	1449	990	599	$SEGA_{69}$	-651	990
500	$SEGA_{36}$	3507	990	550	$SEGC_{52}$	1407	990	600	$SEGB_{69}$	-693	990

■ PAD COORDINATES 5

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

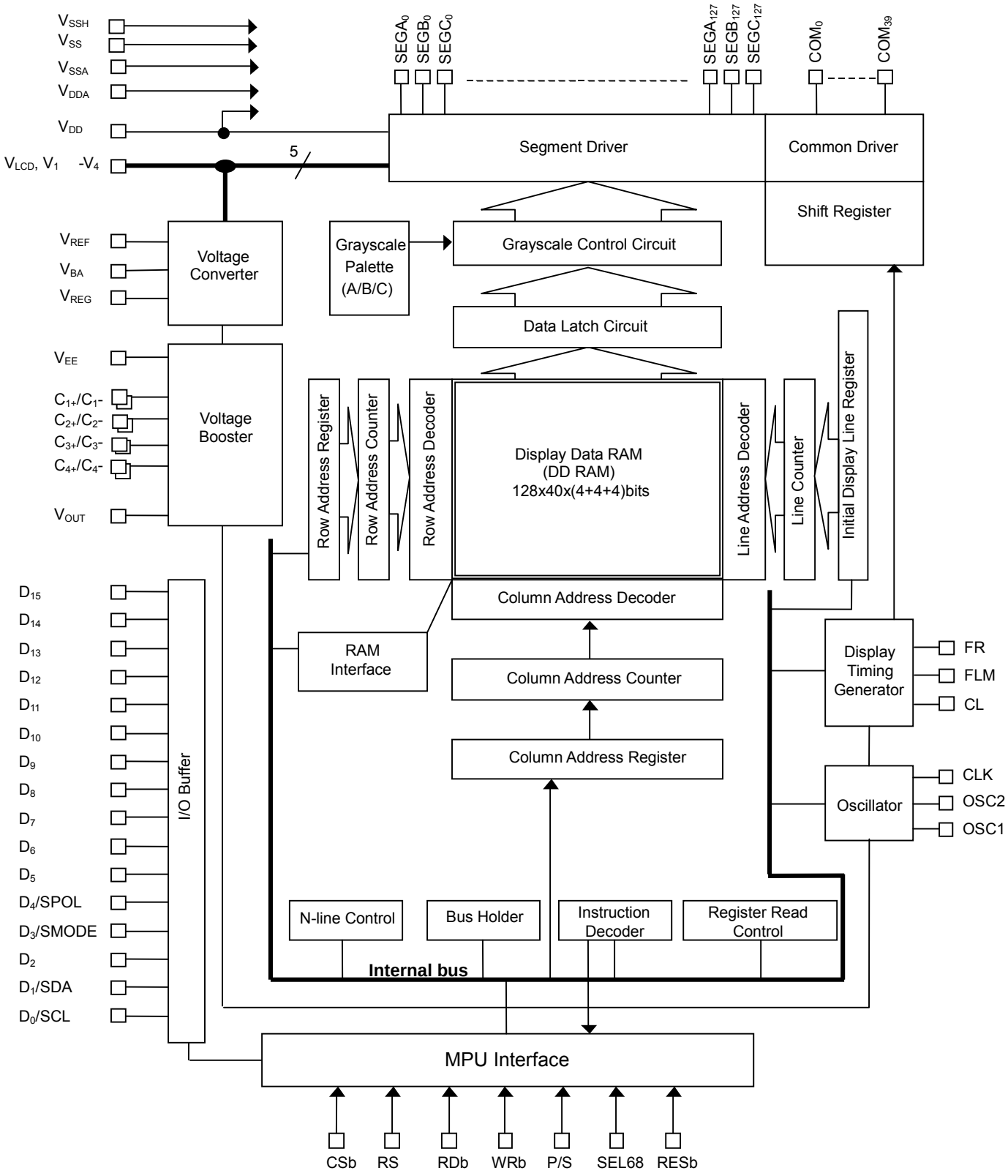
No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
601	$SEGC_{69}$	-735	990	651	$SEGB_{86}$	-2835	990	701	$SEGA_{103}$	-4935	990
602	$SEGA_{70}$	-777	990	652	$SEGC_{86}$	-2877	990	702	$SEGB_{103}$	-4977	990
603	$SEGB_{70}$	-819	990	653	$SEGA_{87}$	-2919	990	703	$SEGC_{103}$	-5019	990
604	$SEGC_{70}$	-861	990	654	$SEGB_{87}$	-2961	990	704	$SEGA_{104}$	-5061	990
605	$SEGA_{71}$	-903	990	655	$SEGC_{87}$	-3003	990	705	$SEGB_{104}$	-5103	990
606	$SEGB_{71}$	-945	990	656	$SEGA_{88}$	-3045	990	706	$SEGC_{104}$	-5145	990
607	$SEGC_{71}$	-987	990	657	$SEGB_{88}$	-3087	990	707	$SEGA_{105}$	-5187	990
608	$SEGA_{72}$	-1029	990	658	$SEGC_{88}$	-3129	990	708	$SEGB_{105}$	-5229	990
609	$SEGB_{72}$	-1071	990	659	$SEGA_{89}$	-3171	990	709	$SEGC_{105}$	-5271	990
610	$SEGC_{72}$	-1113	990	660	$SEGB_{89}$	-3213	990	710	$SEGA_{106}$	-5313	990
611	$SEGA_{73}$	-1155	990	661	$SEGC_{89}$	-3255	990	711	$SEGB_{106}$	-5355	990
612	$SEGB_{73}$	-1197	990	662	$SEGA_{90}$	-3297	990	712	$SEGC_{106}$	-5397	990
613	$SEGC_{73}$	-1239	990	663	$SEGB_{90}$	-3339	990	713	$SEGA_{107}$	-5439	990
614	$SEGA_{74}$	-1281	990	664	$SEGC_{90}$	-3381	990	714	$SEGB_{107}$	-5481	990
615	$SEGB_{74}$	-1323	990	665	$SEGA_{91}$	-3423	990	715	$SEGC_{107}$	-5523	990
616	$SEGC_{74}$	-1365	990	666	$SEGB_{91}$	-3465	990	716	$SEGA_{108}$	-5565	990
617	$SEGA_{75}$	-1407	990	667	$SEGC_{91}$	-3507	990	717	$SEGB_{108}$	-5607	990
618	$SEGB_{75}$	-1449	990	668	$SEGA_{92}$	-3549	990	718	$SEGC_{108}$	-5649	990
619	$SEGC_{75}$	-1491	990	669	$SEGB_{92}$	-3591	990	719	$SEGA_{109}$	-5691	990
620	$SEGA_{76}$	-1533	990	670	$SEGC_{92}$	-3633	990	720	$SEGB_{109}$	-5733	990
621	$SEGB_{76}$	-1575	990	671	$SEGA_{93}$	-3675	990	721	$SEGC_{109}$	-5775	990
622	$SEGC_{76}$	-1617	990	672	$SEGB_{93}$	-3717	990	722	$SEGA_{110}$	-5817	990
623	$SEGA_{77}$	-1659	990	673	$SEGC_{93}$	-3759	990	723	$SEGB_{110}$	-5859	990
624	$SEGB_{77}$	-1701	990	674	$SEGA_{94}$	-3801	990	724	$SEGC_{110}$	-5901	990
625	$SEGC_{77}$	-1743	990	675	$SEGB_{94}$	-3843	990	725	$SEGA_{111}$	-5943	990
626	$SEGA_{78}$	-1785	990	676	$SEGC_{94}$	-3885	990	726	$SEGB_{111}$	-5985	990
627	$SEGB_{78}$	-1827	990	677	$SEGA_{95}$	-3927	990	727	$SEGC_{111}$	-6027	990
628	$SEGC_{78}$	-1869	990	678	$SEGB_{95}$	-3969	990	728	$SEGA_{112}$	-6069	990
629	$SEGA_{79}$	-1911	990	679	$SEGC_{95}$	-4011	990	729	$SEGB_{112}$	-6111	990
630	$SEGB_{79}$	-1953	990	680	$SEGA_{96}$	-4053	990	730	$SEGC_{112}$	-6153	990
631	$SEGC_{79}$	-1995	990	681	$SEGB_{96}$	-4095	990	731	$SEGA_{113}$	-6195	990
632	$SEGA_{80}$	-2037	990	682	$SEGC_{96}$	-4137	990	732	$SEGB_{113}$	-6237	990
633	$SEGB_{80}$	-2079	990	683	$SEGA_{97}$	-4179	990	733	$SEGC_{113}$	-6279	990
634	$SEGC_{80}$	-2121	990	684	$SEGB_{97}$	-4221	990	734	$SEGA_{114}$	-6321	990
635	$SEGA_{81}$	-2163	990	685	$SEGC_{97}$	-4263	990	735	$SEGB_{114}$	-6363	990
636	$SEGB_{81}$	-2205	990	686	$SEGA_{98}$	-4305	990	736	$SEGC_{114}$	-6405	990
637	$SEGC_{81}$	-2247	990	687	$SEGB_{98}$	-4347	990	737	$SEGA_{115}$	-6447	990
638	$SEGA_{82}$	-2289	990	688	$SEGC_{98}$	-4389	990	738	$SEGB_{115}$	-6489	990
639	$SEGB_{82}$	-2331	990	689	$SEGA_{99}$	-4431	990	739	$SEGC_{115}$	-6531	990
640	$SEGC_{82}$	-2373	990	690	$SEGB_{99}$	-4473	990	740	$SEGA_{116}$	-6573	990
641	$SEGA_{83}$	-2415	990	691	$SEGC_{99}$	-4515	990	741	$SEGB_{116}$	-6615	990
642	$SEGB_{83}$	-2457	990	692	$SEGA_{100}$	-4557	990	742	$SEGC_{116}$	-6657	990
643	$SEGC_{83}$	-2499	990	693	$SEGB_{100}$	-4599	990	743	$SEGA_{117}$	-6699	990
644	$SEGA_{84}$	-2541	990	694	$SEGC_{100}$	-4641	990	744	$SEGB_{117}$	-6741	990
645	$SEGB_{84}$	-2583	990	695	$SEGA_{101}$	-4683	990	745	$SEGC_{117}$	-6783	990
646	$SEGC_{84}$	-2625	990	696	$SEGB_{101}$	-4725	990	746	$SEGA_{118}$	-6825	990
647	$SEGA_{85}$	-2667	990	697	$SEGC_{101}$	-4767	990	747	$SEGB_{118}$	-6867	990
648	$SEGB_{85}$	-2709	990	698	$SEGA_{102}$	-4809	990	748	$SEGC_{118}$	-6909	990
649	$SEGC_{85}$	-2751	990	699	$SEGB_{102}$	-4851	990	749	$SEGA_{119}$	-6951	990
650	$SEGA_{86}$	-2793	990	700	$SEGC_{102}$	-4893	990	750	$SEGB_{119}$	-6993	990

■ PAD COORDINATES 6

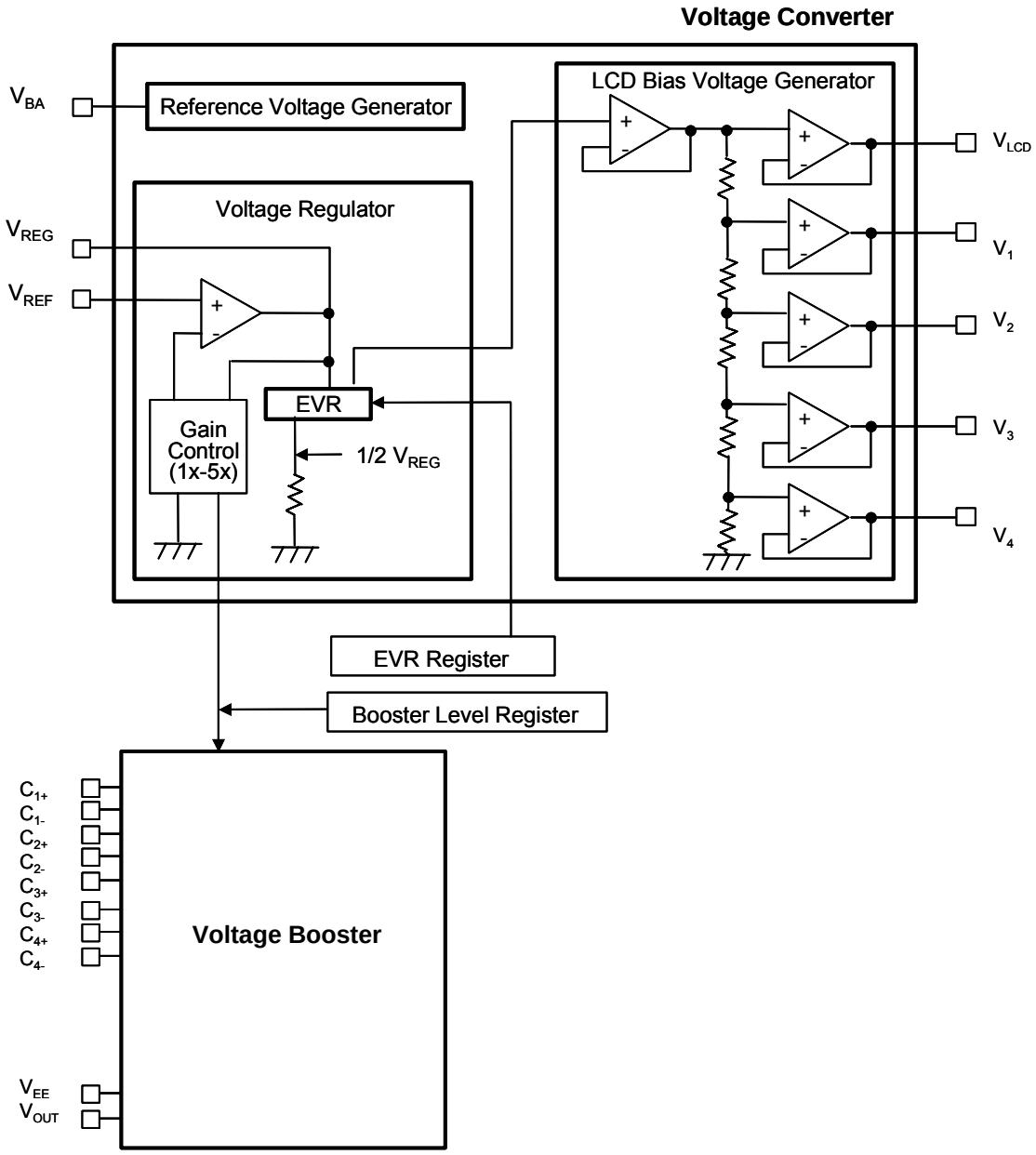
Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)	No.	PAD Name	X(μm)	Y(μm)
751	$SEGC_{119}$	-7035	990	801	DMY_{99}	-9135	990				
752	$SEGA_{120}$	-7077	990	802	DMY_{100}	-9225	-742				
753	$SEGB_{120}$	-7119	990	803	DMY_{101}	-9225	-784				
754	$SEGC_{120}$	-7161	990	804	DMY_{101}	-9225	-826				
755	$SEGA_{121}$	-7203	990	805	DMY_{101}	-9225	-868				
756	$SEGB_{121}$	-7245	990	806	DMY_{102}	-9225	-910				
757	$SEGC_{121}$	-7287	990								
758	$SEGA_{122}$	-7329	990								
759	$SEGB_{122}$	-7371	990								
760	$SEGC_{122}$	-7413	990								
761	$SEGA_{123}$	-7455	990								
762	$SEGB_{123}$	-7497	990								
763	$SEGC_{123}$	-7539	990								
764	$SEGA_{124}$	-7581	990								
765	$SEGB_{124}$	-7623	990								
766	$SEGC_{124}$	-7665	990								
767	$SEGA_{125}$	-7707	990								
768	$SEGB_{125}$	-7749	990								
769	$SEGC_{125}$	-7791	990								
770	$SEGA_{126}$	-7833	990								
771	$SEGB_{126}$	-7875	990								
772	$SEGC_{126}$	-7917	990								
773	$SEGA_{127}$	-7959	990								
774	$SEGB_{127}$	-8001	990								
775	$SEGC_{127}$	-8043	990								
776	DMY_{94}	-8085	990								
777	DMY_{95}	-8127	990								
778	DMY_{96}	-8169	990								
779	COM_{20}	-8211	990								
780	COM_{21}	-8253	990								
781	COM_{22}	-8295	990								
782	COM_{23}	-8337	990								
783	COM_{24}	-8379	990								
784	COM_{25}	-8421	990								
785	COM_{26}	-8463	990								
786	COM_{27}	-8505	990								
787	COM_{28}	-8547	990								
788	COM_{29}	-8589	990								
789	COM_{30}	-8631	990								
790	COM_{31}	-8673	990								
791	COM_{32}	-8715	990								
792	COM_{33}	-8757	990								
793	COM_{34}	-8799	990								
794	COM_{35}	-8841	990								
795	COM_{36}	-8883	990								
796	COM_{37}	-8925	990								
797	COM_{38}	-8967	990								
798	COM_{39}	-9009	990								
799	DMY_{97}	-9051	990								
800	DMY_{98}	-9093	990								

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function
111-121	V_{DD}	Power	Power Supply for Logic Circuits
146-156	V_{SS}	Power	GND for Logic Circuits
239-248	V_{SSH}	Power	GND for High Voltage Circuits
10,11, 42,43,	V_{DDA}	Power	V_{DDA} is internally connected to V_{DD} to fix SEL68 or P/S to "H" if necessary, and cannot be used as main power supply. • V_{DDA} should be open if not used.
4,5, 16,17, 76,77,	V_{SSA}	Power	V_{SSA} is internally connected to V_{SS} to fix SEL68 or P/S to "L" if necessary, and cannot be used as main GND. • V_{SSA} should be open if not used.
158-166 168-176 177-185 187-195 196-204	V_{LCD} V_1 V_2 V_3 V_4	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V_{LCD} and V_1-V_4) are activated by the "Power Control" instruction. Stabilizing capacitors are required between each bias voltage and V_{SS}. • When the external LCD power supply is used, LCD bias voltages are externally supplied on V_{LCD}, V_1, V_2, V_3 and V_4 individually, with the following relation maintained: $V_{SSH}<V_4<V_3<V_2<V_1<V_{LCD}$
271-280 282-291	C_{1+} C_{1-}	Power	Capacitor Connection for Voltage Booster
293-302 304-313	C_{2+} C_{2-}	Power	Capacitor Connection for Voltage Booster
315-324 326-335	C_{3+} C_{3-}	Power	Capacitor Connection for Voltage Booster
337-346 348-357	C_{4+} C_{4-}	Power	Capacitor Connection for Voltage Booster
228-237	V_{BA}	Power	Reference-Voltage Generator Output
217-226	V_{REF}	Power	Voltage Regulator Input
260-269	V_{EE}	Power	Voltage Booster Input • V_{EE} is normally connected to V_{DD}.
249-258	V_{OUT}	Power	Voltage Booster Output • Input if an external LCD power supply is used.
19,20	RESb	I	Reset • Active "L"
206-215	V_{REG}	Power	Voltage Regulator Output
7,8	SEL68	I	MPU Mode Select SEL86 | H | L MPU | 68-series | 80-series

■ TERMINAL DESCRIPTION 2

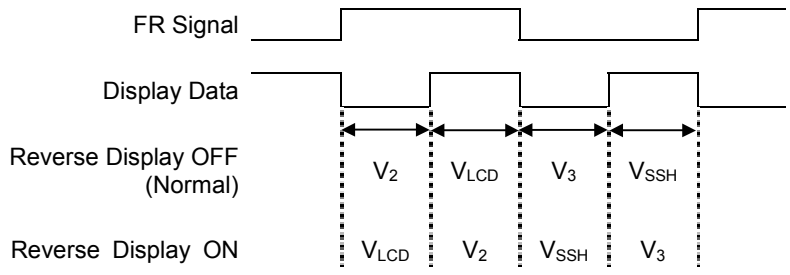
<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Function</th></tr>
<tr><td>45,46</td><td>D_0
/SCL</td><td>I/O</td><td rowspan="4">Parallel Interface
D_7 to D_0 : 8-bit Bi-directional Bus

• In the parallel interface mode (P/S=“H”), D_7-D_0 are connected to 8-bit bi-directional MPU bus.

Serial Interface
SDA : Serial Data
SCL : Serial Clock
SMODE : 3-/4-line Serial Mode Select
SPOL : RS Polarity Select (3-line Serial Interface Mode)

• In the 3 or 4-line serial interface mode (P/S=“L”), D_0 is assigned to SCL, and D_1 to SDA.
• In the 3-line serial interface mode, D_4 is assigned to SPOL.
• Serial data on SDA is latched at the rising edge of SCL signal in order of D_7, D_6,… and D_0, and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL.
• SCL should be set to “L” right after data transmission or during non-access.</td></tr>
<tr><td>49,50</td><td>D_1
/SDA</td><td>I/O</td></tr>
<tr><td>57,58</td><td>D_3
/SMODE</td><td>I/O</td></tr>
<tr><td>61,62</td><td>D_4
/SPOL</td><td>I/O</td></tr>
<tr><td>53,54
65,66
69,70
73,74</td><td>D_2
D_5
D_6
D_7</td><td>I/O</td></tr>
<tr><td>79,80
83,84
87,88
91,92
95,96
99,100
103,104
107,108</td><td>D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}</td><td>I/O</td><td>8-bit Bi-directional Bus
• In the 16-bit bus length mode, D_{15}-D_8 are assigned to upper 8-bit data bus.
• In the serial interface mode or the 8-bit parallel interface mode, D_{15}-D_8 should be fixed to “H” or “L”.</td></tr>
<tr><td>24,25</td><td>CSb</td><td>I</td><td>Chip Select
• Active “L”</td></tr>
<tr><td>29,30</td><td>RS</td><td>I</td><td>Register Select
• This signal interprets transferred data as display data or instruction.
<table><tr><th>RS</th><th>H</th><th>L</th></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table></td></tr>
<tr><td>39,40</td><td>RDb (E)</td><td>I</td><td>80-series MPU Interface (P/S=“H”, SEL68=“L”)
Data Read (RDb) Signal
• Active “L”
68-series MPU Interface (P/S=“H”, SEL68=“H”)
Enable Signal
• Active “H”</td></tr>
<tr><td>34,35</td><td>WRb (R/W)</td><td>I</td><td>80-series MPU Interface (P/S=“H”, SEL68=“L”)
Data Write (WRb) Signal
• Active “L”
68-series MPU Interface (P/S=“H”, SEL68=“H”)
Data Read or Write (R/W) Signal
<table><tr><th>R/W</th><th>H</th><th>L</th></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table></td></tr>
</table>

■ TERMINAL DESCRIPTION 3

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Function</th></tr>
<tr><td>13,14</td><td>P/S</td><td>I</td><td>Parallel/Serial Interface Mode Select
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>CSb</td><td>RS</td><td>D_0 ~ D_7</td><td>RDb, WRb</td><td>-</td></tr>
<tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D_1)</td><td>Write Only</td><td>SCL (D_0)</td></tr>
</table>
• In the serial interface mode (P/S=“L”), RDb, WRb, D_2 and D_5-D_{15} should be fixed to “H” or “L”,.</td></tr>
<tr><td>124,125</td><td>CL</td><td>O</td><td>Line Clock
• CL is normally open.</td></tr>
<tr><td>128,129</td><td>FLM</td><td>O</td><td>First Line Maker
• FLM is normally open.</td></tr>
<tr><td>132,133</td><td>FR</td><td>O</td><td>Frame Rate
• FR is normally open.</td></tr>
<tr><td>136,137</td><td>CLK</td><td>O</td><td>Clock Output
• CLK is normally open.</td></tr>
<tr><td>140,141
143,144</td><td>OSC1
OSC2</td><td>I
O</td><td>OSC
• When the internal oscillator is used, fix OSC1 to “H” or “L” and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor.
• When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.</td></tr>
<tr><td>392-775</td><td>$SEGA_0$ ~$SEGA_{127}$
$SEGB_0$ ~$SEGB_{127}$
$SEGC_0$ ~$SEGC_{127}$</td><td>O</td><td>Segment Drivers
<table>
<tr><th>REV Register</th><th>OFF</th><th>ON</th></tr>
<tr><td>Normal</td><td>0</td><td>1</td></tr>
<tr><td>Reverse</td><td>1</td><td>0</td></tr>
</table>
• Segment drivers output the following voltage levels.
<u>B/W Mode (Example)</u>

</td></tr>
<tr><td>369-388,
779-798,</td><td>COM_0 ~ COM_{40}</td><td>O</td><td>Common Drivers
• Common drivers output the following voltage levels.
<table>
<tr><th>Data</th><th>FR</th><th>Output Levels</th></tr>
<tr><td>H</td><td>H</td><td>V_{SSH}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>V_{LCD}</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
</table></td></tr>
</table>

NOTE) DUMMY PADs: No. 1-3, 12, 18, 21-23, 26-28, 31-33, 36-38, 41, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 81, 82, 85, 86, 89, 90, 93, 94, 97, 98, 101, 102, 105, 106, 109, 110, 122, 123, 126, 127, 130, 131, 134, 135, 138, 139, 142, 145, 157, 167, 186, 205, 216, 227, 238, 259, 270, 281, 292, 314, 325, 336, 347, 358-368, 389-391, 776-778, 799-806.

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) " -" : Fix to "H" or "L".

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D_7-D_0 (D_{15}-D_0)
L	80-series MPU	CSb	RS	RDb	WRb	D_7-D_0 (D_{15}-D_0)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is inactive (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D_7, D_6,…, and D_0, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb="H") temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

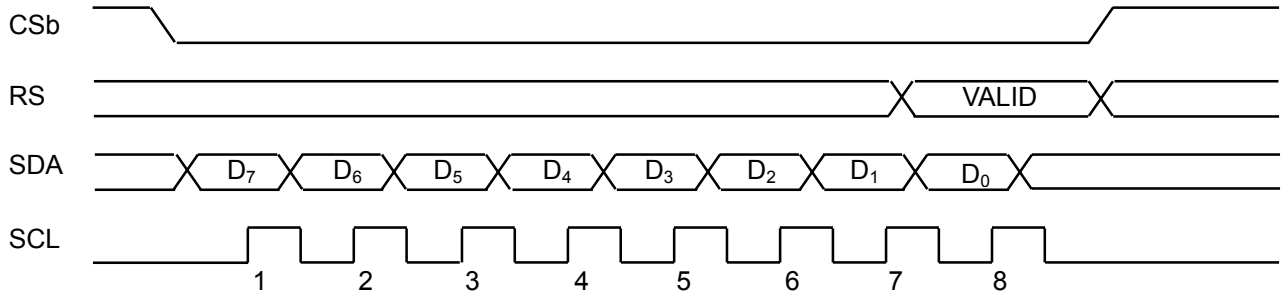


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is not active (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D_7, D_6,…, and D_0, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9^{th} SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb="H") temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

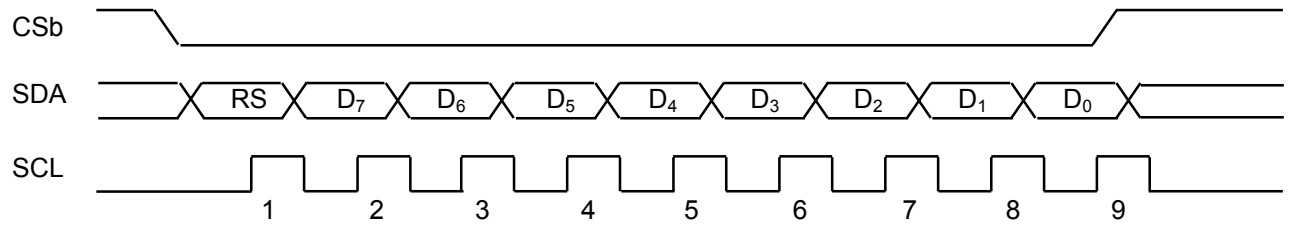


Fig 2 3-line Serial Interface Timing

(1-7) Accessing DDRAM

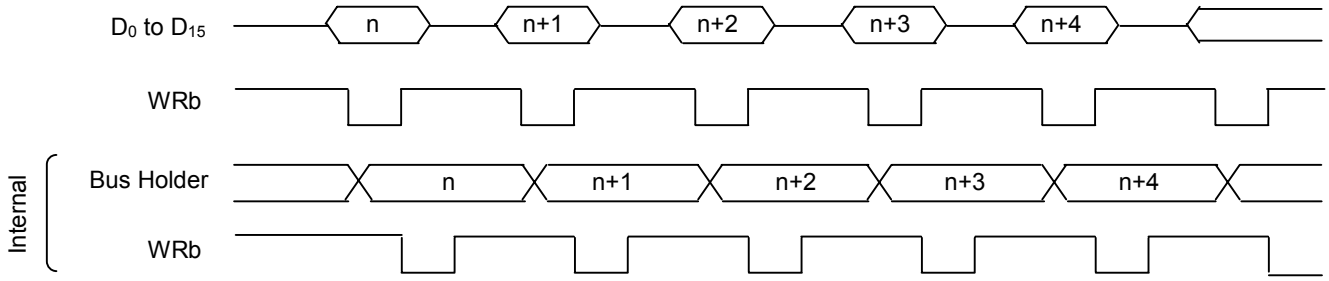
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

Display Data Write Operation



Display Data Read Operation

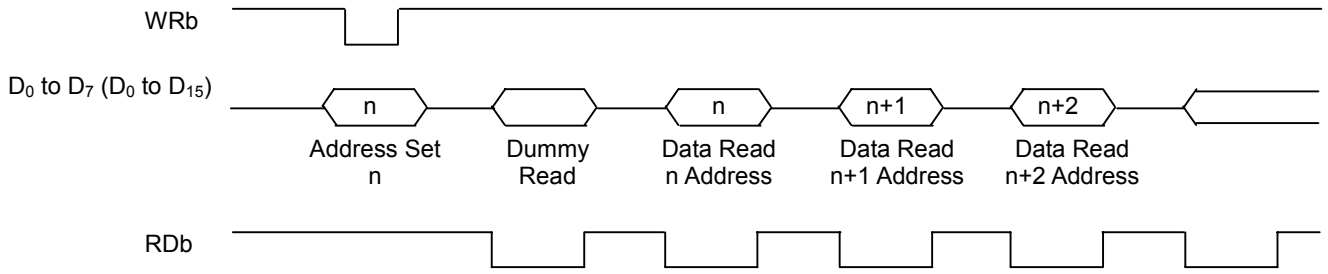


Fig 3 Internal-signal Timing of Display Data Read/Write Operations

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

(1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the "Register Address" and "Register Read" instructions. For more information, refer to "(14-23) Register Address" and "(14-24) Register Read".

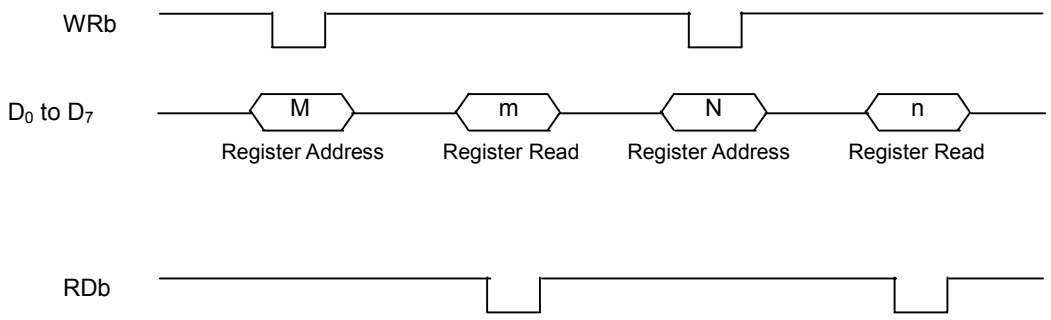


Fig 4 Access Timing of Instruction Register

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D_0 (WLS) bit of the "Bus Length" instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D_{15} to D_0). However, only lower 8 bits (D_7 to D_0) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D_{15} to D_0) are transmitted for DDRAM access. For more information, refer to "(4-4) Bit Assignment of Display Data".

Table 8 Selection of 8-/16-bit Bus Length Mode

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

(2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the "Initial COM" instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes "H". At the rising edge of the CL signal, the line counter is counted-up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers Ai, Bi and Ci (i=0 to 127) generate LCD waveforms.

(3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

(4) DDRAM

(4-1) DDRAM Address Range

The DDRAM is capable of 40 bits for row address and 1,536 bits (12-bit x 128-segment) for column address. The range of the column address is varied depending on the settings as follows, and the row address is from (00H) to (27H). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

8-bit Bus Length

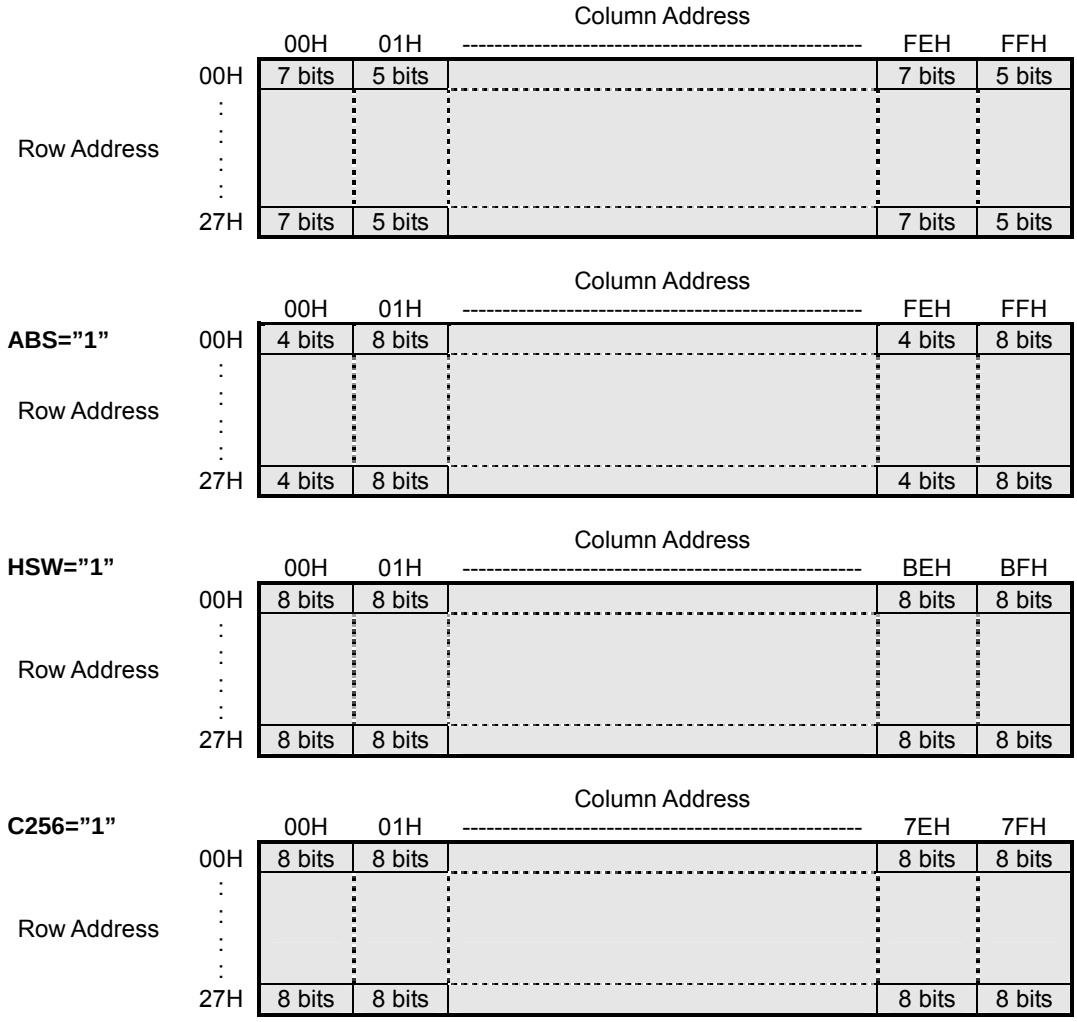


Fig 5 Range of Column Address in 8-bit Bus Length

16-bit Bus Length

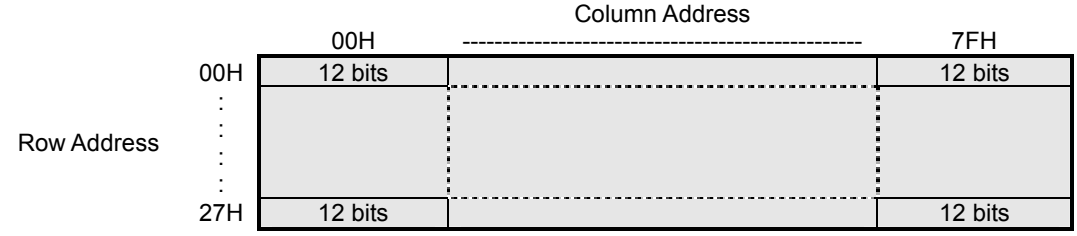


Fig 6 Range of Column Address in 16-bit Bus Length

(4-2) Window Area for DDRAM Access

In addition to the normal DDRAM access discussed previously, the window area access can be used. This area is set by the "Increment Control" instruction and the designation of the start point and the end point.

By the "Increment Control", auto-increment is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up , whenever the DDRAM is accessed. And, the start point is specified by the "Column Address" and "Row Address" instructions, and the end point by the "Window End Column Address" and "Window End Row Address" instructions. For more information, refer to "(14-9) Increment Control", "(14-25) Window End Column Address" and "(14-26)Window End Row Address". The typical sequence of the window area setting is listed below.

1. Set "1" at D_3 (WIN), D_1 (AYI) and D_0 (AXI) of "Increment Control" instruction.
2. Set start point by "Column Address" and "Row Address" instructions.
3. Set end point by "Window End Column Address" and "Window End Row Address" instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.

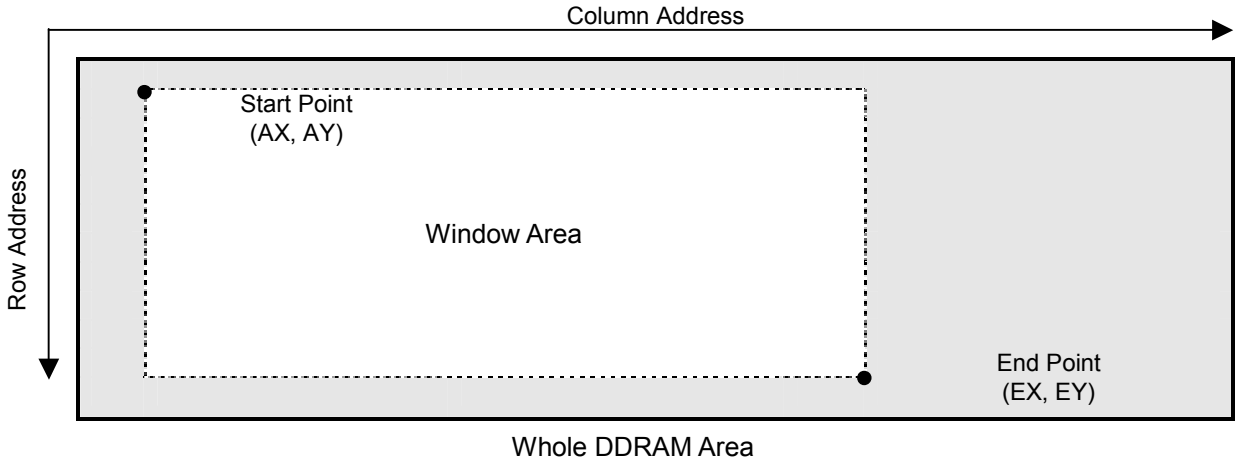
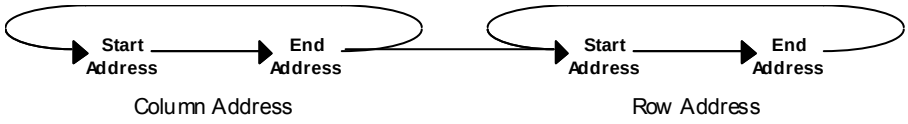


Fig 7 Window Area

NOTE1) The following relation should be maintained to avoid malfunctions.
- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE3) Auto-increment in the window area



NOTE2) A read-modify-write operation is enabled by setting "1" at the D_2 (AIM) of the "Increment Control" instruction. Refer to the description about "AIM" bit in "(14-9) Increment Control".

(4-3) Segment Direction

The DDRAM access direction is controlled by the D_0 (REF) bit of the "Display Control (2)" instruction. This function is used to reverse the segment direction for reducing the restrictions on the IC position of an LCD module.

(4-4) Bit Assignment of Display Data

(4-4-1) Bit Assignment Overview

These maps is used for grasping general outlines of the variations in the bit assignment of display data.

Table 9-1 RAM MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	HSW	REF	C256	SEG$_0$												SEG$_1$											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
16bit	1	0	x	0	0	X=00H												X=01H											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	0	x	1	0	X=7FH												X=7EH											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	1	x	0	0	X=00H												X=01H											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	1	1	x	1	0	X=7FH												X=7EH											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
8bit	0	0	0	0	0	X=00H							X=01H					X=02H							X=03H				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	0	0	1	0	X=FEH							X=FFH					X=FCH							X=FDH				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	1	0	0	0	X=00H				X=01H								X=02H				X=03H							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	1	0	1	0	X=FEH				X=FFH								X=FCH				X=FDH							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	0	0	X=00H								X=01H								X=02H							
						D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	1	0	X=BEH(L)				X=BFH								X=BDH								X=BEH(H)			
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4

Mode	WLS	ABS	HSW	REF	C256	SEG$_{126}$												SEG$_{127}$											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
16bit	1	0	x	0	0	X=7EH												X=7FH											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	0	x	1	0	X=01H												X=00H											
						D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
	1	1	x	0	0	X=7EH												X=7FH											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	1	1	x	1	0	X=01H												X=00H											
						D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
8bit	0	0	0	0	0	X=FCH							X=FDH					X=FEH							X=FFH				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	0	0	1	0	X=02H							X=03H					X=00H							X=01H				
						D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
	0	1	0	0	0	X=FCH				X=FDH								X=FEH				X=FFH							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	1	0	1	0	X=02H				X=03H								X=00H				X=01H							
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	0	0	X=BDH								X=BEH								X=BFH							
						D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	1	1	0	X=01H(L)				X=02H								X=00H								X=01H(H)			
						D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4

Table 9-2 RAM MAP 2 (Variable 8-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	HSW	REF	C256	SEG$_0$												SEG$_1$											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
8 bit	0	x	x	0	1	X=00H												X=01H											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	x	1	1	X=7FH												X=7EH											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Mode	WLS	ABS	HSW	REF	C256	SEG$_{126}$												SEG$_{127}$											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
8 bit	0	x	x	0	1	X=7EH												X=7FH											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	0	x	x	1	1	X=01H												X=00H											
						-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-	-	-	-	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Table 10 SWAP

SWAP	SWAP	Palette A				Palette B				Palette C			
		A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_3	C_2	C_1	C_0
0	0	SEGAx				SEGBx				SEGCx			
1	1												
0	1	SEGCx				SEGBx				SEGAx			
1	0												

NOTE1) On the RAM MAP 2, A_0, B_0, C_1 and C_0 bits are fixed to “1”.
NOTE2) The functions of the variable 8-grayscale mode are different from those of the fixed 8-grayscale mode.
NOTE3) The contents of the DDRAM at “C256=0” are not compatible with the contents at “C256=1”.
NOTE4) “C256=1” can be used in the 8-bit bus length mode, but not in the 16-bit bus length mode.

(4-4-2) Bit Assignment in Variable 16-grayscale Mode

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	0	X=00H	←→	X=7FH
*	0	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	1	X=00H	←→	X=7FH
*	0	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	0	X=00H	←→	X=7FH
*	1	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	1	X=00H	←→	X=7FH
*	1	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	0	0	0	X=00H							X=01H					⟷	X=FEH							X=FFH							
0	0	1	1	X=FEH							X=FFH					⟷	X=00H							X=01H							
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	⟷	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
Grayscale Palette				Palette A				Palette B			Palette C					⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGA_0$				$SEGB_0$			$SEGC_0$					⟷	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	0	0	1	X=00H							X=01H					⟷	X=FEH							X=FFH							
0	0	1	0	X=FEH							X=FFH					⟷	X=00H							X=01H							
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	⟷	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1					
Grayscale Palette				Palette A				Palette B			Palette C					⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGC_0$				$SEGB_0$			$SEGA_0$					⟷	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	1	0	0	X=00H							X=01H					⟷	X=FEH							X=FFH							
0	1	1	1	X=FEH							X=FFH					⟷	X=00H							X=01H							
Display Data in DDRAM				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	⟷	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					
Grayscale Palette				Palette A				Palette B			Palette C					⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGA_0$				$SEGB_0$			$SEGC_0$					⟷	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$								

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																											
0	1	0	1	X=00H							X=01H					⟷	X=FEH							X=FFH							
0	1	1	0	X=FEH							X=FFH					⟷	X=00H							X=01H							
Display Data in DDRAM				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	⟷	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0					
Grayscale Palette				Palette A				Palette B			Palette C					⟷	Palette A				Palette B			Palette C								
Segment Driver				$SEGC_0$				$SEGB_0$			$SEGA_0$					⟷	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$								

HSW	ABS	REF	SWAP
1	*	0	0

Column Address / Display Data / Segment Driver																																
X=00H								X=01H								X=02H								..								
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…							
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…							

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP
1	*	0	1

Column Address / Display Data / Segment Driver																																
X=00H								X=01H								X=02H								..								
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…							
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…							

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	0

Column Address / Display Data / Segment Driver																																
X=BEH				X=BFH								X=BDH								X=BEH				..								
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…							
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…							

Column Address / Display Data / Segment Driver																								
…	X=01H				X=02H								X=00H								X=01H			
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	1

Column Address / Display Data / Segment Driver																																
X=BEH				X=BFH								X=BDH								X=BEH				..								
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…								
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…							
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…							

Column Address / Display Data / Segment Driver																								
…	X=01H				X=02H								X=00H								X=01H			
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

(4-4-3) Bit Assignment in Variable 8-level Gradation Mode

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
*	*	0	0	X=00H								←→	X=7FH						
*	*	1	1	X=7FH								←→	X=00H						
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
*	*	0	1	X=00H								←→	X=7FH						
*	*	1	0	X=7FH								←→	X=00H						
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

(4-4-4) Bit Assignment in Fixed 8-level Gradation Mode

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	0	X=00H	←→	X=7FH
*	0	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	0	0	1	X=00H	←→	X=7FH
*	0	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	0	X=00H	←→	X=7FH
*	1	1	1	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver		
*	1	0	1	X=00H	←→	X=7FH
*	1	1	0	X=7FH	←→	X=00H

Display Data in DDRAM	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette	Palette A				Palette B				Palette C				←→	Palette A				Palette B				Palette C			
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver					
0	0	0	0	X=00H	X=01H	←→	X=FEH	X=FFH	
0	0	1	1	X=FEH	X=FFH	←→	X=00H	X=01H	
Display Data in DDRAM				D_7 D_6 D_5 D_4 D_2 D_1 D_0	D_7 D_4 D_3 D_2 D_1	←→	D_7 D_6 D_5 D_4 D_2 D_1 D_0	D_7 D_4 D_3 D_2 D_1	
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	←→	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver					
0	0	0	1	X=00H	X=01H	←→	X=FEH	X=FFH	
0	0	1	0	X=FEH	X=FFH	←→	X=00H	X=01H	
Display Data in DDRAM				D_7 D_6 D_5 D_4 D_2 D_1 D_0	D_7 D_4 D_3 D_2 D_1	←→	D_7 D_6 D_5 D_4 D_2 D_1 D_0	D_7 D_4 D_3 D_2 D_1	
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	←→	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver					
0	1	0	0	X=00H	X=01H	←→	X=FEH	X=FFH	
0	1	1	1	X=FEH	X=FFH	←→	X=00H	X=01H	
Display Data in DDRAM				D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0		←→	D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0		
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	←→	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver					
0	1	0	1	X=00H	X=01H	←→	X=FEH	X=FFH	
0	1	1	0	X=FEH	X=FFH	←→	X=00H	X=01H	
Display Data in DDRAM				D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0		←→	D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0		
Grayscale Palette				Palette A	Palette B	Palette C	←→	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	←→	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

NOTE) The data indicated with a slash mark (/) is invalid.

HSW	ABS	REF	SWAP
1	*	0	0

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP
1	*	0	1

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	0

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$				

HSW	ABS	REF	SWAP
1	*	1	1

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$				

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
*	*	0	0	X=00H								←→	X=7FH						
*	*	1	1	X=7FH								←→	X=00H						
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver															
*	*	0	1	X=00H								←→	X=7FH						
*	*	1	0	X=7FH								←→	X=00H						
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C	
Segment Driver				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

(4-4-5) Bit Assignment in B&W Mode

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	0	0	0	X=00H	⟷	X=7FH				
*	0	1	1	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1	⟷	D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	⟷	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	0	0	1	X=00H	⟷	X=7FH				
*	0	1	0	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1	⟷	D_{15} D_{14} D_{13} D_{12} / D_{10} D_9 D_8 D_7 / D_4 D_3 D_2 D_1				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	⟷	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	1	0	0	X=00H	⟷	X=7FH				
*	1	1	1	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0	⟷	D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	⟷	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver						
*	1	0	1	X=00H	⟷	X=7FH				
*	1	1	0	X=7FH	⟷	X=00H				
Display Data in DDRAM				D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0	⟷	D_{11} D_{10} D_9 D_8 / D_7 D_6 D_5 D_4 / D_3 D_2 D_1 D_0				
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	⟷	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	0	0	0	X=00H	X=01H	⟷	X=FEH	X=FFH			
0	0	1	1	X=FEH	X=FFH	⟷	X=00H	X=01H			
Display Data in DDRAM				D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1	⟷	D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1			
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C	
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	⟷	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	0	0	1	X=00H	X=01H	⟷	X=FEH	X=FFH			
0	0	1	0	X=FEH	X=FFH	⟷	X=00H	X=01H			
Display Data in DDRAM				D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1	⟷	D_7 D_6 D_5 D_4 D_2 D_1 D_0 D_7	D_4 D_3 D_2 D_1			
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C	
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	⟷	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	1	0	0	X=00H	X=01H	⟷	X=FEH	X=FFH			
0	1	1	1	X=FEH	X=FFH	⟷	X=00H	X=01H			
Display Data in DDRAM				D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0	⟷	D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0			
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C	
Segment Driver				$SEGA_0$	$SEGB_0$	$SEGC_0$	⟷	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver							
0	1	0	1	X=00H	X=01H	⟷	X=FEH	X=FFH			
0	1	1	0	X=FEH	X=FFH	⟷	X=00H	X=01H			
Display Data in DDRAM				D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0	⟷	D_3 D_2 D_1 D_0 D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0			
Grayscale Palette				Palette A	Palette B	Palette C	⟷	Palette A	Palette B	Palette C	
Segment Driver				$SEGC_0$	$SEGB_0$	$SEGA_0$	⟷	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$	

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

HSW	ABS	REF	SWAP
1	*	0	0

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP
1	*	0	1

Column Address / Display Data / Segment Driver																								
X=00H								X=01H								X=02H								..
Display Data in DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=BDH								X=BEH								X=BFH							
…	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP
1	*	1	0

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGC_0$				$SEGB_0$				$SEGA_0$				$SEGC_1$				$SEGB_1$				$SEGA_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGC_{126}$				$SEGB_{126}$				$SEGA_{126}$				$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$				

HSW	ABS	REF	SWAP
1	*	1	1

Column Address / Display Data / Segment Driver																								
X=BEH								X=BFH								X=BDH								X=BEH		..
Display Data in DDRAM	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	…
Grayscale Palette	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				…
Segment Driver	$SEGA_0$				$SEGB_0$				$SEGC_0$				$SEGA_1$				$SEGB_1$				$SEGC_1$				…

Column Address / Display Data / Segment Driver																								
…	X=01H								X=02H								X=00H								X=01H	
…	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	
…	Palette A				Palette B				Palette C				Palette A				Palette B				Palette C				
…	$SEGA_{126}$				$SEGB_{126}$				$SEGC_{126}$				$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$				

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	0	X=00H						←→	X=7FH										
*	*	1	1	X=7FH						←→	X=00H										
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C		
Segment Driver				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$		

HSW	ABS	REF	SWAP	Column Address / Display Data / Segment Driver																	
*	*	0	1	X=00H						←→	X=7FH										
*	*	1	0	X=7FH						←→	X=00H										
Display Data in DDRAM				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Grayscale Palette				Palette A			Palette B			Palette C		←→	Palette A			Palette B			Palette C		
Segment Driver				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$		

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(4-5) Write Data and Read Data

16-bit Bus Length

ABS=0

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓															↓
Read Data	D_{15}	D_{14}	D_{13}	D_{12}	*	D_{10}	D_9	D_8	D_7	*	*	D_4	D_3	D_2	D_1	*

ABS=1

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓															↓
Read Data	*	*	*	*	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

8-bit Bus Length

ABS=0, HSW=0, C256=0 (Column Address: 00H, 02H, …FCH, FEH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	*	D_2	D_1	D_0

ABS=0, HSW=0, C256=0 (Column Address: 01H, 03H, …FDH, FFH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	*	*	D_4	D_3	D_2	D_1	*

ABS=1, HSW=0, C256=0 (Column Address: 00H, 02H, …FCH, FEH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	*	*	*	*	D_3	D_2	D_1	D_0

ABS=1, HSW=0, C256=0 (Column Address: 01H, 03H, …FDH, FFH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ABS=0, HSW=1, C256=0 (Column Address: 00H, 01H, …BEH, BFH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

ABS=0, HSW=0, C256=1 (Column Address: 00H, 01H, …7EH, 7FH)

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write Data	↓							↓
Read Data	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

NOTE) * : Invalid Data

(5) GRAYSCALE CONTROL CIRCUIT

(5-1) Display Mode Selection

A display mode is selected by the combination of the D_2 (MON) bit of the "Display Control (1)" instruction and the D_3 (PWM) and D_2 (C256) bits of the "Display Mode Control" instruction, as shown below.

Table 11 Display Mode Selection

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f_{OSC1}
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f_{OSC2}
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f_{OSC3}
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, "C256" bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256="0" (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256="1" (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the "C256" bit is usually "1". For more information how the display data is assigned, refer to "(4-4) Bit Assignment of Display Data".

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the "Frequency Control" Instruction. Refer to "(10) OSCILLATOR" and "OSCILLATION FREQUENCY AND FRAME FREQUENCY".

(5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes Aj, Bj and Cj (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEGAi, SEGBi and SEGCi (i=0 to 127) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

(5-1-2) Variable 8-grayscale Mode

Each of the palettes Aj, Bj and Cj (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEGAi, SEGBi and SEGCi (i=0 to 127)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

(5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes Aj, Bj and Cj (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEGAi, SEGBi and SEGCi (i=0 to 127)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

(5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.

(6) GRAYSCALE PALETTE

(6-1) Grayscale Selection in Variable 16-grayscale Mode

Table 12-1 Grayscale selection

(Palette Aj, Bj, and Cj)

Display Data MSB----LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

Table 12-2 Grayscale Palette

(Palette Aj, Bj, and Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) “MON=0”, “PWM=0”, “C256=0”
NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

(6-2) Grayscale Selection in Variable 8-grayscale Mode

Table 13-1 Grayscale selection

(Palette Aj and Bj)

Display Data MSB----LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

Table 13-2 Grayscale Palette

(Palette Aj and Bj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) “MON=0”, “PWM=0”, “C256=1”.
NOTE2) Applied to palette Aj and Bj (j=0 to 15)
NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

Table 13-3 Grayscale selection

(Palette Cj)

Display Data MSB----LSB	Palette Name
0 0 * *	Palette A3/B3/C3
0 1 * *	Palette A7/B7/C7
1 0 * *	Palette A11/B11/C11
1 1 * *	Palette A15/B15/C15

Table 13-4 Grayscale Palette

(Palette Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) “MON=0”, “PWM=0”, “C256=1”
NOTE2) Applied to palette Cj (j=0 to 15)
NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

(6-3) Grayscale Selection in Fixed 8-grayscale Mode

Table 14-1 Grayscale Selection

(Palette Aj and Bj)

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

Table 14-2 Grayscale Palette

(Palette Cj)

Display Data MSB- - - -LSB	Grayscale
0 0 * *	0/7
0 1 * *	3/7
1 0 * *	5/7
1 1 * *	7/7

NOTE1) “MON=0”, “PWM=1”, “C256=0 or 1”

(6-4) Grayscale Selection in B&W Mode

Table 15 Grayscale Selection

Display Data MSB- - - -LSB	Grayscale
0 * * *	0
1 * * *	1

NOTE1) “MON=1”, “PWM=0 or 1” and “C256=0 or 1”

(7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting "1" at the D_0 (SON) bit of the "Duty-1 /Display Clock ON/OFF" instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers Ai, Bi and Ci (i=0 to 127) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes "H".

(8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The "All Pixels ON/OFF", "Display ON/OFF" and "Reverse Display ON/OFF" instructions control the data in this circuit, but does not change the data in the DDRAM.

(9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 40 common drivers and 384-segment drivers. The common drivers generate LCD driving waveforms formed on the V_{LCD}, V_1, V_4 and V_{SSH} levels. The segment drivers generate waveforms formed on the V_{LCD}, V_2, V_3 and V_{SSH} levels.

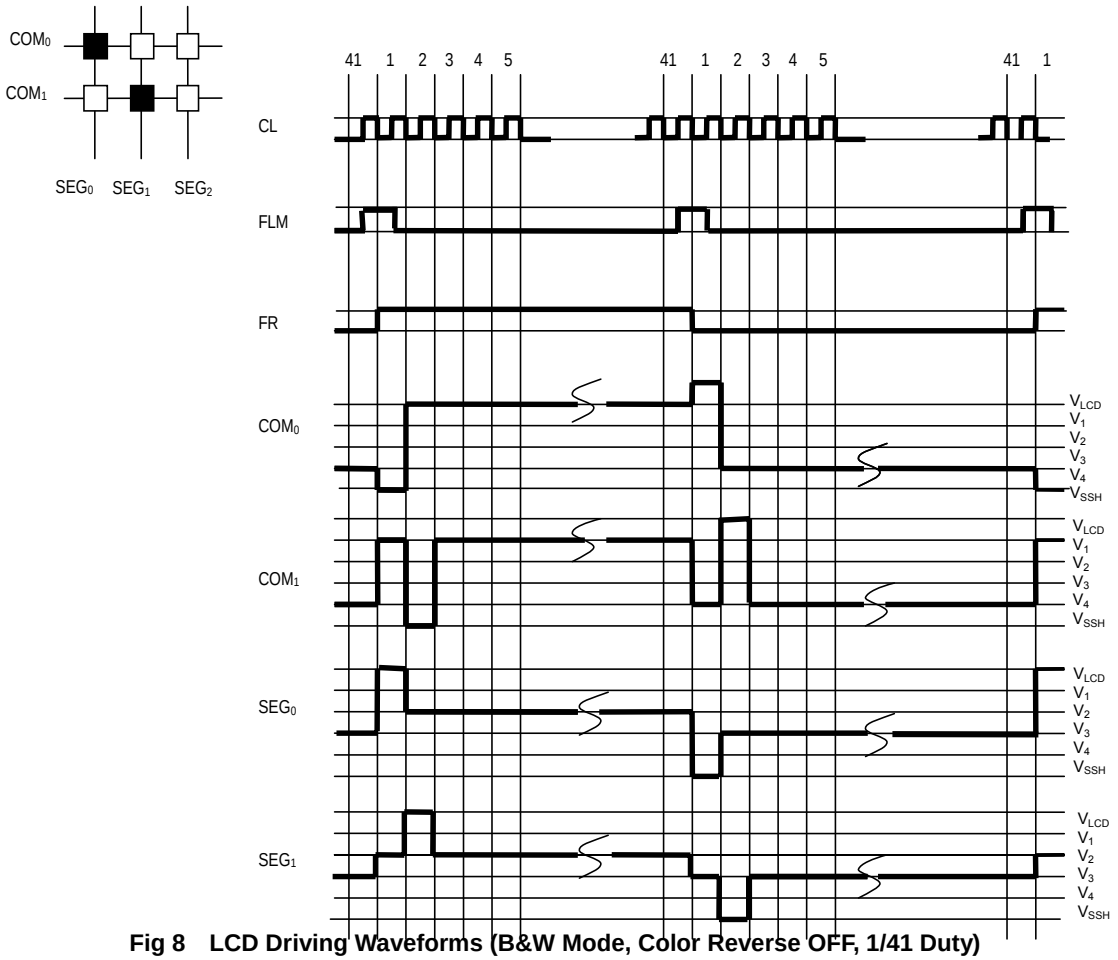


Fig 8 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/41 Duty)

(10) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting "0" at the D_1 (CKS) bit of the "Bus Length" instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D_2-D_0 (RF2-RF0) bits of the "Frequency Control" instruction. For more safety, make sure what is the best frequency in the particular application.

(10-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at "H" or "L" and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

Table 16 Oscillation Frequency vs. Display Mode

Symbol	MON	PWM	Display Mode
f_{OSC1}	0	0	Variable 8-/16-grayscale Mode
f_{OSC2}	0	1	Fixed 8-grayscale Mode
f_{OSC3}	1	*	B&W Mode

*: Don't care

(10-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

(10-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

(11) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D_3 (AMPON) and D_1 (DCON) bits of the "Power Control" instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 17.

Table 17 Configuration of LCD Power Supply

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4	1, 3, 4
0	1	Inactive	Active	V_{OUT}	2, 3, 4
1	1	Active	Active	–	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C_{1+}, C_{1-}, C_{2+}, C_{2-}, C_{3+}, C_{3-}, C_4+, C_4-, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) Only the voltage converter is used. The V_{OUT} is externally supplied, and the C_{1+}, C_{1-}, C_{2+}, C_{2-}, C_{3+}, C_{3-}, C_{4+}, C_{4-}, and V_{EE} are open. The reference voltage is supplied on the V_{REF}.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

(11-1) Voltage Booster

The internal voltage booster generates up to $5xV_{EE}$ voltage. The boost level is selected from 2x, 3x, 4x or 5x, by setting the D_2-D_0 (VU2-VU0) bits of the "Boost Level" instruction. The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

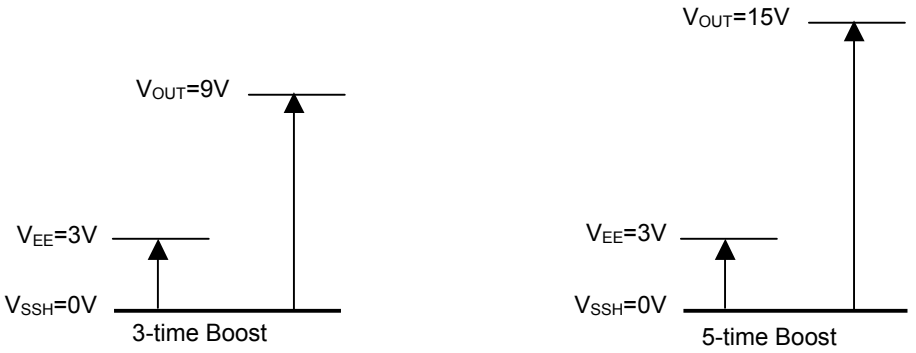


Fig 9 Boost Voltage

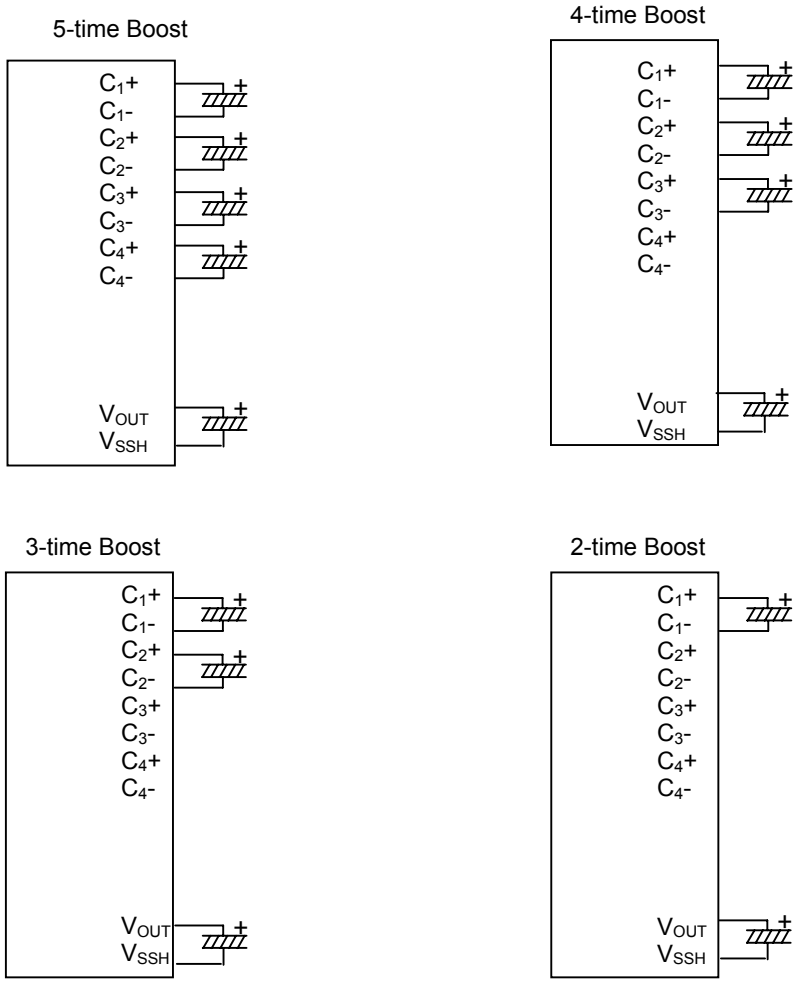


Fig 10 External Capacitor Connection of Voltage Booster

(11-2) Voltage Converter

(11-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage (V_{BA}=0.9xV_{EE}). When using the internal LCD power supply, connect the V_{BA} and the V_{REF}, or supply 0.9xV_{EE} or lower voltage on the V_{REF}. When using an external LCD power supply, the V_{BA} should be open.

(11-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and its multiple (boost level) is set by the D_2-D_0 (VU2-VU0) bits of the "Boost Level" instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \qquad \text{(N: Boost Level)}$$

(11-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the V_{LCD} voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D_2-D_0 (DV_2-DV0) bits of the "EVR Control" instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \qquad \text{(M: EVR Value)}$$

(11-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the V_{LCD}, V_1, V_2, V_3 and V_4, and its bias ratio is selected from 1/4, 1/5, 1/6, 1/7 or 1/8..

As shown in Fig 11, when using only the internal LCD power supply, the capacitors CA2 are connected to the V_{LCD}, V_1, V_2, V_3 and V_4 respectively.

As shown in Fig 12, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the V_{LCD}, V_1, V_2, V_3 and V_4, and the internal LCD power supply should be turned off by setting "0" at the "DCON" and "AMPON" bits. And the C_{1+}, C_1-, C_{2+}, C_{2-}, C_{3+}, C_3-, C_{4+}, C_4-, V_{EE}, V_{REF} and V_{REG} are open.

Fig 13 and 14 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 15 shows the circuit when partially using the LCD power supply without the voltage booster.

(11-3) External Components for LCD Power Supply

Using Only Internal LCD Power Supply (5x boost)

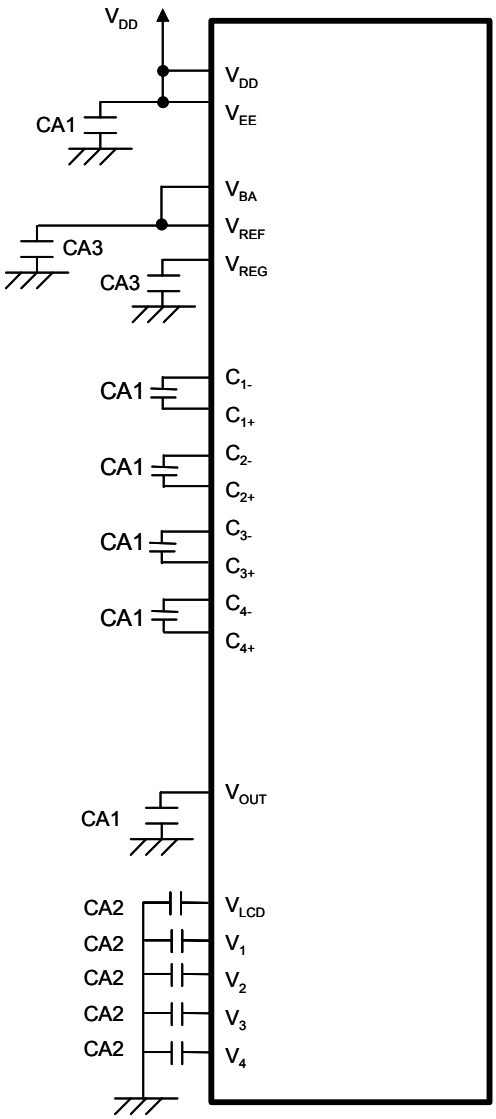


Fig 11

Using Only External LCD Power Supply

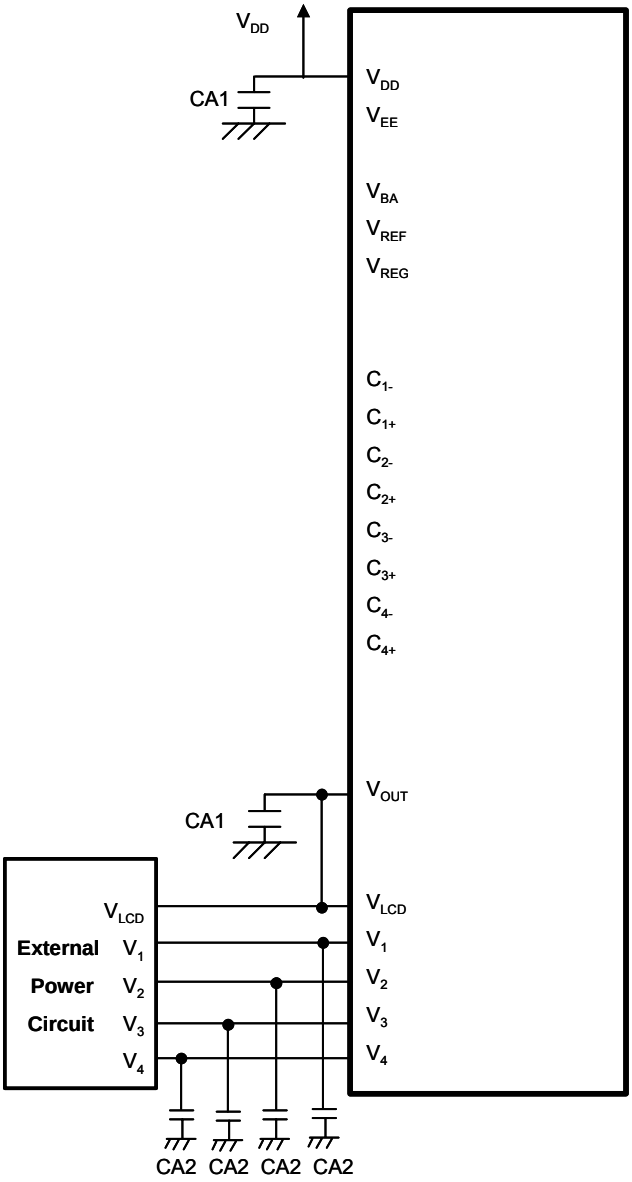


Fig 12

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply
Without Reference Voltage generator (1)
(5x boost)

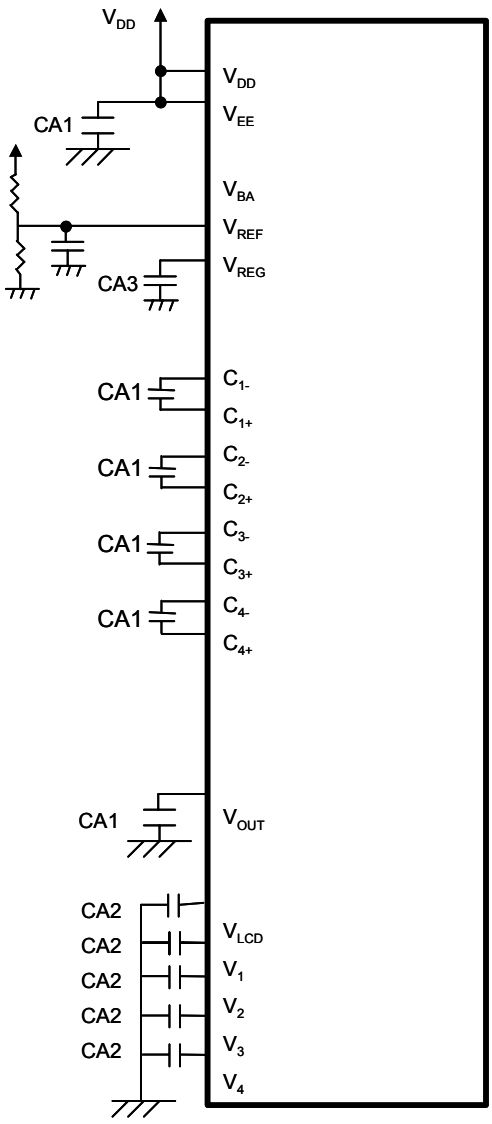


Fig 13

Using Internal LCD Power Supply
Without Reference Voltage generator (2)
(5x boost)

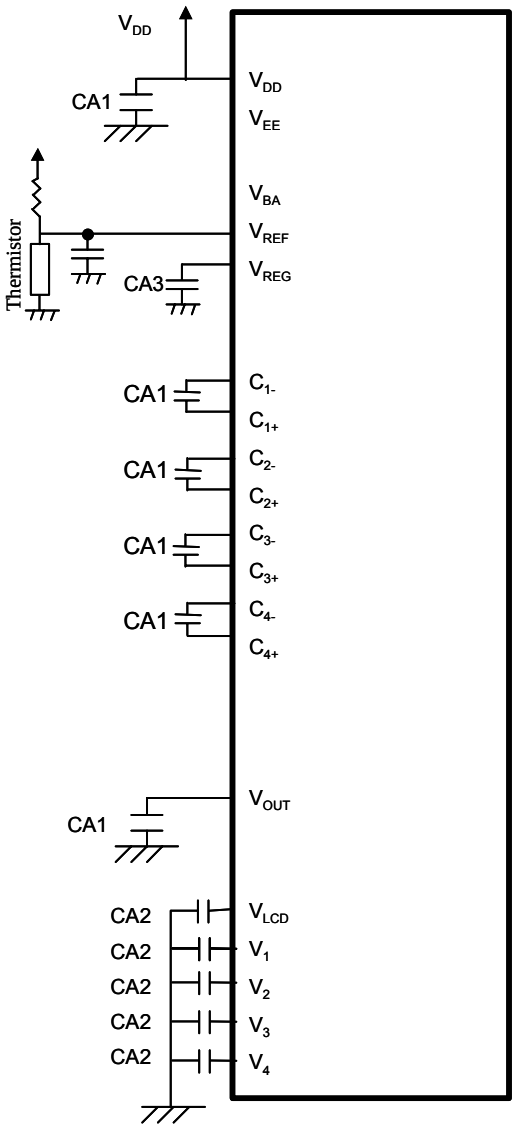


Fig 14

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply
Without Voltage Booster

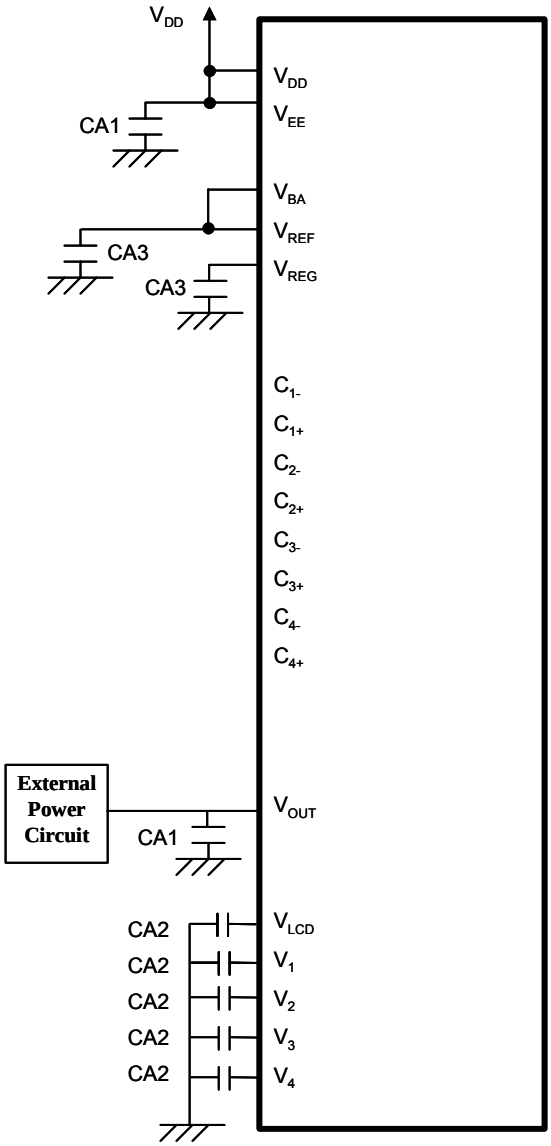


Fig 15

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_{LCD}, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(11-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the V_{LCD} and V_1-V_4 and for the V_{OUT}. The V_{LCD} and V_1-V_4 are discharged by setting "1" at the D_0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. And the V_{OUT} (100KΩ internal resistor between V_{OUT} and V_{EE}) is discharged by setting "1" at the D_1 (DIS2) bit of this instruction. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to "(14-22) Discharge ON/OFF".

(11-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to "(18) TYPICAL INSTRUCTION SEQUENCES".

(11-5-1) Power ON/OFF in Using Internal LCD Power Supply

Power ON

First "V_{DD} and V_{EE} ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First "Reset by RESb or "HALT" instruction", next "V_{DD} and V_{EE} OFF". If using different power sources for the V_{DD} and the V_{EE} individually, the V_{EE} must be turned off after the reset or the "HALT". After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_{LCD}, V_1, V_2, V_3 and V_4) drop below the threshold level of LCD pixels.

(11-5-2) Power ON/OFF in Using External LCD Power Supply

Power ON

First "V_{DD} and V_{EE} ON", next "Reset by RESb", then "External LCD power supply ON". When using only external V_{OUT}, first "V_{DD} ON", next "Reset by RESb", then "External V_{OUT} ON", as well.

Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next "V_{DD} OFF". For more safety, placing a resistor in series on the V_{LCD} line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50Ω and 100Ω.

(12) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to "L". Connecting the RESb with MPU's reset is recommended so that the LSI and MPU is initialized at a time.

Default Status

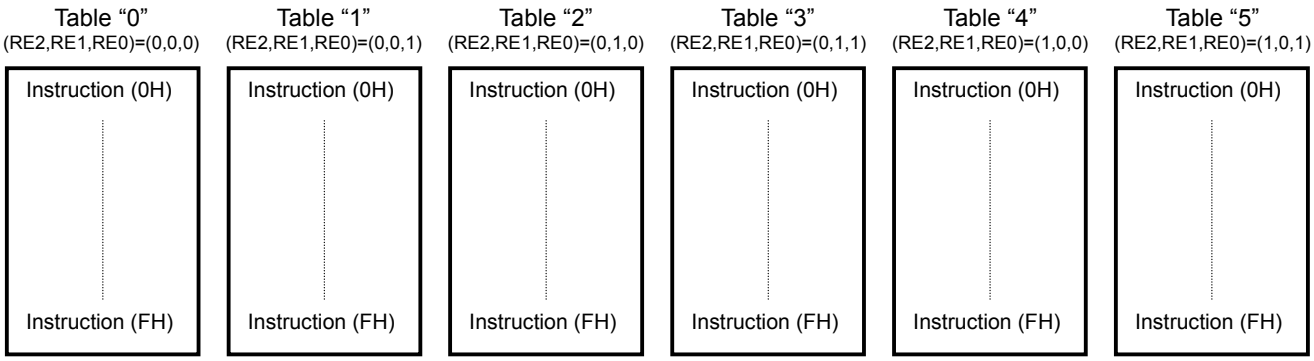
1. Display Data in DDRAM :Undefined
2. Column Address :(00)H
3. Row Address :(00)H
4. Initial Display Line :(0)H (1st line)
5. Display ON/OFF :OFF
6. Reverse Display ON/OFF :OFF (Normal)
7. Duty Cycle Ratio :1/41Duty (DSE=0)
8. N-line Inversion ON/OFF :OFF
9. COM Scan Direction :$COM_0 \rightarrow COM_{39}$
10. Increment Control :Auto-increment OFF (AIM, AXI, AYI)=(0, 0, 0)
11. REF :REF=0 (Normal)
12. Swap :OFF (Normal)
13. EVR Value :(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply :OFF
15. Display Mode :Grayscale Mode
16. LCD Bias Ratio :1/8 Bias
17. Palette 0 :(0, 0, 0, 0, 0)
18. Palette 1 :(0, 0, 0, 1, 1)
19. Palette 2 :(0, 0, 1, 0, 1)
20. Palette 3 :(0, 0, 1, 1, 1)
21. Palette 4 :(0, 1, 0, 0, 1)
22. Palette 5 :(0, 1, 0, 1, 1)
23. Palette 6 :(0, 1, 1, 0, 1)
24. Palette 7 :(0, 1, 1, 1, 1)
25. Palette 8 :(1, 0, 0, 0, 1)
26. Palette 9 :(1, 0, 0, 1, 1)
27. Palette 10 :(1, 0, 1, 0, 1)
28. Palette 11 :(1, 0, 1, 1, 1)
29. Palette 12 :(1, 1, 0, 0, 1)
30. Palette 13 :(1, 1, 0, 1, 1)
31. Palette 14 :(1, 1, 1, 0, 1)
32. Palette 15 :(1, 1, 1, 1, 1)
33. Display Mode Control :Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length :8-bit Bus Length
35. Discharge ON/OFF :OFF (DIS2, DIS)=(0,0)

(13) INSTRUCTION TABLES

(13-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 16, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 17 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 16 Instruction Table Overview

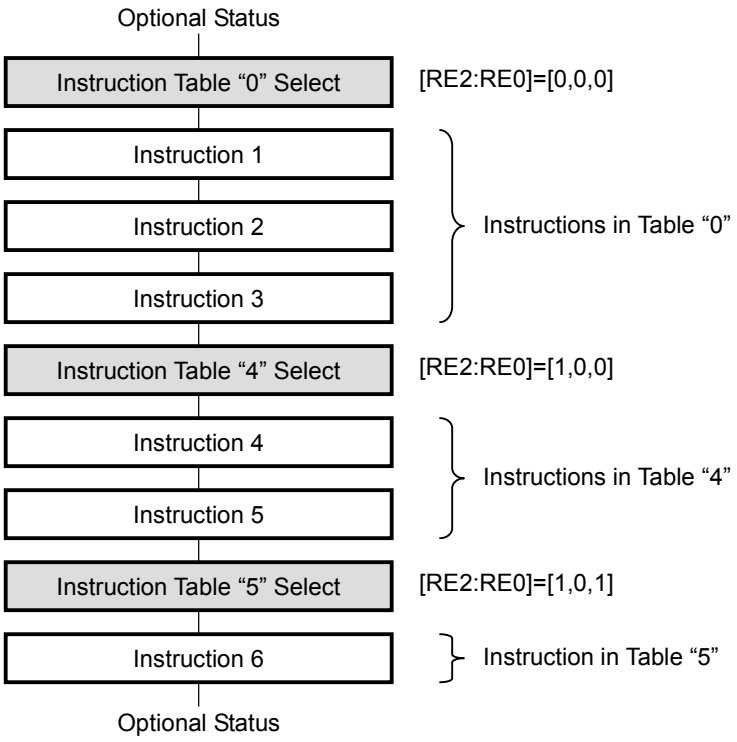


Fig 17 Outline of Instruction Sequence

(13-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

	Instructions/ Register Address [NH]	Code (80 Series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data
3	Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point
	Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point
4	Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point
	Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	*	*	AY5	AY4	Setting Row Address for start point
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	*	*	LA5	LA4	Setting Row Address for Initial COM
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	*	*	N5	N4	Setting the Number of N-line Inversion
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF REF : Segment Direction
9	Increment Control [AH]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN : Window Area ON/OFF AIM : Read-Modify-Write ON/OFF AYI : Row Increment AXI : Column Increment
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio
12	Boost Level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	VU2-0 : Setting Boost Level
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
	Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)
	Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)
	Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)
	Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PG84	Setting Palette Data : B0(PS=0) /B8(PS=1)
	Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)
	Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)
	Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)
	Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)
	Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)
	Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)
	Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)
	Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)
	Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)
	Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
	Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Setting Palette Data : C4(PS=0) /C12(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

	Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
15	Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
	Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16	Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17	Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18	Display Mode Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed Grayscale Mode C256 : 256-color Mode ON/OFF. :
19	Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High Speed Writing ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20	EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
	EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21	Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22	Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge ON/OFF
23	Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24	Register Read	0	1	0	1	0/1	0/1	0/1					Read Data				Reading Instruction
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(13-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	*	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	*	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	*	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Upper/Lower Palette Register
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWM S	PWM A	PWM B	PWM C	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.
NOTE2) [NH] (N=0-F) : Register Address
NOTE3) Any nonexistent instruction code is prohibited.
NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.
NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

(14-1) Display Data Write

The "Display Data Write" instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display Data							

(14-2) Display Data Read

The "Display Data Read" instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display Data							

(14-3) Column Address

The "Column Address" instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

(14-4) Row Address

The "Row Address" instruction specifies the row address of the start point. Available setting range is from (00H) to (27H), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	AY5	AY4

(Default: AY5-AY4=0H / Register Address: 3H)

(14-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to "(14-16) Initial COM". The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	LA5	LA4

(Default: LA5-LA4=0H / Register Address: 5H)

Table 18 Initial Display Line Address

LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			⋮			⋮
1	0	0	1	1	1	39

(14-6) N-line Inversion

The number of N line is selected in between "2" and "40". When the N-line inversion is enabled by setting "1" at the D_2 (NLIN) bit of the "Display Control (2)" instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting "0" at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	N5	N4

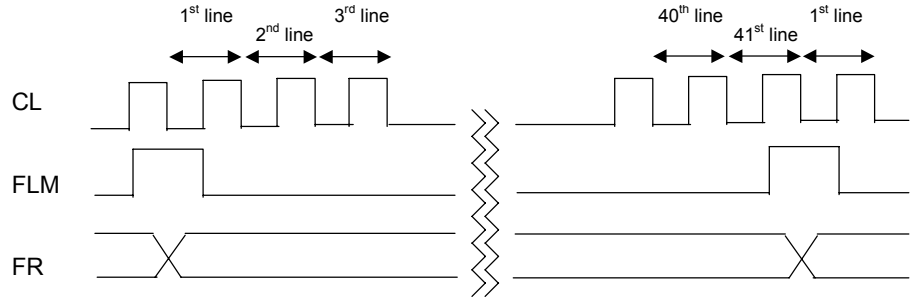
(Default: N5-N4=0H / Register Address: 7H)

Table 19 N-line Inversion

LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	N value
0	0	0	0	0	0	Inhibited*
0	0	0	0	0	1	2
			⋮			⋮
1	0	0	1	1	1	40

NOTE1) N Line=(N Value)+1

N-line inversion OFF



N-line inversion ON

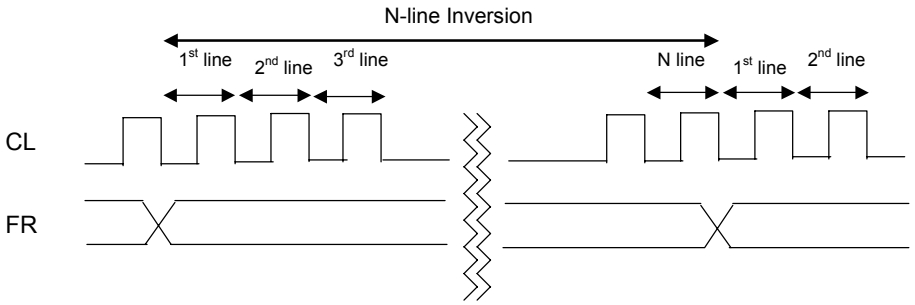


Fig 18 N-line Inversion Timing (1/41 Duty)

(14-7) Display Control (1)

The "Display Control (1)" instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

D_0 (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V_{SSH} level)
ON/OFF=1 : Display ON

D_1 (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the "REV" bit of the "Display Control (2)" instruction.

ALLON=0 : Normal
ALLON=1 : All pixels ON

D_2 (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)
MON=1 : B&W Mode

D_3 (SHIFT)

SHIFT=0 : $COM_0 \rightarrow COM_{39}$
SHIFT=1 : $COM_0 \leftarrow COM_{39}$

(14-8) Display Control (2)

The "Display Control (2)" instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

(Default: [REV,NLIN,SWAP,REF]=0H / Register Address: 9H)

D_0 (REF)

This bit controls the DDRAM access direction which reverses the segment direction for reducing the restrictions on the IC position of an LCD module. For more information, refer to "(17) SWAP FUNCTION".

D_1 (SWAP)

This bit swaps palettes Aj and palettes Cj (j=0-15). This function reduces the restrictions on the IC position of an LCD module. Refer to "(16) SWAP FUNCTION".

SWAP=0 : SWAP OFF
SWAP=1 : SWAP ON

D_2 (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)
NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

D_3 (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)
REV=1 : Reverse Display ON

Table 20 Reverse Display ON/OFF

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(14-9) Increment Control

The "AIM", "AYI" and "AXI" bits set an auto-increment operation to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up, whenever the DDRAM is accessed. The "WIN" bits enables/disables the window area access.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	WIN	AIM	AYI	AXI

(Default: [WIN,AIM,AYI,AXI]=0H / Register Address: AH)

D_2 (AIM)

Table 21 Read-modify-write ON/OFF

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

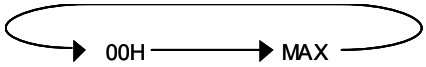
NOTE1) Increment in writing and reading display data
NOTE2) Increment in writing display data only

D_1, D_0 (AYI, AXI)

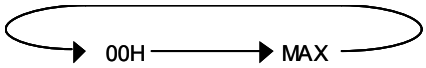
Table 22 Column/Row Increment

AYI	AXI	Column/Row Increment	NOTE
0	0	Non Increment	1
0	1	Column Address Increment	2
1	0	Row Address Increment	3
1	1	Column & Row Addresses Increment	4

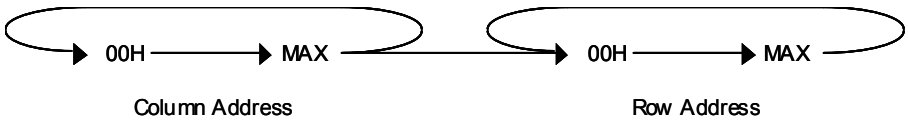
NOTE1) Non increment. The "AIM" bit is disabled.
NOTE2) Increment operation of column address. The "AIM" bit is enabled.



NOTE3) Row address increment. The "AIM" bit is enabled.



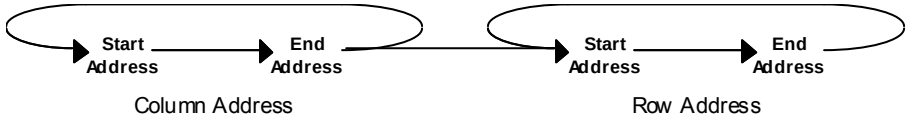
NOTE4) Column & row addresses increment. The "AIM" bit is enabled.



D_3 (WIN)

The window access should be enabled (WIN=1) in combination with the auto-increment operation (AXI=1, AYI=1). The typical sequence of the window area setting is discussed in "(4-2) Window Area for DDRAM Access".

WIN=0 : Window Area Access OFF (Normal DDRAM Access)
WIN=1 : Window Area Access ON



(14-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

D_0 (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)
ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

D_1 (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF
DCON=1 : Voltage Booster ON

D_2 (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)
HALT=1 : Power Save ON

Internal State in Power Save Mode (HALT="1")
- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V_{SSH} level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V_{LCD}, V_1, V_2, V_3 and V_4 are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

D_3 (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF
AMPON=1 : Voltage Converter ON

(14-11) Duty Cycle Ratio

The "Duty Cycle Ratio" instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the "Boost Level", the "LCD Bias Ratio" and the "EVR Control".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

Table 23 Duty Cycle Ratio

DS_3	DS_2	DS_1	DS_0	Duty cycle ratio		# of Commons
				DSE=0	DSE=1	
0	0	0	0	1/41	1/40	40 commons
0	0	0	1	1/37	1/36	36 commons
0	0	1	0	1/33	1/32	32 commons
0	0	1	1	1/29	1/28	28 commons
0	1	0	0	1/25	1/24	24 commons
0	1	0	1	1/21	1/20	20 commons
0	1	1	0	1/17	1/16	16 commons
0	1	1	1	1/13	1/12	12 commons
1	0	0	0	1/9	1/8	8 commons
1	0	0	1	1/5	1/4	4 commons
1	0	1	0	Inhibited		
1	0	1	1	Inhibited		
1	1	0	0	Inhibited		
1	1	0	1	Inhibited		
1	1	1	0	Inhibited		
1	1	1	1	Inhibited		

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting "1" at the D_1 (DSE) bit of the "Duty-1 ON/OFF" instruction. Refer to "(14-17) Duty-1 /Display Clock ON/OFF".

(14-12) Boost Level

The "Boost Level" selects the multiple of the voltage booster.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU2	VU1	VU0

(Default:VU2-VU0=0H / Register Address: DH)

D_2, D_1, D_0 (VU2, VU1, VU0)

Table 24 Boost Level

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

.

(14-13) LCD Bias Ratio

The “LCD bias ratio” selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

Table 25 LCD Bias Ratio

B2	B1	B0	LCD Bias Ratio
0	0	0	1/8
0	0	1	1/7
0	1	0	1/6
0	1	1	1/5
1	0	0	1/4
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(14-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

Table 26 Instruction Table Select

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) “TST0” bit must be “0”. This is used for maker tests only.

(14-15) Palette A / B / C

Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in "(6) GRAYSCALE PALETTE" for default setting.

Palette A5 (PS=0) / Palette A13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

Palette A6 (PS=0) / Palette A14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

Palette A7 (PS=0) / Palette A15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B5 (PS=0) / Palette B13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

Palette B6 (PS=0) / Palette B14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

Palette B7 (PS=0) / Palette B15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C5 (PS=0) / Palette C13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

Palette C6 (PS=0) / Palette C14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

Palette C7 (PS=0) / Palette C15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

(14-16) Initial COM

The "Initial COM" instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

Table 27 Initial COM

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM_0	COM_{39}
0	0	0	1	COM_4	COM_{35}
0	0	1	0	COM_8	COM_{31}
0	0	1	1	COM_{12}	COM_{27}
0	1	0	0	COM_{16}	COM_{23}
0	1	0	1	COM_{20}	COM_{19}
0	1	1	0	COM_{24}	COM_{15}
0	1	1	1	COM_{28}	COM_{11}
1	0	0	0	COM_{32}	COM_7
1	0	0	1	COM_{36}	COM_3
1	0	1	0	Inhibited	Inhibited
1	0	1	1	Inhibited	Inhibited
1	1	0	0	Inhibited	Inhibited
1	1	0	1	Inhibited	Inhibited
1	1	1	0	Inhibited	Inhibited
1	1	1	1	Inhibited	Inhibited

(14-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

D_0 (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at "L" level.
SON=1 : CL, FLM, FR, and CLK are enabled.

D_1 (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting "1" at the "DSE" bit.

DSE=0 : OFF (Duty-0)
DSE=1 : ON (Duty-1)

NOTE) For the last common timing at "DSE=0", all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/41 duty cycle, the segment waveforms for 41st common timing are the same as for 40th common timing (last line).

(14-18) Display Mode Control

The "Display Mode Control" instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D_2 (MON) bit of the "Display Control (1)" is used in combination. Refer to "(5) GRAY SCALE CONTROL CIRCUIT" and "(14-7) Display Control (1)."

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	C256	*	*

(Default: PWM,C256=0H / Register Address: 8H)

D_3 (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)
PWM=1 : Fixed 8-grayscale Mode

D_2 (C256)

C256=0 : Variable 16-grayscale Mode at "PWM=0" (4096 colors)
C256=1 : Variable 8-grayscale Mode at "PWM=0" (256 colors)

(14-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration, ABS mode ON/OFF and high speed writing ON/OFF as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	HSW	ABS	CKS	WLS

(Default: HSW,ABS,CKS,WLS=0H / Register Address: 9H)

D_0 (WLS)

WLS=0: 8-bit Bus Length
WLS=1: 16-bit Bus Length

D_1 (CKS)

CKS =0: Internal Oscillator using an internal resistor
CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to "(10) OSCILLATOR".

D_2 (ABS)

ABS=0: ABS Mode OFF (Normal)
ABS=1: ABS Mode ON

D_3 (HSW)

HSW=0: High Speed Writing OFF (Normal)
HSW=1: High Speed Writing ON

(14-20) EVR Control

The "EVR Control" instruction adjusts V_{LCD} to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V_{LCD}. The setting order is upper byte first, then lower byte. Refer to "(11-2-3) Electrical Variable Resistor (EVR)".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV0

(Default: DV_3-DV0=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV6	DV_5	DV_4

(Default: DV6-DV_4=0H / Register Address: BH)

Table 28 EVR Control

DV6	DV_5	DV_4	DV_3	DV_2	DV_1	DV0	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	1	High

Formula of VLCD
VLCD [V] = 0.5x VREG + M (VREG – 0.5x VREG) / 127

VBA = VEE x 0.9
VREG = VREF x N

VBA : Output of the reference voltage generator
VREF : Input of the voltage regulator
VREG : Output of the voltage regulator
N : Boost level
M : EVR Value

(14-21) Frequency Control

The "Frequency Control" instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV_3-DV0=0H / Register Address: DH)

Table 29 Frequency Control

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	0.7 x Reference Value
1	1	0	1.3 x Reference Value
1	1	1	Inhibited

(14-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V_{LCD}, V_1, V_2, V_3,V_4 and V_{OUT}. Refer to "(11-4) Discharge Circuit".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	DIS2	DIS

(Default: DIS2,DIS1=0H / Register Address: EH)

D_0 (DIS)

DIS=0 : Discharge OFF
DIS=1 : Discharge ON (Discharge from V_{LCD}, V_1, V_2, V_3 and V_4)

D_1 (DIS2)

DIS2=0 : Discharge OFF
DIS2=1 : Discharge ON (Discharge from V_{OUT} through the internal resistor between V_{OUT} and V_{EE})

NOTE) Resistance is 100KΩ typical.

(14-23) Register Address

The "Register Address" instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

(14-24) Register Read

The "Register Read" instruction reads out instruction data from the register which address is specified by the "Register Address" instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data			

(14-25) Window End Column Address

The "Window End Column Address" instruction specifies the column address of the end point. Refer to "(4-2) Window Area for DDRAM Access". The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

(14-26) Window End Row Address

The "Window End Row Address" instruction specifies the row address of the end point. Refer to "(4-2) Window Area for DDRAM Access". The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	EY5	EY4

(Default: EY5-EY4=0H / Register Address: 3H)

(14-27) Initial Line-reverse Address

The "Initial Line-reverse Address" instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	LS5	LS4

(Default: LS5-LS4=0H / Register Address: 5H)

(14-28) Last Line-reverse Address

The "Last Line-reverse Address" instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	LE5	LE4

(Default: LE5-LE4=0H / Register Address: 7H)

(14-29) Line Reverse ON/OFF

The "Line Reverse ON/OFF" instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D_3 (REV) bit of the "Display Control (2)" instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

D_0 (LREV)

LREV =0 : Line Reverse OFF (Normal)
LREV =1 : Line Reverse ON

D_1 (BT)

BT =0 : No Blink
BT =1 : Blink once every 32 frames

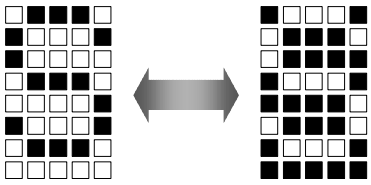


Fig 19 On-screen Image in Using Line-reverse Display and Blink Function

(14-30) Upper/Lower Palette Select

The "Upper/Lower Palette Select" instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PS

(Default: PS=0 / Register Address: 9H)

D_0 (PS)

PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, …, PC74)
PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, …, PC154)

(14-31) PWM Control

The "PWM control" instruction selects PWM type, as shown in Fig 20.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

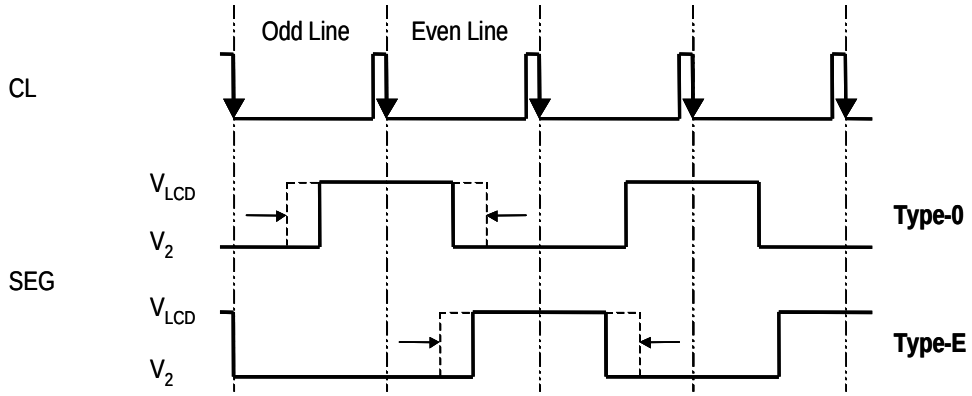
D_3 (PWMS)

PWMS=0 : Type 1
PWMS=1 : Type 2

D_2 (PWMA), D_1 (PWMB), D_0 (PWMC)

PWMZ=0 (Z=A, B and C): Type 1-O
PWMZ=1 (Z=A, B and C): Type 1-E

PWM Type 1 (PWMS=0)



PWM Type 2 (PWMS=1)

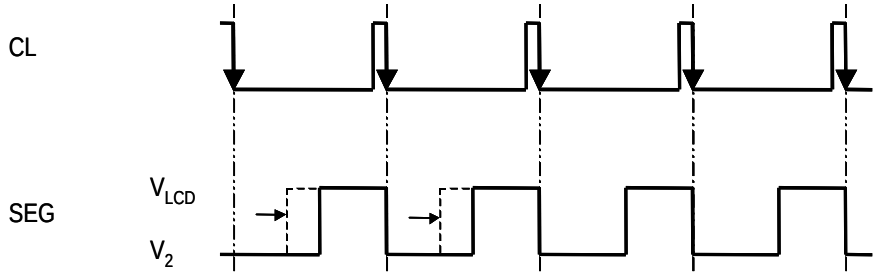


Fig 20 PWM Control

(15) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(14-11) Duty Cycle Ratio”, “(14-12) Boost Level”, “(14-13) LCD Bias Ratio” and “(14-20) EVR Control”. Typical setting sequence is shown in “(18-4) Partial Display Sequence”.

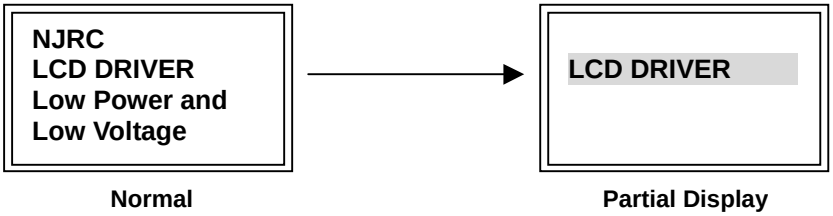


Fig 21 On-screen Image in Using Partial Display Function

(16) SWAP FUNCTION

The swap function switches the palettes Aj and the palettes Cj (j=0-15), and is controlled by the D_1 (SWAP) bit of the "Display Control (2)" instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 22 "Overview of Swap Function" illustrates general outlines of internal operations, and (16-1-1) through (16-1-4) show each configuration on a mode-by-mode basis.

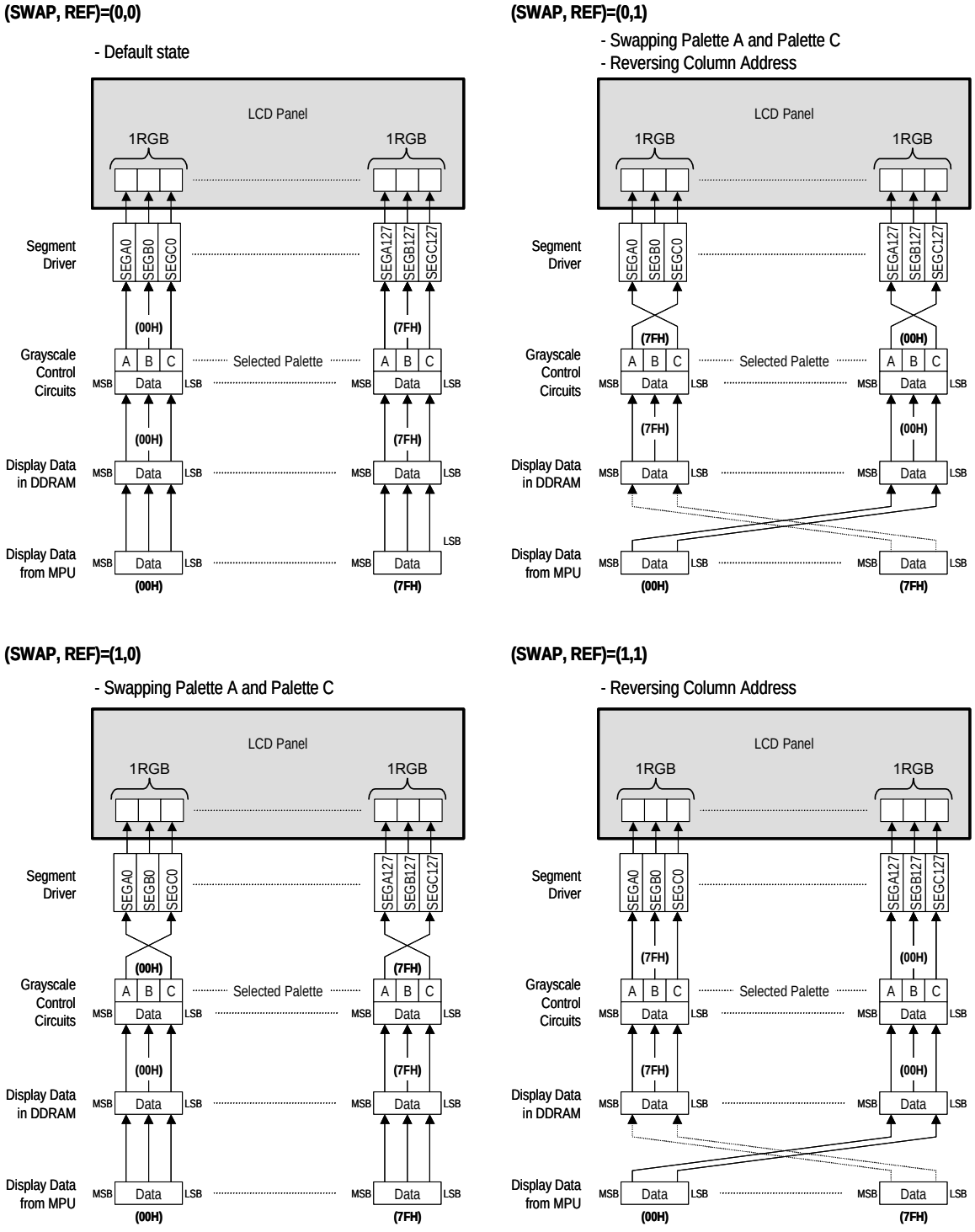
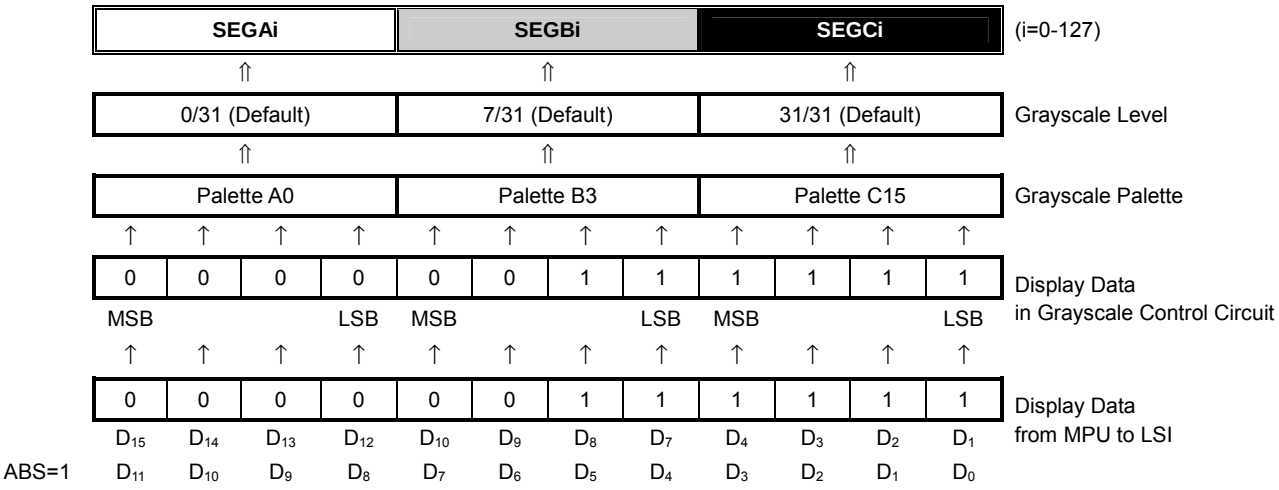


Fig 22 Overview of SWAP Function

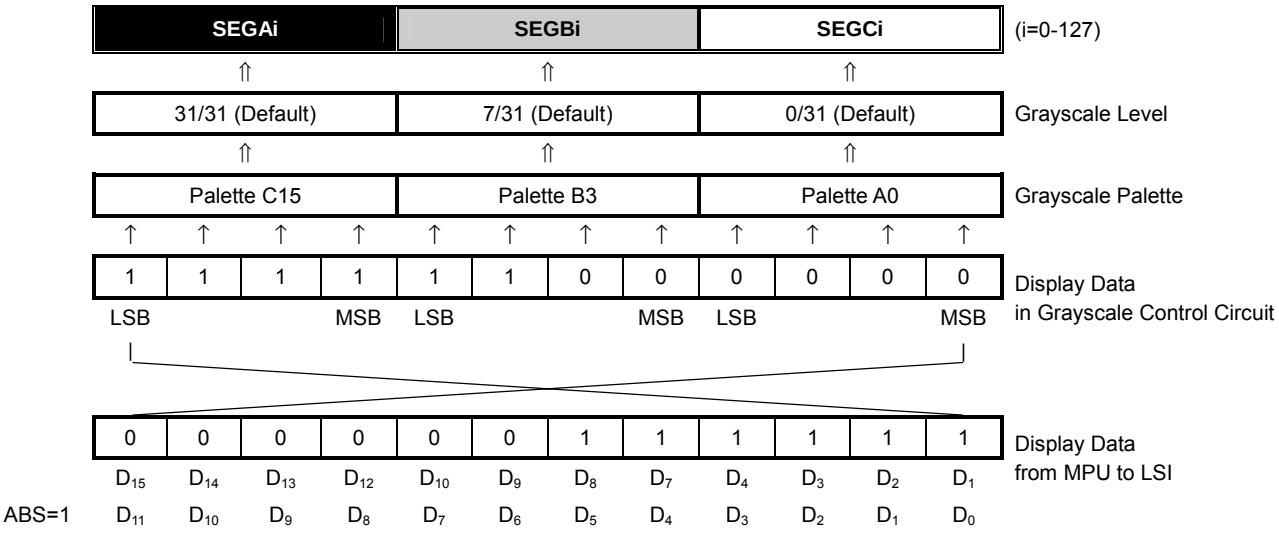
(16-1) Swap Function in Variable 16-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



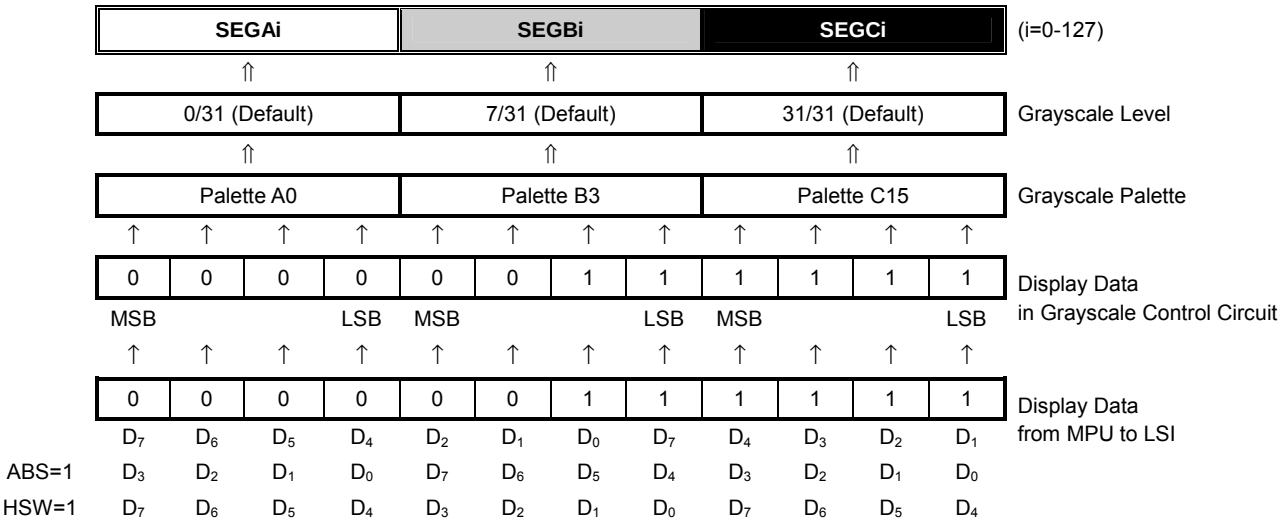
(REF, SWAP)=(0,1) or (1,0)



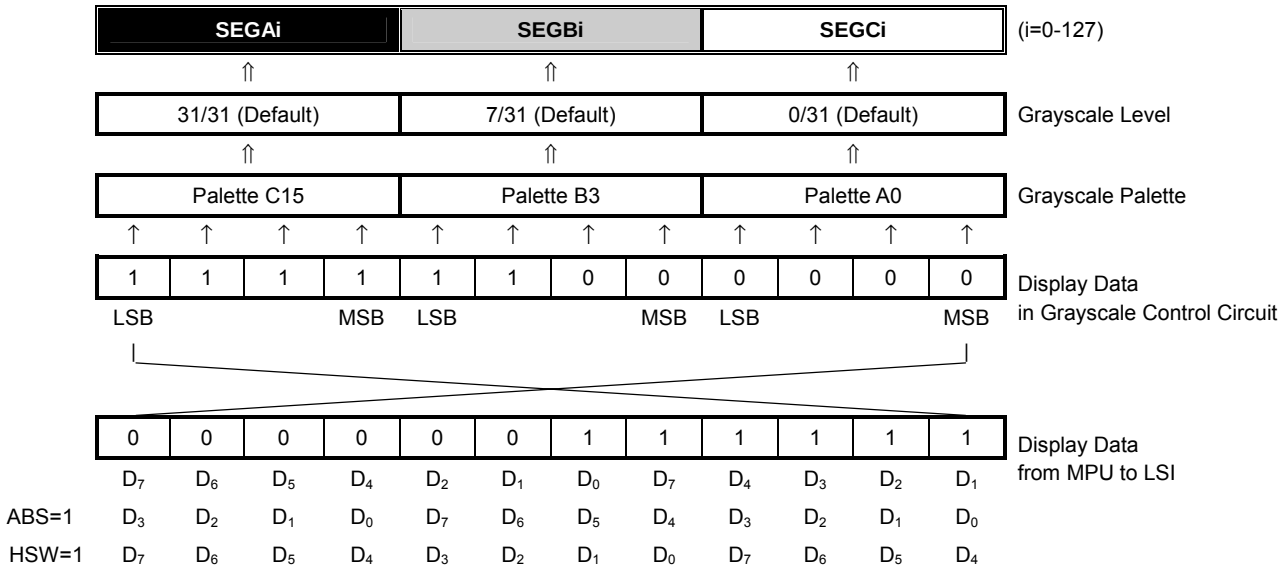
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

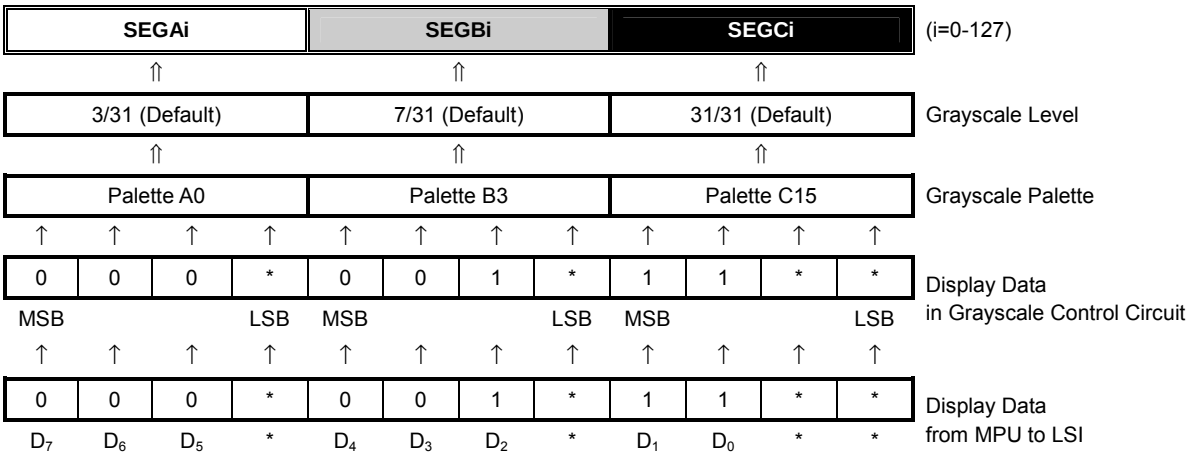


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

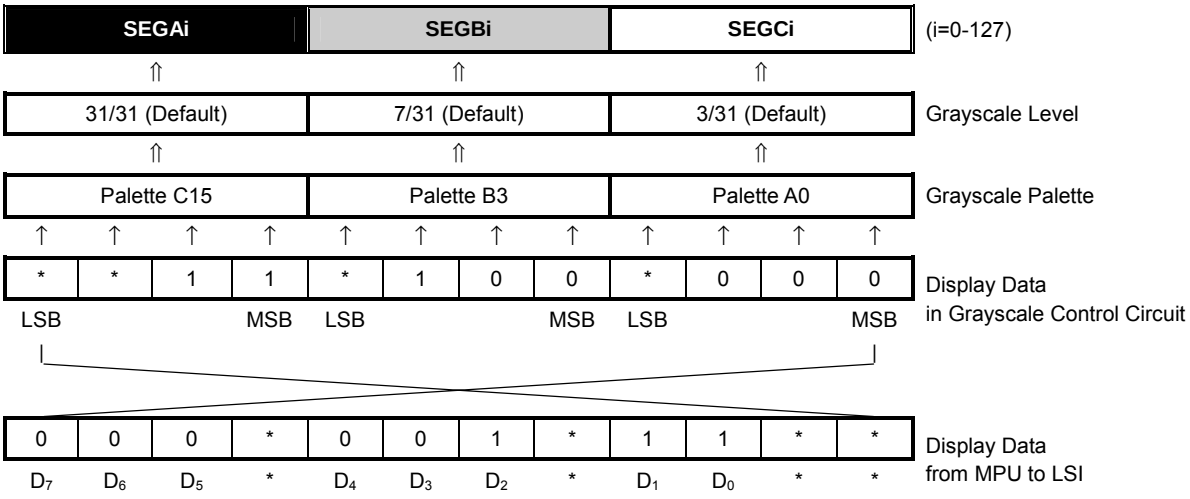
(16-2) Swap Function in Variable 8-grayscale Mode

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

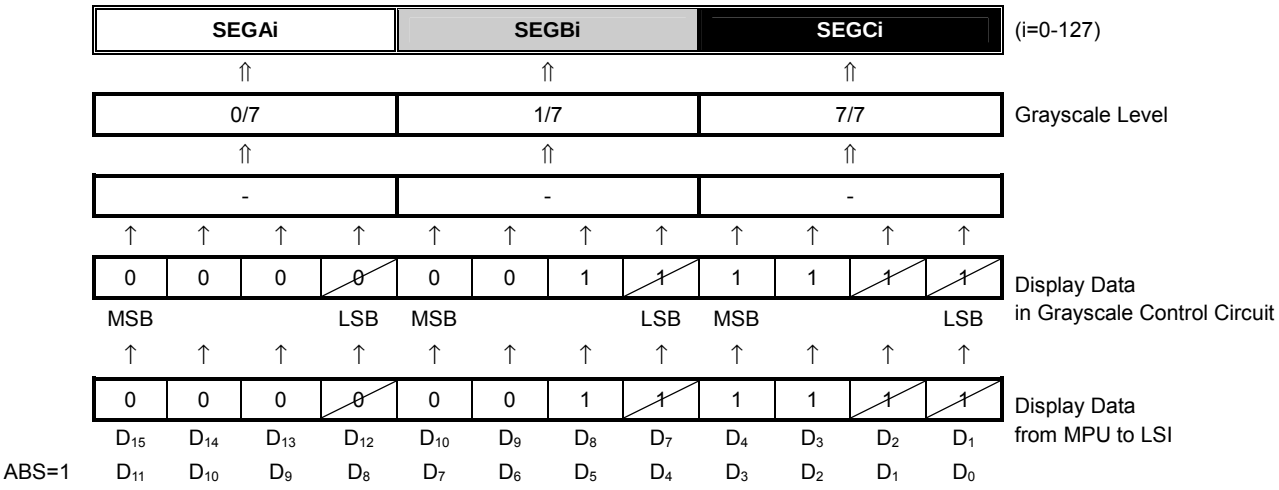


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.

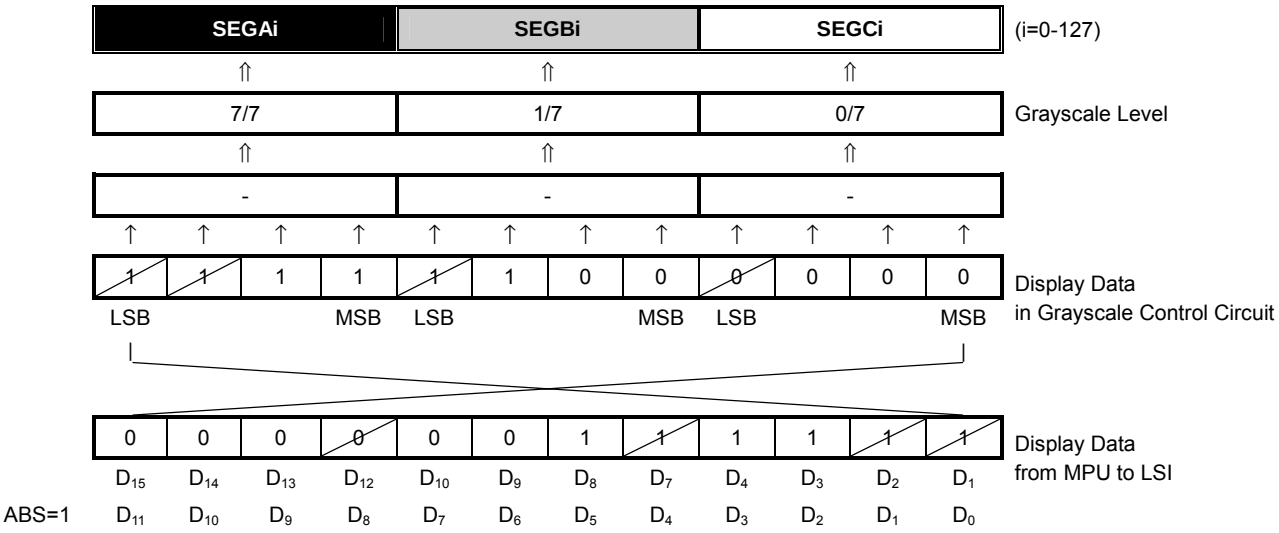
(16-3) Swap Function in Fixed 8-grayscale Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



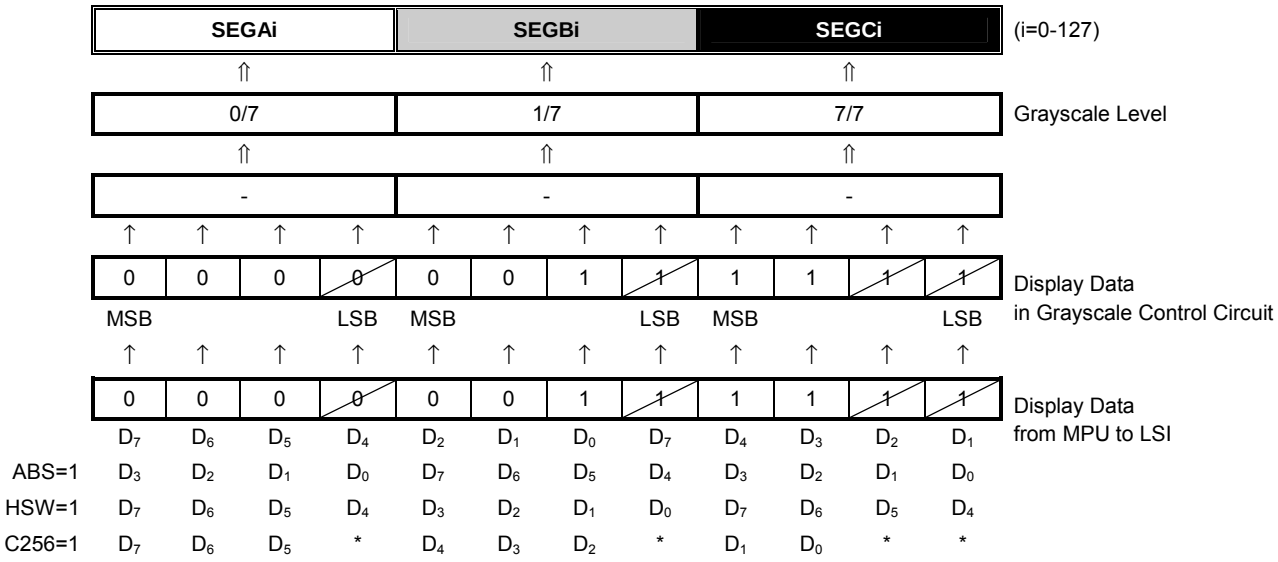
(REF, SWAP)=(0,1) or (1,0)



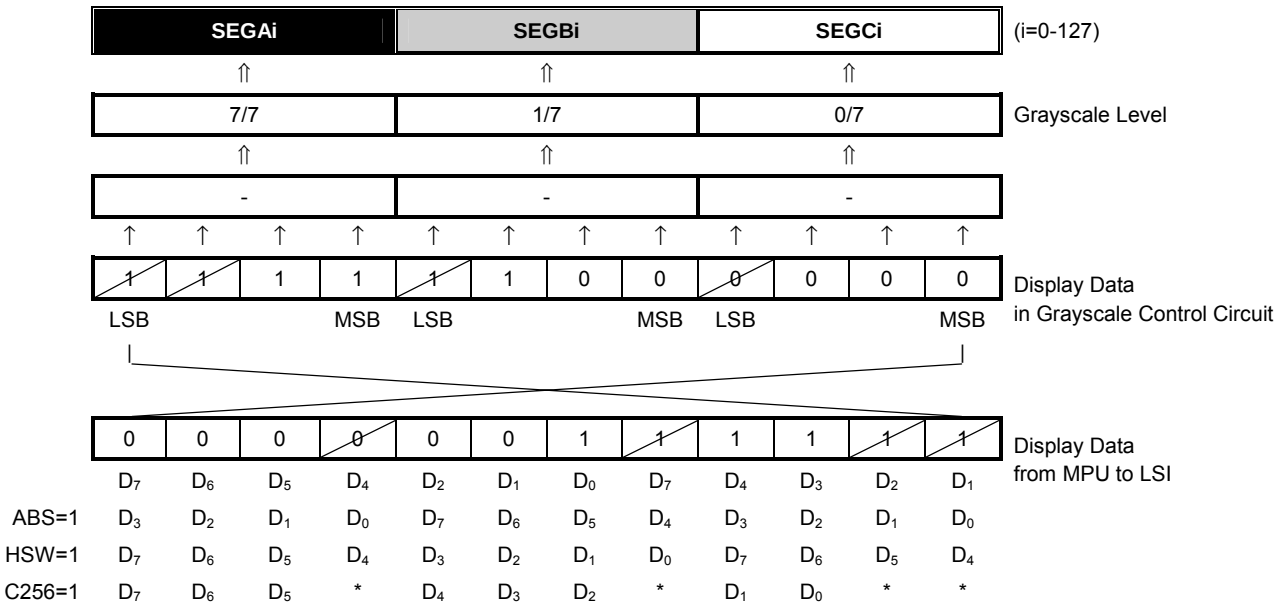
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



(REF, SWAP)=(0,1) or (1,0)

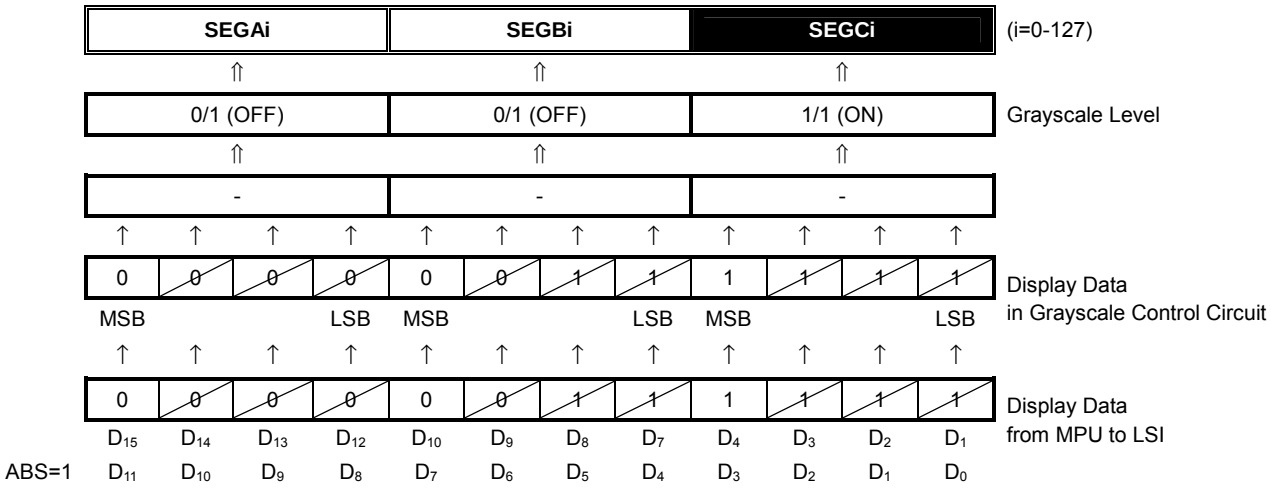


NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.
NOTE2) The data indicated with a slash mark (/) is invalid.

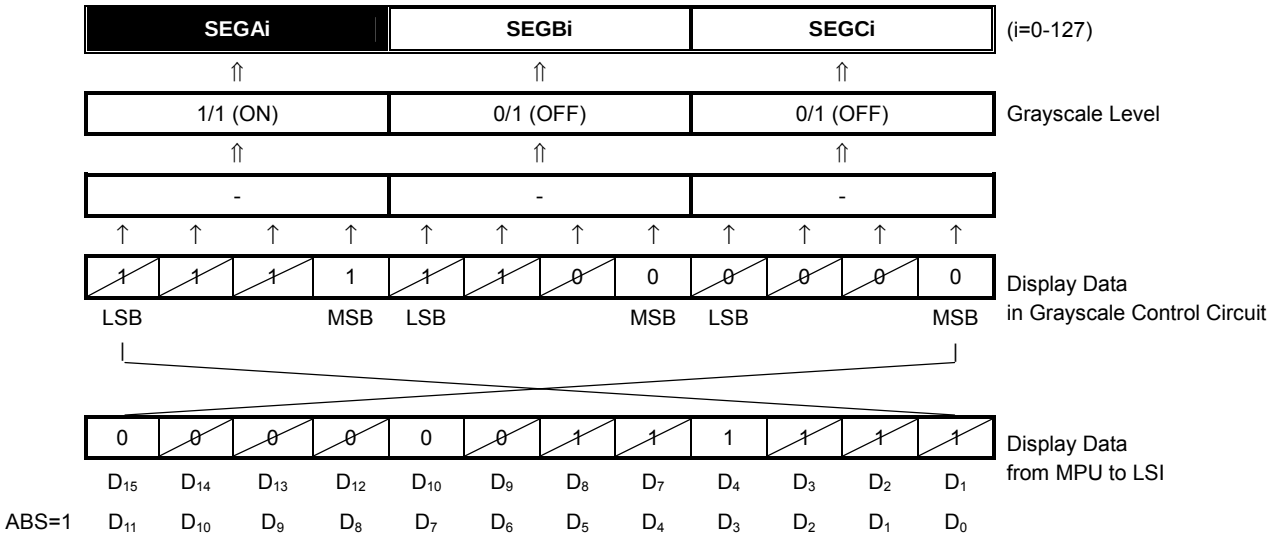
(16-4) Swap Function in B&W Mode

16-bit Bus Length

(REF, SWAP)=(0,0) or (1,1)



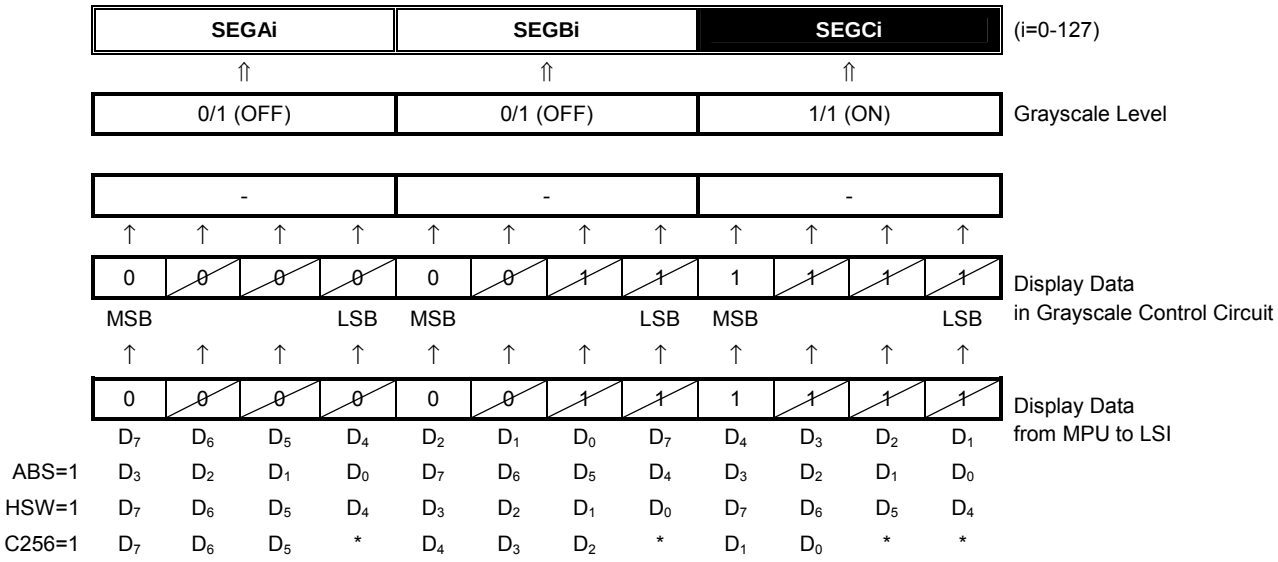
(REF, SWAP)=(0,1) or (1,0)



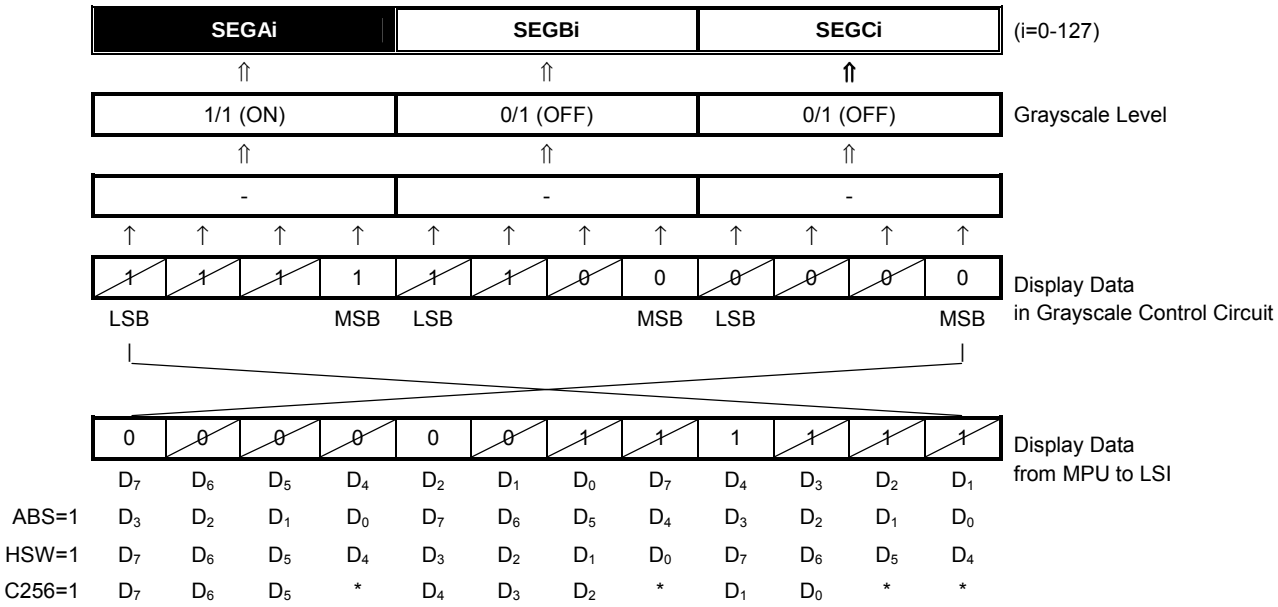
NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as “0”.
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the setting bit such as the ABS, HSW, and C256 are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

(17) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D_3 (SHIFT) bit of the "Display Control (1)" and the "Duty Cycle Ratio", "Initial Display Line" and "Initial COM" instructions.

When the "Initial Display Line" is set to (LA7:LA0=00H: Address "0"), the row address corresponding to an initial COM is "0". However, if the "Initial Display Line" is other than "0", the row address is shifted from "0" by just that address. For instance, when the initial display line address is (LA7:LA0=05H: Address "5") and the initial COM is (SC3:SC0=1H), the row address on the initial COM is "5" and the initial COM is "COM_4".

(17-1) through (17-5) illustrate the examples of the relation between row address and common driver.

(17-1) Initial display line “0”, 1/41 duty cycle (Common forward scan, DSE=”0”)

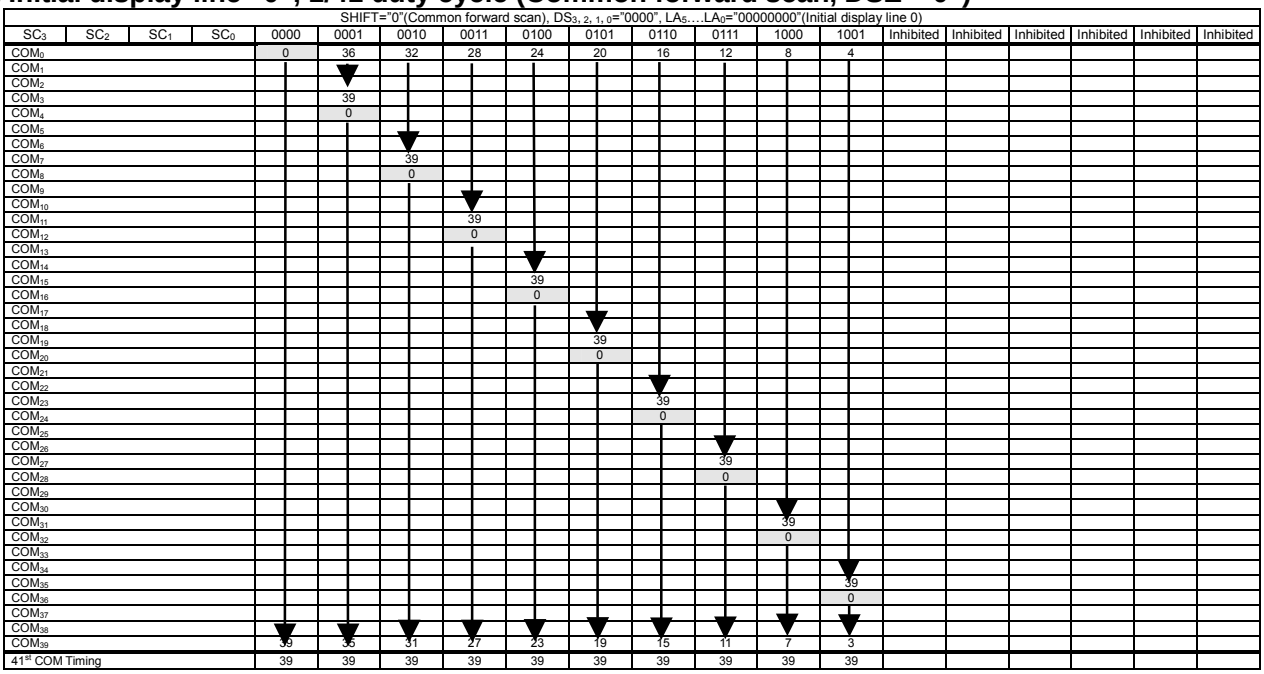


Fig 23 Relation between Row address and Common Driver (1)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 41st COM timing are the same as for 40th COM timing (Row address “27H”).

(17-2) Initial display line “0”, 1/41 duty cycle (Common backward scan, DSE=”0”)

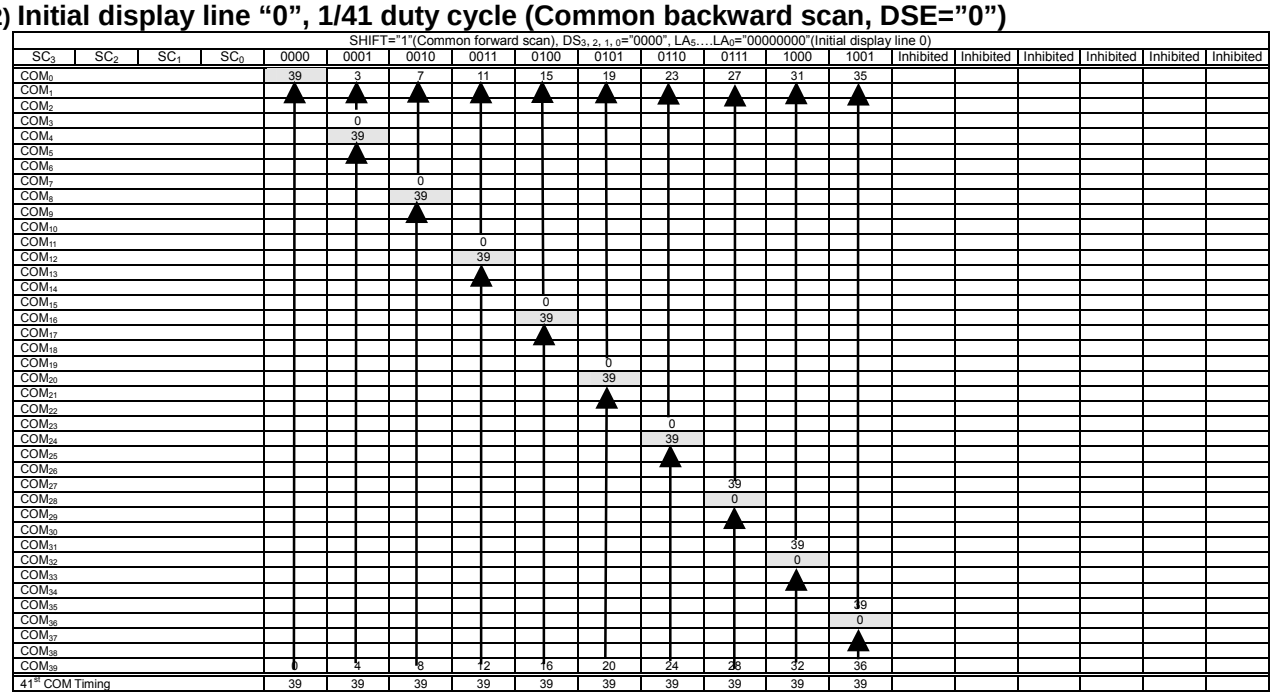


Fig 24 Relation between Row address and Common Driver (2)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 41st COM timing are the same as for 40th COM timing (Row address “27H”).

(17-3) Initial display line “0”, 1/17 duty cycle (Common forward scan, DSE=”0”)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0110”, LA_5….LA_0=”00000000”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				0							12	8	4						
COM_1																			
COM_2																			
COM_3											15								
COM_4					0														
COM_5																			
COM_6																			
COM_7												15							
COM_8						0													
COM_9																			
COM_{10}																			
COM_{11}													15						
COM_{12}							0												
COM_{13}																			
COM_{14}																			
COM_{15}				15															
COM_{16}								0											
COM_{17}																			
COM_{18}					15														
COM_{19}																			
COM_{20}									0										
COM_{21}																			
COM_{22}																			
COM_{23}						15													
COM_{24}										0									
COM_{25}																			
COM_{26}																			
COM_{27}							15												
COM_{28}											0								
COM_{29}																			
COM_{30}																			
COM_{31}								15											
COM_{32}												0							
COM_{33}																			
COM_{34}									15										
COM_{35}																			
COM_{36}													0						
COM_{37}																			
COM_{38}										15	11	7	3						
COM_{39}																			
17th COM Timing				16	16	16	16	16	16	16	16	16	16						

Fig 25 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address.
NOTE2) Segment waveforms for 17th COM timing are the same as for 16th COM timing.

(17-4) Initial display line “5”, 1/41 duty cycle (Common forward scan, DSE=”0”)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0000”, LA_5….LA_0=”00000101”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				5	1	37	33	29	25	21	17	13	9						
COM_1																			
COM_2						39													
COM_3						0													
COM_4					5														
COM_5																			
COM_6							39												
COM_7							0												
COM_8						5													
COM_9																			
COM_{10}								39											
COM_{11}								0											
COM_{12}							5												
COM_{13}																			
COM_{14}									39										
COM_{15}									0										
COM_{16}								5											
COM_{17}																			
COM_{18}										39									
COM_{19}									5	0									
COM_{20}																			
COM_{21}											39								
COM_{22}																			
COM_{23}										5	0								
COM_{24}																			
COM_{25}																			
COM_{26}												0							
COM_{27}											5								
COM_{28}																			
COM_{29}																			
COM_{30}													0						
COM_{31}												5							
COM_{32}																			
COM_{33}				39															
COM_{34}				0									5						
COM_{35}																			
COM_{36}																			
COM_{37}					39														
COM_{38}																			
COM_{39}				4	0	36	32	28	24	20	16	12	8						
41st COM Timing				39	39	39	39	39	39	39	39	39	39						

Fig 26 Relation between Row address and Common Driver (4)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 41st COM timing are the same as for 40th COM timing (Row address “27H”).

(17-5) Initial display line “0”, 1/40 duty cycle (Common forward scan, DSE=”1”)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0000”, LA_5….LA_0=”00000000”(Initial display line 0) DSE=”1”

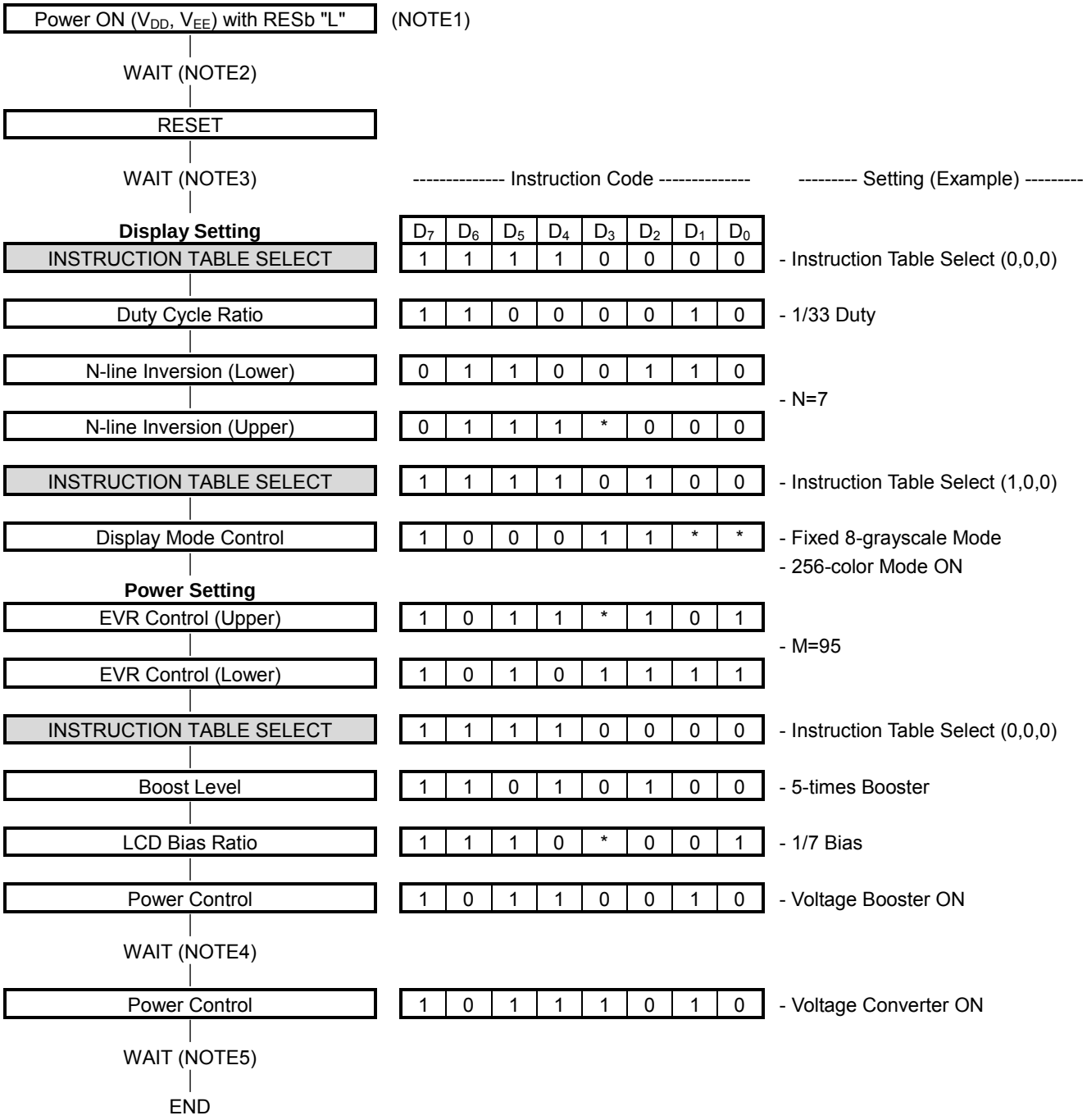
SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				0	36	32	28	24	20	16	12	8	4						
COM_1																			
COM_2																			
COM_3					39														
COM_4					0														
COM_5																			
COM_6																			
COM_7						39													
COM_8						0													
COM_9																			
COM_{10}																			
COM_{11}							39												
COM_{12}							0												
COM_{13}																			
COM_{14}																			
COM_{15}								39											
COM_{16}								0											
COM_{17}																			
COM_{18}																			
COM_{19}									39										
COM_{20}									0										
COM_{21}																			
COM_{22}																			
COM_{23}										39									
COM_{24}										0									
COM_{25}																			
COM_{26}																			
COM_{27}											39								
COM_{28}											0								
COM_{29}																			
COM_{30}																			
COM_{31}												39							
COM_{32}												0							
COM_{33}																			
COM_{34}																			
COM_{35}													39						
COM_{36}													0						
COM_{37}																			
COM_{38}																			
COM_{39}				39	35	31	27	23	19	15	11	7	3						

Fig 27 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

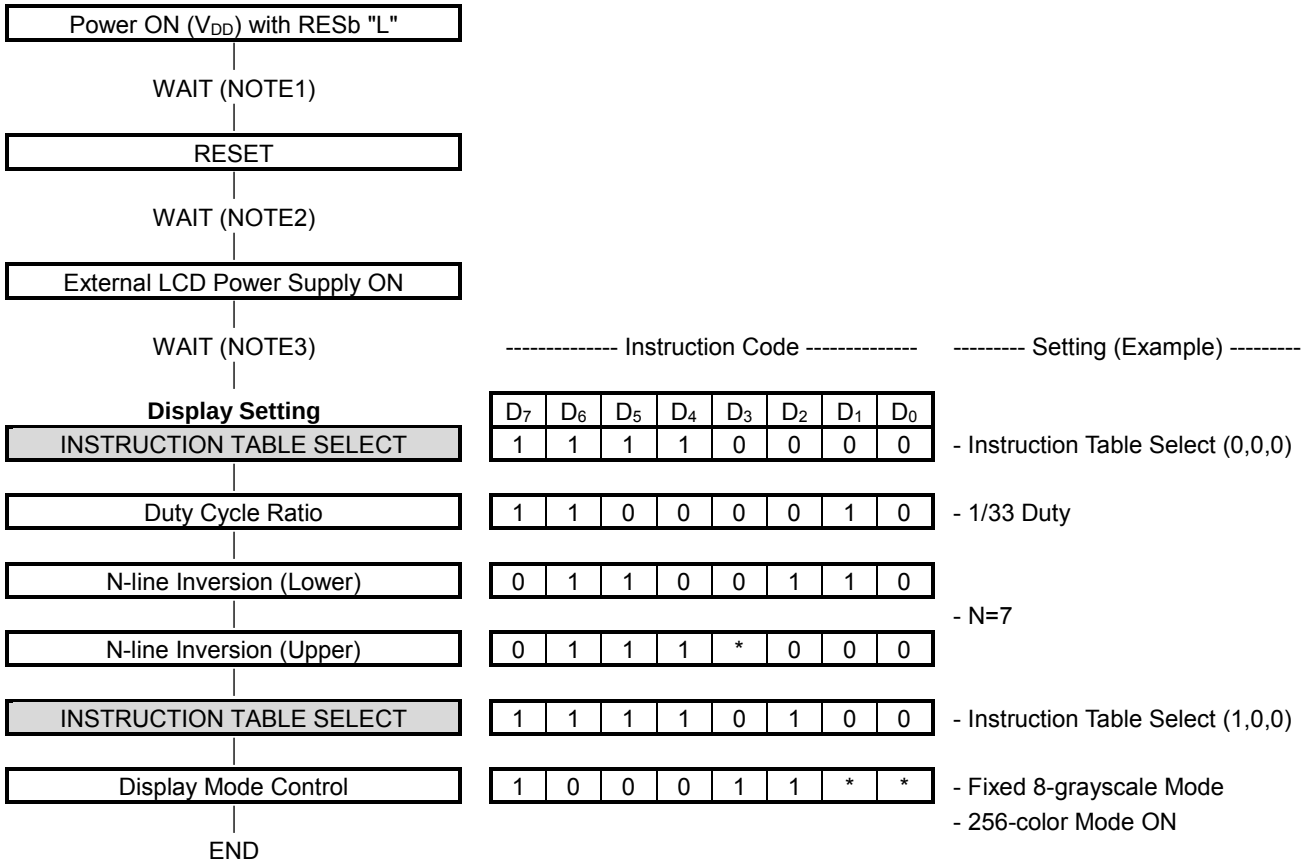
(18) TYPICAL INSTRUCTION SEQUENCES

(18-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the V_{DD} and the V_{EE}, turn on the V_{DD} first.
NOTE2) Wait until the V_{DD} and V_{EE} are stabilized.
NOTE3) Wait 10 [us] or more.
NOTE4) Wait until the V_{OUT} is stabilized.
NOTE5) Wait until the V_{LCD} and V_1-V_4 are stabilized.

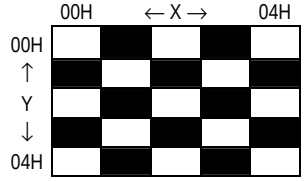
(18-2) Initialization Sequence in Using External LCD Power Supply



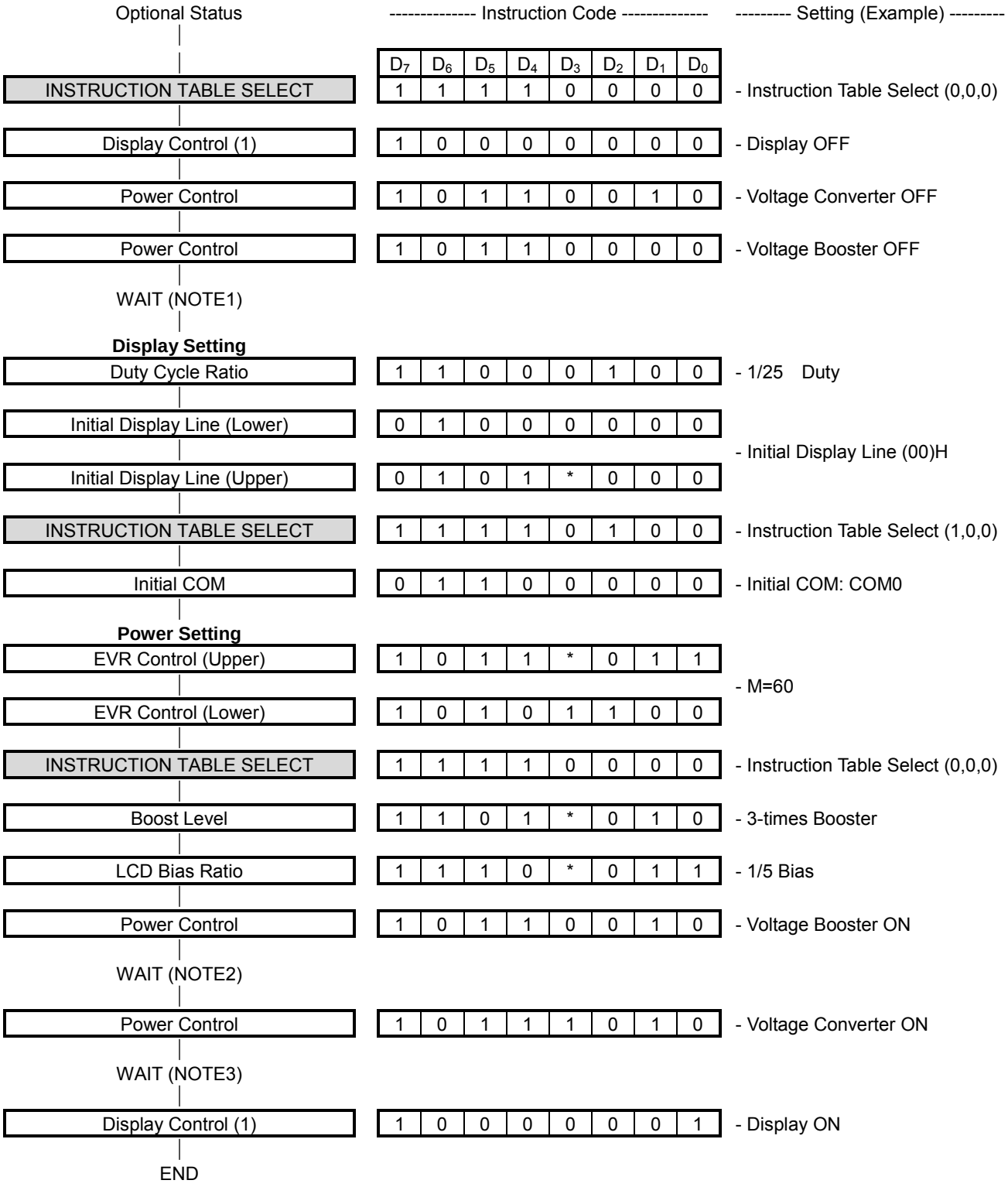
NOTE1) Wait until the V_{DD} is stabilized.
NOTE2) Wait 10 [us] or more.
NOTE3) Wait until the external LCD power supply (V_{OUT}, V_{LCD}, V_1-V_4) are stabilized.

(18-3) Display Data Write Sequence

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Setting (Example)
Optional Status									
INSTRUCTION TABLE SELECT	1	1	1	1	0	0	0	0	- Instruction Table Select (0,0,0)
Initial Display Line (Lower)	0	1	0	0	0	0	0	0	
Initial Display Line (Upper)	0	1	0	1	*	0	0	0	-Initial Display Line (00)H
Increment Control	1	0	1	0	1	1	1	1	- Window Area Access ON - Read-modify-write ON - Column & Row Increment
Column Address (Lower)	0	0	0	0	0	0	0	0	
Column Address (Upper)	0	0	0	1	0	0	0	0	- Window Start Column Address (00)H
Row Address (Lower)	0	0	1	0	0	0	0	0	
Row Address (Upper)	0	0	1	1	0	0	0	0	- Window Start Row Address (00)H
INSTRUCTION TABLE SELECT	1	1	1	1	0	1	0	1	- Instruction Table Select (1,0,1)
Window End Column Address (Lower)	0	0	0	0	0	1	0	0	
Window End Column Address (Upper)	0	0	0	1	0	0	0	0	-Window End Column Address (04)H
Window End Row Address (Lower)	0	0	1	0	0	1	0	0	
Window End Row Address (Upper)	0	0	1	1	0	0	0	0	- Window End Row Address (04)H
Display Data Write	0	0	0	0	0	0	0	0	- Writing Display Data on the DDRAM for Checker Flag in B&W Mode (Example)
:	1	1	1	1	1	1	1	1	
:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	
:	Repeating All “0” and All “1” Alternately								
:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	
:	1	1	1	1	1	1	1	1	
Display Data Write	0	0	0	0	0	0	0	0	
INSTRUCTION TABLE SELECT	1	1	1	1	0	0	0	0	- Instruction Table Select (0,0,0)
Display Control (1)	1	0	0	0	0	0	0	1	- Display ON
END									

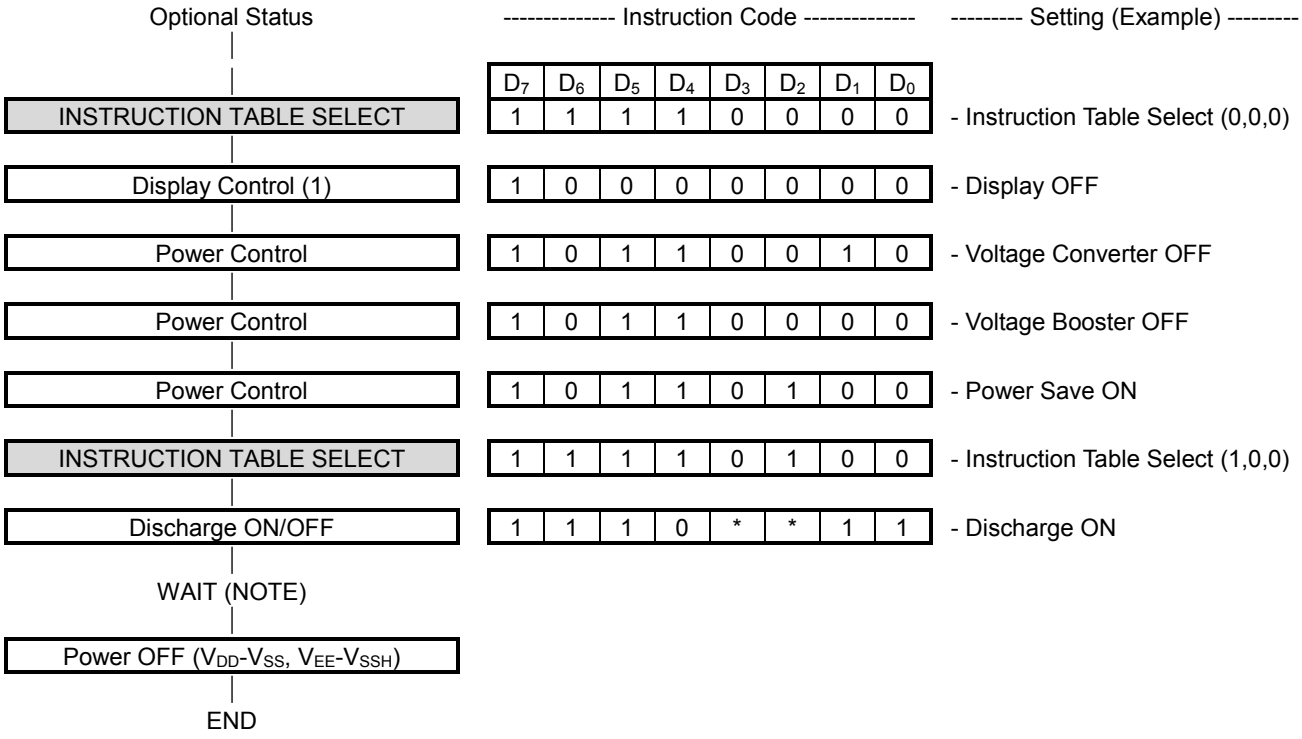


(18-4) Partial Display Sequence



NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.
NOTE2) Wait until the V_{OUT} is stabilized.
NOTE3) Wait until the V_{LCD} and V_1-V_4 are stabilized.

(18-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	Tstg			-45 to +125	°C

NOTE1) D_0 to D_{15}, CSb, RS, RDb, WRb, OSC1, RESb
NOTE2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS} and between V_{EE} and V_{SSH}.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	1
	V_{DD2}		2.4		3.3	V	2
	V_{EE}	V_{EE}	2.4		3.3	V	3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	5
Operating Temperature	Topr		-30		85	°C	

NOTE1) Applied to the condition when the reference voltage generator is not used.
NOTE2) Applied to the condition when the reference voltage generator is used.
NOTE3) Applied to the condition when the voltage booster is used.
NOTE4) The following relation among the LCD bias voltages must be maintained.
$V_{SSH} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$
NOTE5) Relation: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CSb=H, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C		166	203	240	kHz	*8
	f_{OSC2}			37	46	55		*9
	f_{OSC3}			5.3	6.6	7.8		*10
External oscillation Frequency	f_{r1}	Rf=51kΩ			172		kHz	*11
	f_{r2}	Rf=240kΩ			40			
	f_{r3}	Rf=1800kΩ			5.5			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 5) RL = 500kΩ (V_{OUT} - V_{SS})		(N x V_{EE}) x 0.95			V	*12
Supply current (1)	I_{DD1}	V_{DD} = 3V, 5-time booster Whole ON pattern			520	780	µA	*13
Supply current (2)	I_{DD2}	V_{DD} = 3V, 5-time booster Checker pattern			650	980		
Supply current (3)	I_{DD3}	V_{DD} = 3V,4-time booster Whole ON pattern			360	540		
Supply current (4)	I_{DD4}	V_{DD} = 3V, 4-time booster Checker pattern			450	680		
V_{BA} Operating voltage	V_{BA}	V_{EE} = 2.4 to 3.3V		(0.9 V_{EE}) x 0.98	0.9 V_{EE}	(0.9 V_{EE}) x 1.02	V	*14
V_{REG} Operating voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 0.9 x V_{EE} N-time booster (N=2 to 5)		(V_{REF} x N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*15
Output Voltage	V_2			-100	0	+100	mV	*16
	V_3			-100	0	+100		
	V_{D12}			-30	0	+30		
	V_{D34}			-30	0	+30		
	V_{D24}			-30	0	+30		

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/41 to 1/25	1/21 to 1/13	1/9	1/5	
Internal clock	f_{OSC}	Variable 8-/16-level Grayscale Mode	f_{OSC} / (62xD)	f_{OSC} / (62xDx2)	f_{OSC} / (62xDx4)	f_{OSC} / (62xDx8)	FLM
		Fixed 8-level Grayscale Mode	f_{OSC} / (14xD)	f_{OSC} / (14xDx2)	f_{OSC} / (14xDx4)	f_{OSC} / (14xDx8)	
		B&W Mode	f_{OSC} / (2xD)	f_{OSC} / (2xDx2)	f_{OSC} / (2xDx4)	f_{OSC} / (2xDx8)	
External clock	f_{CK}	Variable 8-/16-level Grayscale Mode	f_{CK} / (62xD)	f_{CK} / (62xDx2)	f_{CK} / (62xDx4)	f_{CK} / (62xDx8)	
		Fixed 8-level Grayscale Mode	f_{CK} / (14xD)	f_{CK} / (14xDx2)	f_{CK} / (14xDx4)	f_{CK} / (14xDx8)	
		B&W Mode	f_{CK} / (2xD)	f_{CK} / (2xDx2)	f_{CK} / (2xDx4)	f_{CK} / (2xDx8)	

NOTE1) D_0-D_{15}, CSb, RS, RDb, WRb, P/S, SEL68 and RESb

NOTE2) D_0-D_{15}

NOTE3) CL, FLM, FR and CLK

NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1

NOTE5) D_0-D_{15} in high impedance

NOTE6) $SEGA_0$-$SEGA_{127}$, $SEGB_0$-$SEGB_{127}$, $SEGC_0$-$SEGC_{127}$ and COM_0-COM_{39}
This parameter defines the resistance between each COM/SEG and each LCD bias (V_{LCD}, V_1, V_2, V_3 and V_4).
- 0.5V Difference / 1/8 LCD Bias

NOTE7) V_{DD}
Oscillator is halted.
- CSb=1 (Disabled) / No-load on COM/SEG

NOTE8) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)

NOTE9) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)

NOTE10) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.
- (Rf2, Rf1, Rf0)=(0,0,0)

NOTE11) OSC2
- V_{DD}=3V / Ta=25°C

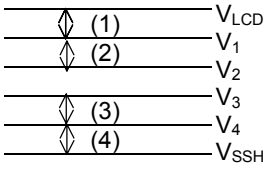
NOTE12) V_{OUT}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- V_{EE}=2.4V to 3.3V / EVR= (1,1,1,1,1,1,1) / 1/4 to 1/8 LCD Bias / 1/41 Duty Cycle / No-load on COM/SEG / RL=500kΩ between V_{OUT} and V_{SSH} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"

NOTE13) V_{SS}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- EVR= (1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU / V_{DD}=V_{EE} / V_{REF}=0.9V_{EE} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/41 Duty cycle / Ta=25°C

NOTE14) V_{BA}
- V_{BA}=V_{REF} / Boost Level (N)="1",/ DCON="0" / V_{OUT}=13.5V

NOTE15) V_{REG}
- V_{EE}=2.4V to 3.3V / V_{REF}=0.9V_{EE} / VOUT=18V / 1/4 to 1/8 LCD bias ratio / 1/41 duty cycle / EVR=(1,1,1,1,1,1,1) / Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NLIN="0"

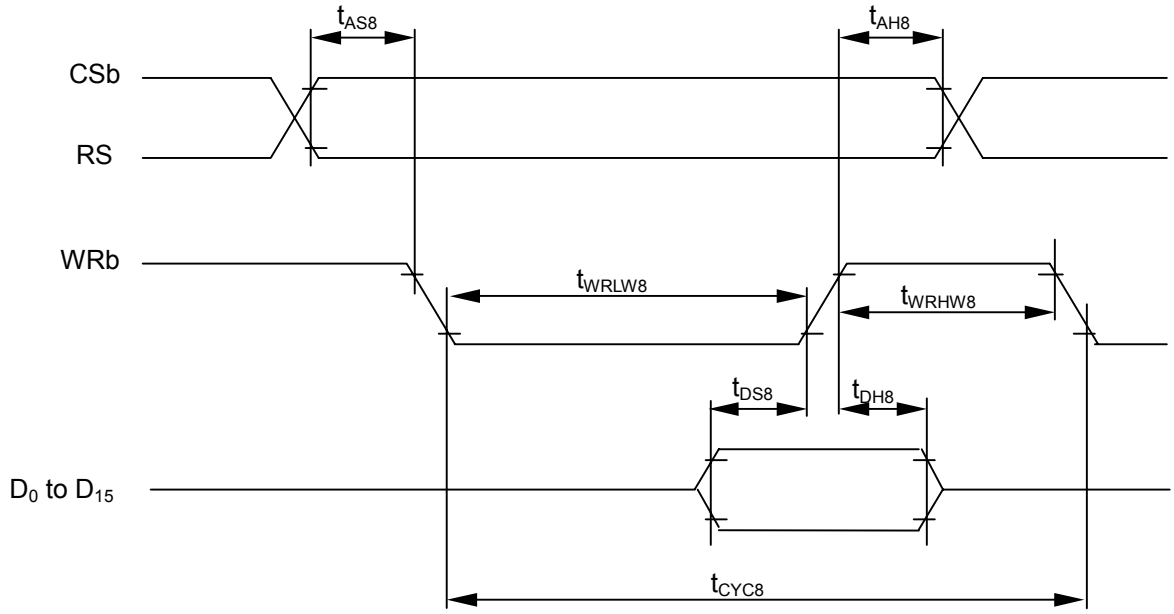
NOTE16) V_{LCD}, V_1, V_2, V_3 and V_4
- V_{EE}=3.0V / V_{REF}=0.9V_{EE} / V_{OUT}=15V/ 1/4 to 1/8 LCD Bias / EVR= (1,1,1,1,1,1,1) / Display OFF / No-load on COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



V_{D12}: (1)-(2)
V_{D34}: (3)-(4)
V_{D24}: (2)-(4)

■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

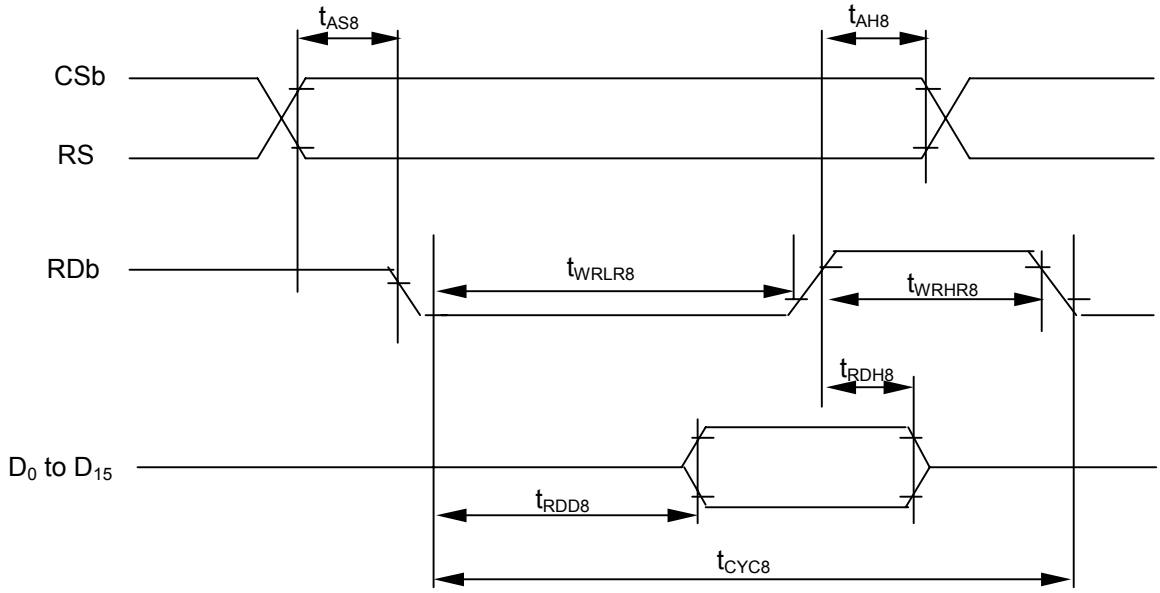
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(2) Read Operation (Parallel Interface / 80-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

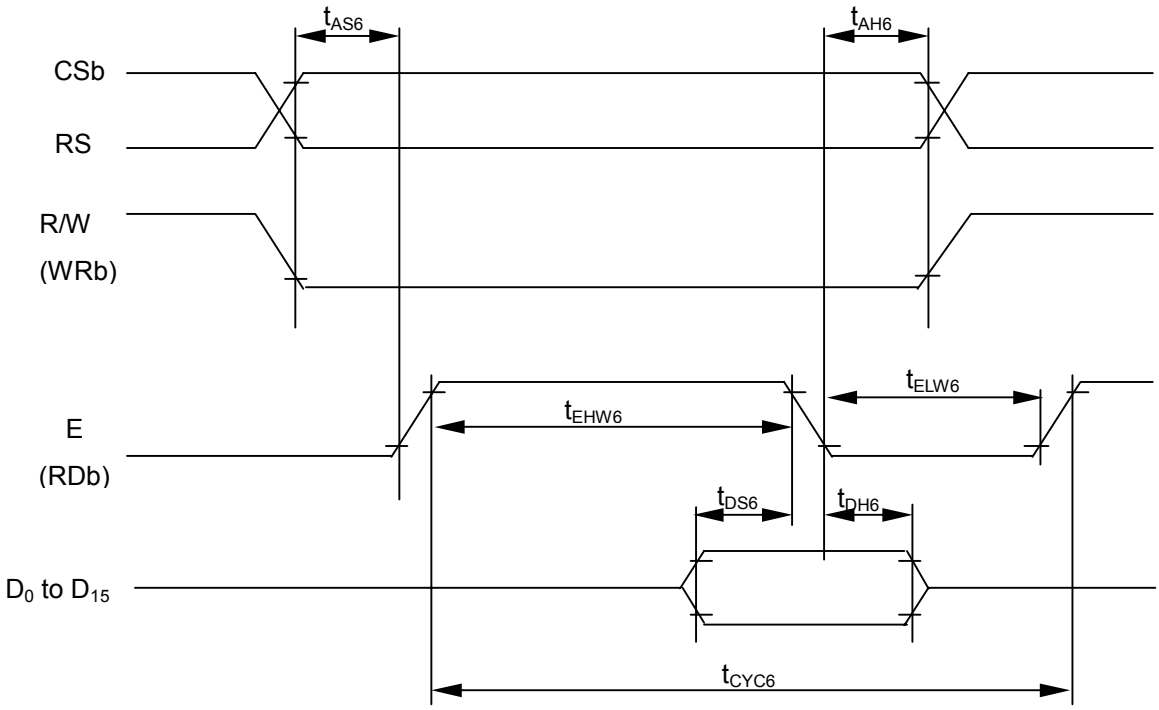
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	110	ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(3) Write Operation (Parallel Interface / 68-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		90 35 35		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

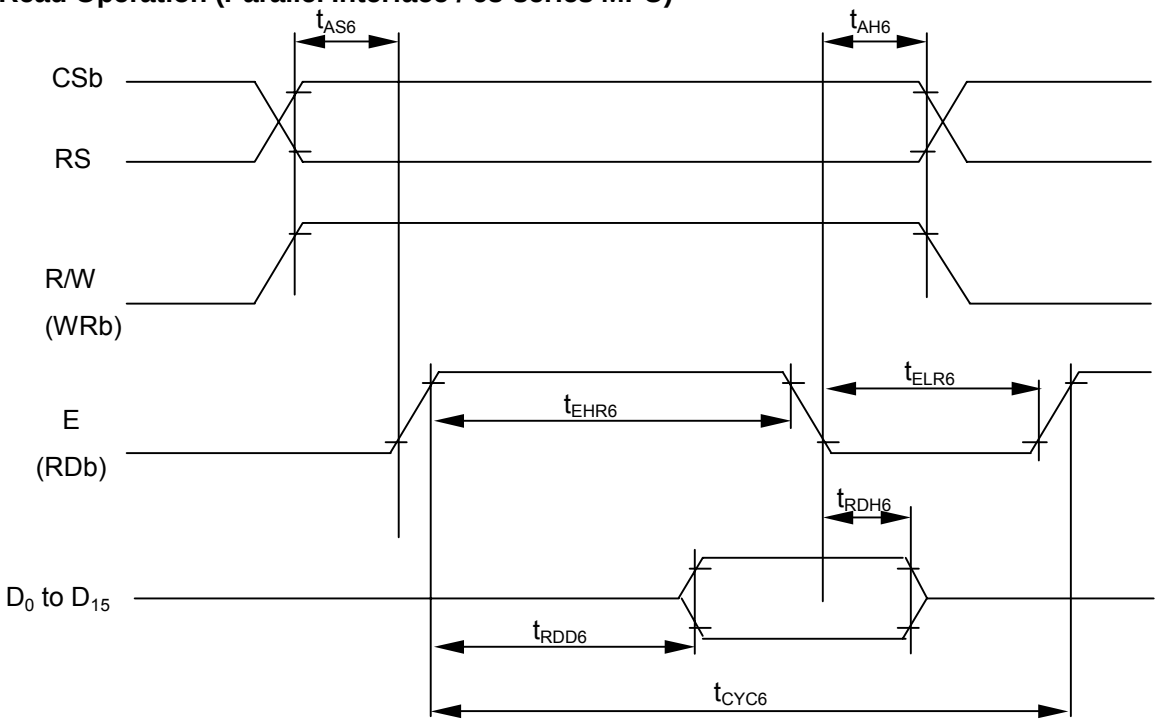
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		160 70 70		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		50 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		180 80 80		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		70 10		ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(4) Read Operation (Parallel Interface / 68-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

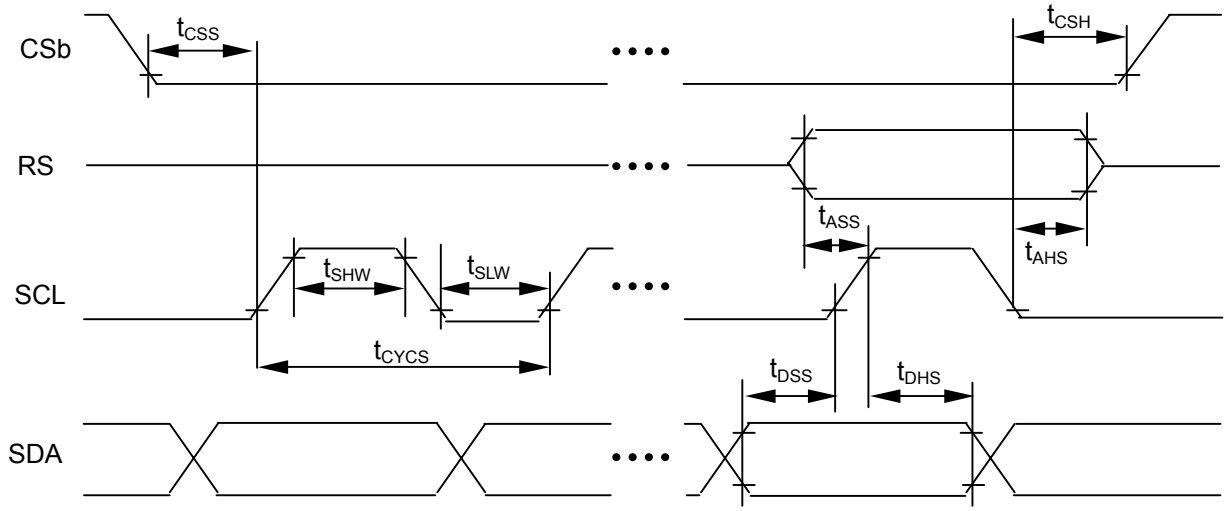
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	110	ns ns	D_0 to D_{15}

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(5) Write Operation (Serial Interface)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

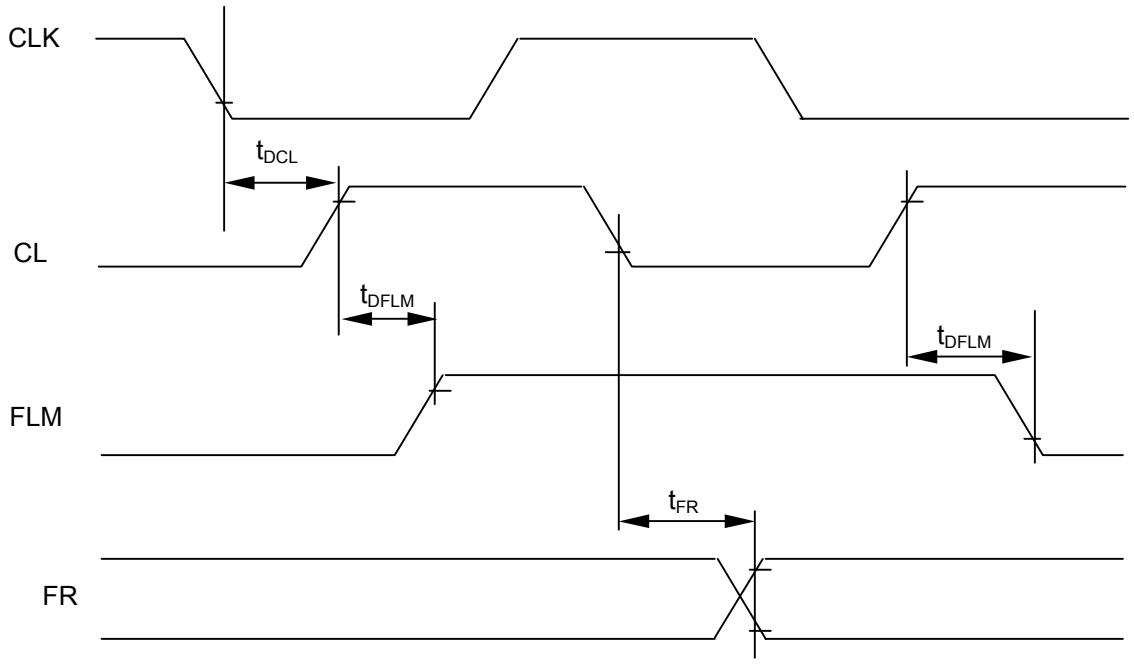
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(6) Display Control Timing



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

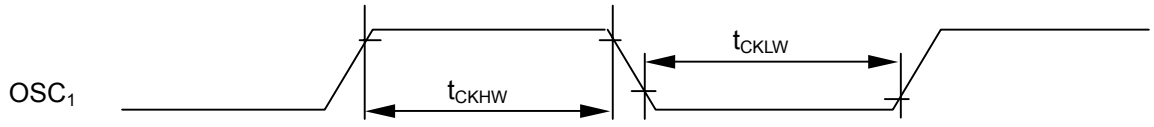
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(7) Input Clock Timing

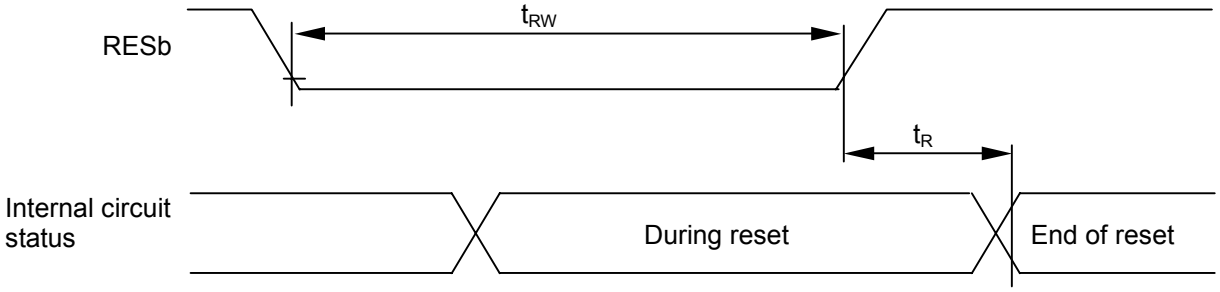


(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 “H” level pulse width (1)	t_{CKHW1}		2.27	3.29	µs	OSC1 (NOTE2)
OSC1 “L” level pulse width (1)	t_{CKLW1}		2.27	3.29	µs	
OSC1 “H” level pulse width (2)	t_{CKHW2}		10	14.7	µs	OSC1 (NOTE3)
OSC1 “L” level pulse width (2)	t_{CKLW2}		10	14.7	µs	
OSC1 “H” level pulse width (3)	t_{CKHW3}		70	103	µs	OSC1 (NOTE4)
OSC1 “L” level pulse width (3)	t_{CKLW3}		70	103	µs	

NOTE1) Each timing is specified based on 20% and 80% of V_{DD}.
NOTE2) Applied to Variable 8-/16-level grayscale mode (MON=”0”,PWM=”0”)
NOTE3) Applied to fixed 8-level grayscale mode (MON=”0”,PWM=”1”)
NOTE4) Applied to B&W mode (MON=”1”)

(8) Reset Input Timing



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb “L” level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb “L” level pulse width	t_{RW}		10.0		µs	RESb

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

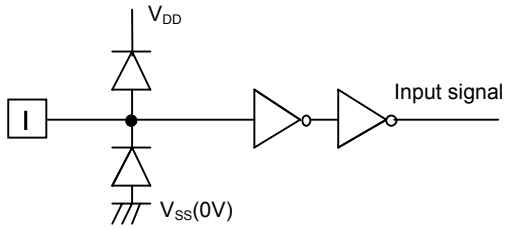
(9) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

■ INPUT/OUTPUT BLOCK DIAGRAMS

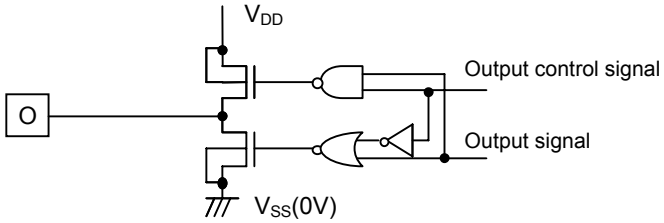
Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



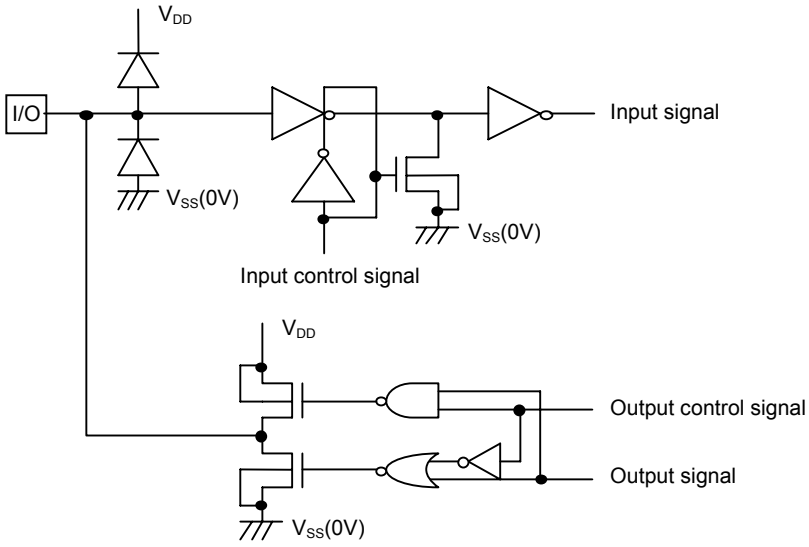
Output Block Diagram

Terminals : FLM, CL, FR, CLK



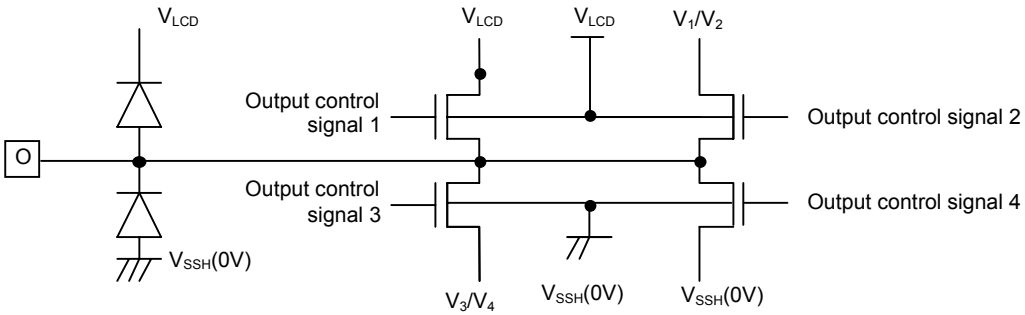
Input/Output Block Diagram

Terminals : D_0 - D_{15}



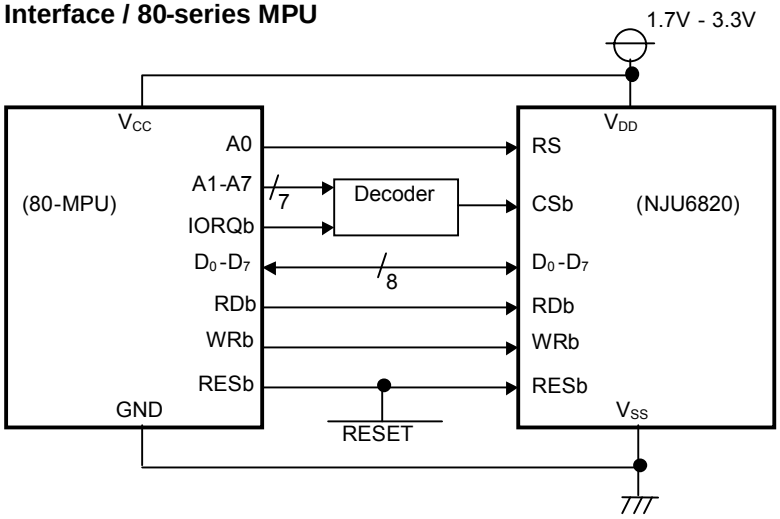
COM/SEG Driver Block Diagram

Terminals : $SEGA_0/B_0/C_0$ – $SEGA_{127}/B_{127}/C_{127}$, COM_0 – COM_{39}

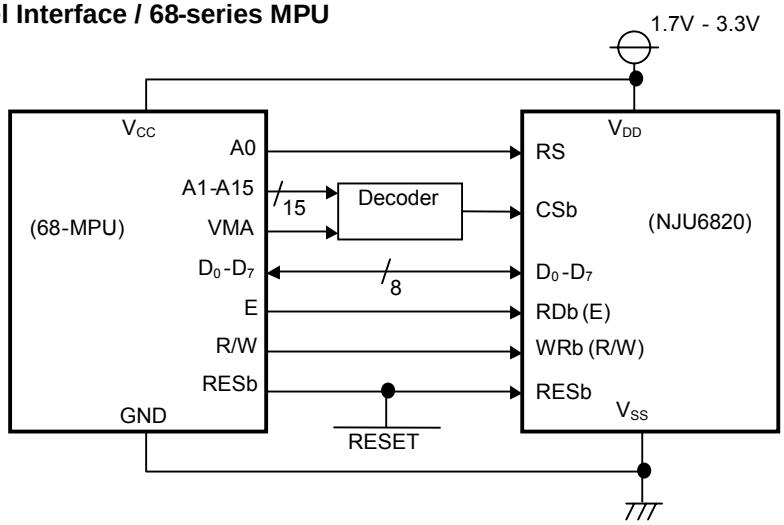


■ MPU CONNECTIONS

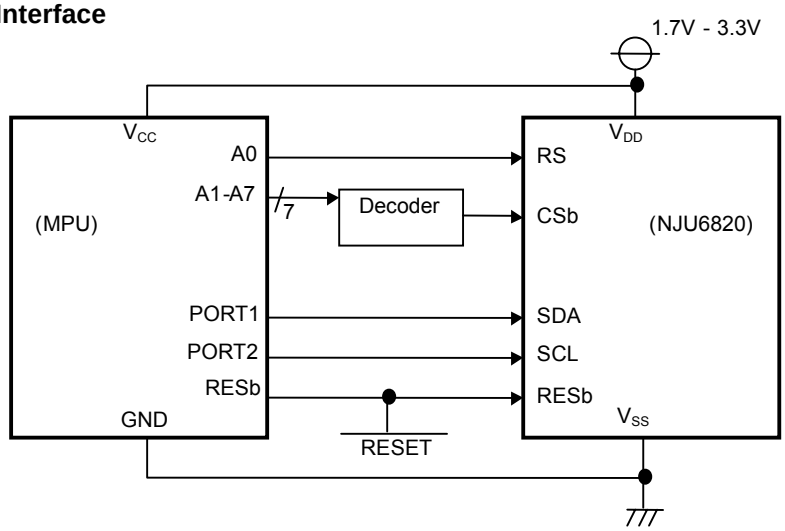
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



[CAUTION]
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