
OKI Semiconductor

MR53V3203J**Preliminary**

2,097,152-Word X 16-Bit MASK ROM

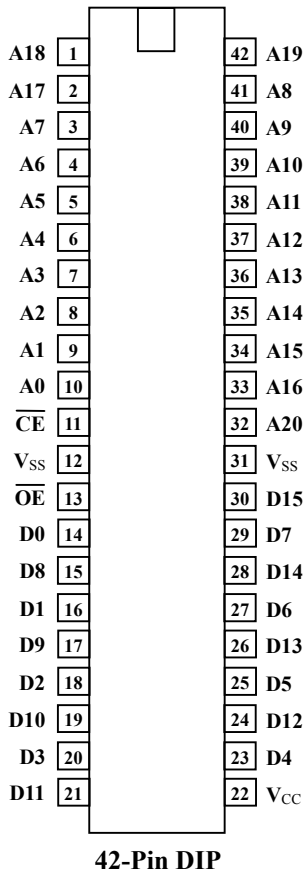
DESCRIPTION

The MR53V3203J is a 32Mbit Read-Only Memory whose configuration can is 2,097,152 word x 16bit. The MR53V3203J operates asynchronously, external clocks are not required, making this device easy-to-use. The MR53V3203J is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS silicon gate technology and is offered in 42-pin DIP

FEATURES

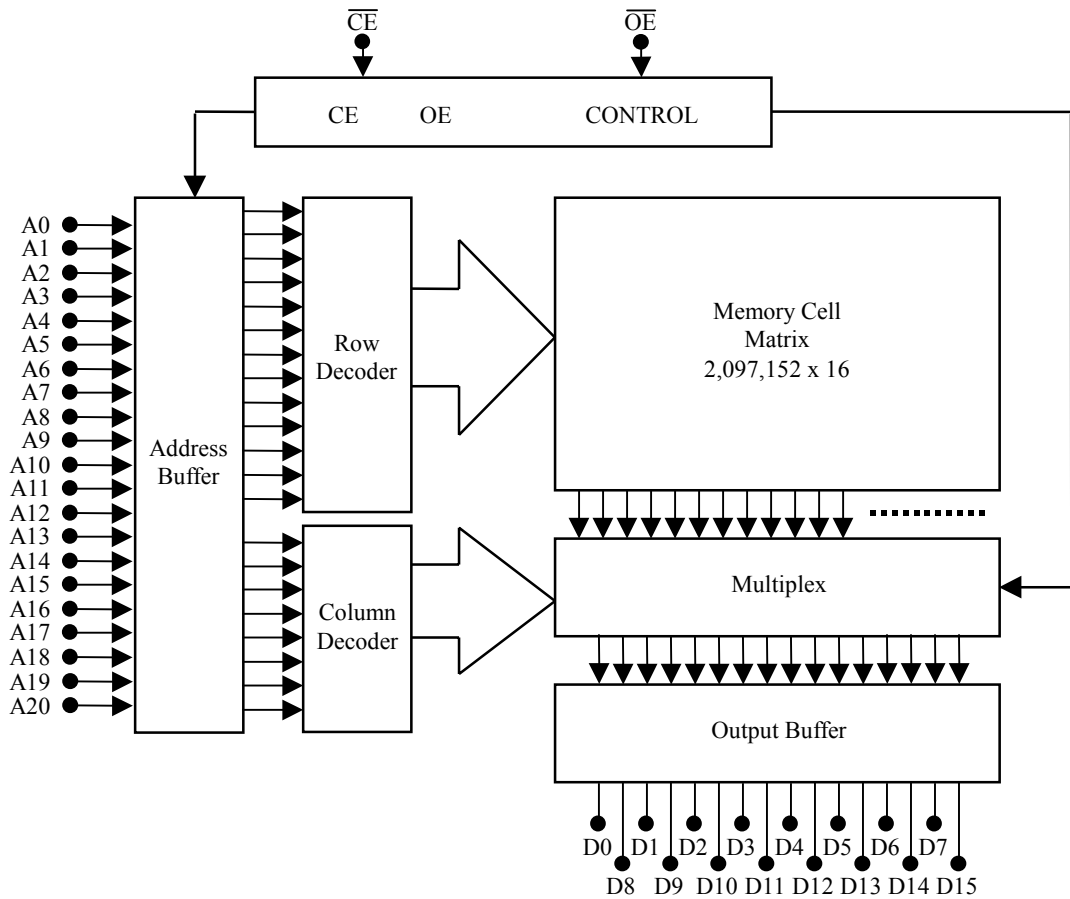
- 2,097,152 word x 16bit configuration
- Single +2.7V~3.6V power supply
- Access time 100ns (@Vcc=3.0V~3.6V)
 120ns (@Vcc=2.7V~3.3V)
- V_{CC} power supply current 40mA (@Vcc=3.0V~3.6V)
 30mA (@Vcc=2.7V~3.3V)
- V_{CC} standby current 10μA
- Input / Output TTL compatible
- Three-state output
- Packages
 42-pin plastic DIP (DIP42-P-600-2.54) MR53V3203J-XXRA

PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
A0~A20	Address input
D0~D15	Data output
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power supply voltage
V _{SS}	GND

BLOCK DIAGRAM



FUNCTION TABLE

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0~D15
STAND BY	H	X	Hi-Z
OUTPUT DISABLE	L	H	Hi-Z
READ	L	L	D _{OUT}

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T _{OPR}	-	0 ~ 70	°C
Storage temperature	T _{STG}	-	-55 ~ 125	°C
Input voltage	V _I	Relative to V _{SS}	-0.5 ~ V _{CC} +0.5	V
Output voltage	V _O		-0.5 ~ V _{CC} +0.5	V
Power supply voltage	V _{CC}		-0.5 ~ 5	V
Power dissipation per package	P _D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 ~ 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
V _{CC} power supply voltage	V _{CC}	V _{CC} =2.7V ~ 3.6V	2.7	-	3.6	°C
Input "H" level	V _{IH}		2.2	-	V _{CC} +0.5	°C
Input "L" level	V _{IL}		-0.5	-	0.8	V

Voltage is relative to V_{SS}

PIN Capacitance

(V_{CC}=3.3V, Ta=25°C, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input	C _{IN}	V _I =0V	-	-	12	pF
Output	C _{OUT}	V _O =0V	-	-	15	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics 1

(V_{CC}=2.7V~3.3V, Ta=0~70°C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input leakage current	C _{IN}	V _I =0V~V _{CC}	-	-	10	μA
Output leakage current	C _{OUT}	V _O =0V~V _{CC}	-	-	10	μA
V _{CC} power supply current (Standby)	I _{CCSC}	$\overline{CE}=V_{CC}$	-	-	10	μA
	I _{CCST}	$\overline{CE}=V_{IH}$	-	-	1	mA
V _{CC} power supply current (Active)	I _{CCA}	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc= 120ns	-	-	30	mA
Input “H” level	V _{IH}	-	2.0	-	V _{CC} +0.5	V
Input “L” level	V _{IL}	-	-0.5	-	0.8	V
Output “H” level	V _{OH}	I _{OH} =-200 μA	V _{CC} -0.4	-	-	V
Output “L” level	V _{OL}	I _{OL} =1mA	-	-	0.4	V

Voltage is relative to V_{SS}

DC Characteristics 2

(V_{CC}=3.0V~3.6V, Ta=0~70°C)

Parameter	Symbol	Condition	Min.	Typ.	Min.	Unit
Input leakage current	C _{IN}	V _I =0V~V _{CC}	-	-	10	μA
Output leakage current	C _{OUT}	V _O =0V~V _{CC}	-	-	10	μA
V _{CC} power supply current (Standby)	I _{CCSC}	$\overline{CE}=V_{CC}$	-	-	10	μA
	I _{CCST}	$\overline{CE}=V_{IH}$	-	-	1	mA
V _{CC} power supply current (Active)	I _{CCA}	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ tc= 100ns	-	-	40	mA
Input “H” level	V _{IH}	-	2.0	-	V _{CC} +0.5	V
Input “L” level	V _{IL}	-	-0.5	-	0.8	V
Output “H” level	V _{OH}	I _{OH} =-200 μA	V _{CC} -0.4	-	-	V
Output “L” level	V _{OL}	I _{OL} =1mA	-	-	0.4	V

Voltage is relative to V_{SS}

AC Characteristics 1

(V_{CC}=2.7V~3.3V, T_a=0~70°C)

Parameter	Symbol	Condition	Min.	Min.	Unit
Address access cycle time	T _C	-	120	-	ns
Address access time	T _{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	120	ns
$\overline{CE}$ access time	T _{CE}	$\overline{OE}=V_{IL}$	-	120	ns
$\overline{OE}$ access time	T _{OE}	$\overline{CE}=V_{IL}$	-	40	ns
Output disable time	T _{CHZ}	$\overline{OE}=V_{IL}$	0	35	ns
	T _{OHZ}	$\overline{CE}=V_{IL}$	0	30	ns
Output hold time	T _{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

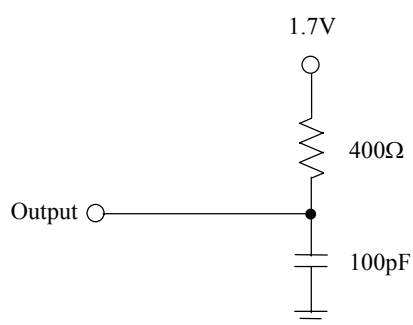
AC Characteristics 2

(V_{CC}=3.0V~3.6V, T_a=0~70°C)

Parameter	Symbol	Condition	Min.	Min.	Unit
Address access cycle time	T _C	-	100	-	ns
Address access time	T _{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	100	ns
$\overline{CE}$ access time	T _{CE}	$\overline{OE}=V_{IL}$	-	100	ns
$\overline{OE}$ access time	T _{OE}	$\overline{CE}=V_{IL}$	-	30	ns
Output disable time	T _{CHZ}	$\overline{OE}=V_{IL}$	0	30	ns
	T _{OHZ}	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T _{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

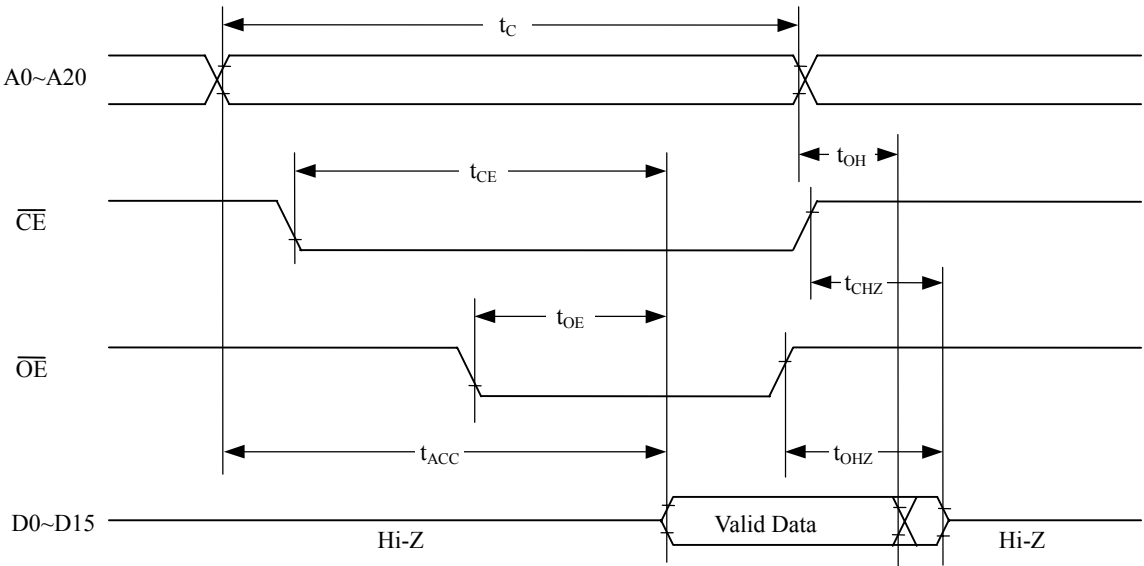
Measurement condition

Input signal level	0V/3V
Input timing reference level	0.8V/2.0V
Output load	100pF
Output timing reference level	0.8V/2.0V



TIMING CHART

16BIT READ MODE



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People To People Technology

ADDRESSES & SEMICONDUCTOR WEB SITES

OKI Electric Industry Co., Ltd.,

Device Business Group,
10-3, Shibaura, 4-chome,
Minato-ku, Tokyo 108, Japan,
Tel.: +81-(0)3-5445-6327,
Fax.: +81-(0)3-5445-6328,
<http://www.oki.co.jp/semi/>

OKI Semiconductor Group,

785 North Mary Avenue,
Sunnyvale, CA 94086, U.S.A.,
Tel.: +1-408-720-1900,
Fax.: +1-408-720-1918,
<http://www.okisemi.com/>

OKI Electric Europe GmbH,

Head Office Europe,
Hellersbergstrasse 2,
D-41460 Neuss, Germany,
Tel: +49-2131-15960,
Fax: +49-2131-103539,
<http://www.oki-europe.de/>

OKI Electronics (Hong Kong) Ltd.,

Suite 1901-1&19, Tower 3,
China Hong Kong City,
33 Canton Road, Tsimshatsui,
Kowloon, Hong Kong,
Tel.: +852-2-736-2336,
Fax.: +852-2-736-2395

OKI Semiconductor (Asia) Pte. Ltd.,

78 Shenton Way 09-01,
Singapore 0207,
Tel.: +65-221-3722,
Fax.: +65-323-5376

OKI Semiconductor (Asia) Pte. Ltd.,

Taipei Branch,
7th Fl. No.260, Tun Hwa North Road,
Taipei, Taiwan, R.O.C.,
Sumitomo-Flysun Building,
Tel.: +886-2-2719-2561,
Fax.: +886-2-2715-2892
<http://www.oki.net.tw/>

For further information, please contact: