

# MAXIM

## DBS Direct Downconverter

MAX2114

### General Description

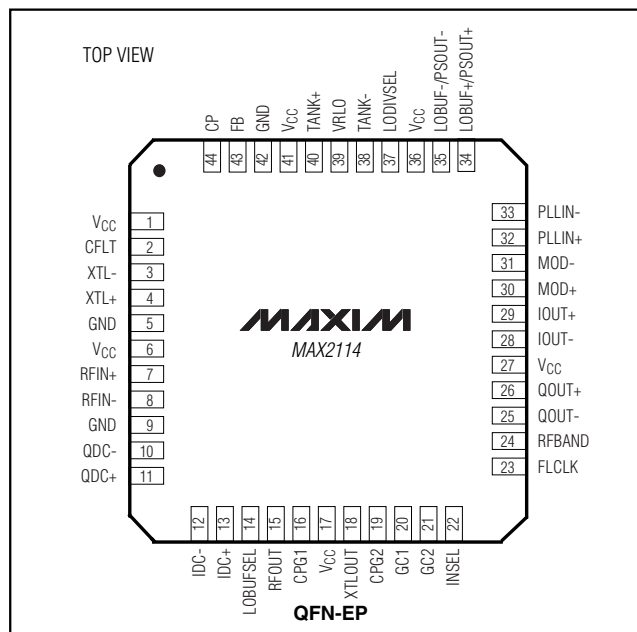
The MAX2114 low-cost, direct-conversion tuner is designed for use in digital direct-broadcast satellite (DBS) television set-top box units. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures. The MAX2114 directly tunes L-band signals to baseband using a broadband I/Q downconverter. The operating frequency range spans 925MHz to 2175MHz.

The MAX2114 includes a low-noise amplifier (LNA) with gain control, I and Q downconverting mixers, lowpass filters with gain and frequency control, a local oscillator (LO) buffer with a 90° quadrature network, and a charge-pump-based phase-locked loop (PLL) for frequency control. The MAX2114 has an on-chip LO, requiring only an external varactor-tuned LC tank for operation. The LO's output drives the internal quadrature generator and has a buffer amplifier to drive off-chip circuitry. The MAX2114 comes in a 44-pin QFN package with exposed paddle (EP).

### Applications

|                                |                        |
|--------------------------------|------------------------|
| U.S. DSS Set-Top Receivers     | Broadband Systems      |
| European DVB-Compliant Systems | LMDS                   |
| Cellular Base Stations         | Professional Receivers |
| Wireless Local Loop            | VSAT                   |
|                                | Microwave Links        |

### Pin Configuration



### Features

- ◆ Complete Low-Cost Solution for DBS Direct Downconversion
- ◆ High Level of Integration Minimizes Component Count
- ◆ 1MBaud to 45MBaud Operation
- ◆ Selectable LO Buffer
- ◆ +5V Single-Supply Operation
- ◆ 925MHz to 2175MHz Input Frequency Range
- ◆ On-Chip Quadrature Generator, Dual-Modulus Prescaler (/32, /33)
- ◆ On-Chip Crystal Oscillator Amplifier
- ◆ PLL Phase Detector with Gain-Controlled Charge Pump
- ◆ Input Levels: -25dBm to -68dBm per Carrier
- ◆ Over 50dB Gain Control Range
- ◆ Noise Figure = 10.6dB; IIP3 = +10.7dBm (at 1550MHz)
- ◆ Automatic Baseband Offset Correction

### Ordering Information

| PART       | TEMP. RANGE  | PIN-PACKAGE |
|------------|--------------|-------------|
| MAX2114UGH | 0°C to +85°C | 44 QFN-EP*  |

\*Exposed paddle

Functional Diagram appears at end of data sheet.

MAXIM

Maxim Integrated Products 1

For price, delivery, and to place orders, please contact Maxim Distribution at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).

# DBS Direct Downconverter

## ABSOLUTE MAXIMUM RATINGS

V<sub>CC</sub> to GND .....-0.3V to +7V  
 All Other Pins to GND .....-0.3V to (V<sub>CC</sub> + 0.3V)  
 RFIN+ to RFIN-, TANK+ to TANK-,  
 IDC+ to IDC-, QDC+ to QDC- .....±2V  
 IOUT-, QOUT- to GND Short-Circuit Duration .....10s  
 LOBUF+/PSOUT+, LOBUF-/PSOUT- Short-Circuit Duration ..10s  
 VRLO Short-Circuit Duration .....0s

Continuous Current (any pin other than V<sub>CC</sub> or GND) .....20mA  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 44-Pin QFN-EP (derate 27mW/°C above +70°C) .....1.8W  
 Operating Temperature .....0°C to +85°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +4.75V to +5.25V, V<sub>FB</sub> = +2.4V, C<sub>IOUT-</sub> = C<sub>QOUT-</sub> = 10pF, f<sub>FLCLK</sub> = 2MHz, RFIN- = unconnected, R<sub>IOUT-</sub> = R<sub>QOUT-</sub> = 10kΩ, V<sub>LOBUFSEL</sub> = +0.5V, V<sub>RFBAND</sub> = V<sub>INSEL</sub> = V<sub>CPG1</sub> = V<sub>CPG2</sub> = +2.4V, V<sub>PLLIN+</sub> = V<sub>MOD+</sub> = +1.3V, V<sub>PLLIN-</sub> = V<sub>MOD-</sub> = +1.1V, T<sub>A</sub> = +25°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +5V, unless otherwise noted.)

| PARAMETER                                                                      | SYMBOL           | CONDITIONS                                                         | MIN  | TYP | MAX  | UNITS |
|--------------------------------------------------------------------------------|------------------|--------------------------------------------------------------------|------|-----|------|-------|
| Operating Supply Voltage                                                       | V <sub>CC</sub>  |                                                                    | 4.75 |     | 5.25 | V     |
| Operating Supply Current                                                       | I <sub>CC</sub>  |                                                                    |      | 195 | 275  | mA    |
| <b>STANDARD DIGITAL INPUTS</b> (INSEL, CPG1, CPG2, LOBUFSEL, LODIVSEL, RFBAND) |                  |                                                                    |      |     |      |       |
| Input Voltage High                                                             | V <sub>IH</sub>  |                                                                    | 2.4  |     |      | V     |
| Input Voltage Low                                                              | V <sub>IL</sub>  |                                                                    |      |     | 0.5  | V     |
| Input Current                                                                  | I <sub>IN</sub>  |                                                                    | -15  |     | 10   | μA    |
| RFBAND Input Current                                                           |                  |                                                                    | -200 |     | 200  | μA    |
| <b>SLEW-RATE-LIMITED DIGITAL INPUT</b> (f <sub>FLCLK</sub> )                   |                  |                                                                    |      |     |      |       |
| FLCLK Input Voltage High                                                       |                  |                                                                    | 1.85 |     |      | V     |
| FLCLK Input Voltage Low                                                        |                  |                                                                    |      |     | 1.45 | V     |
| FLCLK Input Current (Note 1)                                                   |                  | R <sub>SOURCE</sub> = 50kΩ, V <sub>FLCLK</sub> = 1.65V             | -1   |     | 1    | μA    |
| <b>DIFFERENTIAL DIGITAL INPUTS</b> (MOD+, MOD-, PLLIN+, PLLIN-)                |                  |                                                                    |      |     |      |       |
| Common-Mode Input Voltage                                                      | V <sub>CM1</sub> |                                                                    | 1.08 | 1.2 | 1.32 | V     |
| Input Voltage Low                                                              |                  | Referenced to V <sub>CM1</sub>                                     |      |     | -100 | mV    |
| Input Voltage High                                                             |                  | Referenced to V <sub>CM1</sub>                                     | 100  |     |      | mV    |
| Input Current (Note 1)                                                         |                  |                                                                    | -5   |     | 5    | μA    |
| <b>DIFFERENTIAL DIGITAL OUTPUTS</b> (LOBUF+/PSOUT+, LOBUF-/PSOUT-)             |                  |                                                                    |      |     |      |       |
| Common-Mode Output Voltage                                                     | V <sub>CMO</sub> |                                                                    | 2.16 | 2.4 | 2.64 | V     |
| Output Voltage Low (Note 2)                                                    |                  | Referenced to V <sub>CMO</sub> , LOBUFSEL ≤ 0.5V                   |      |     | -150 | mV    |
| Output Voltage High (Note 2)                                                   |                  | Referenced to V <sub>CMO</sub> , LOBUFSEL ≤ 0.5V                   | 150  |     |      | mV    |
| <b>FREQUENCY SYNTHESIZER/LO BUFFER</b>                                         |                  |                                                                    |      |     |      |       |
| Prescaler Ratio                                                                |                  | (V <sub>MOD+</sub> - V <sub>MOD-</sub> ) ≥ 200mV, LOBUFSEL ≤ 0.5V  | 32   |     | 32   |       |
|                                                                                |                  | (V <sub>MOD+</sub> - V <sub>MOD-</sub> ) ≤ -200mV, LOBUFSEL ≤ 0.5V | 33   |     | 33   |       |
|                                                                                |                  | LOBUFSEL ≥ 2.4V, LODIVSEL ≤ 0.5V                                   | 2    |     | 2    |       |
|                                                                                |                  | LOBUFSEL ≥ 2.4V, LODIVSEL ≥ 2.4V                                   | 1    |     | 1    |       |
| Reference Divider Ratio                                                        |                  |                                                                    | 8    |     | 8    |       |
| XTLOUT Output DC Voltage                                                       |                  |                                                                    |      | 1.9 |      | V     |
| Charge-Pump Output High<br>Measured at FB                                      |                  | V <sub>CPG1</sub> ≤ 0.5V, V <sub>CPG2</sub> ≤ 0.5V                 | 0.08 | 0.1 | 0.12 | mA    |
|                                                                                |                  | V <sub>CPG1</sub> ≤ 0.5V, V <sub>CPG2</sub> ≥ 2.4V                 | 0.24 | 0.3 | 0.36 |       |
|                                                                                |                  | V <sub>CPG1</sub> ≥ 2.4V, V <sub>CPG2</sub> ≤ 0.5V                 | 0.48 | 0.6 | 0.72 |       |
|                                                                                |                  | V <sub>CPG1</sub> ≥ 2.4V, V <sub>CPG2</sub> ≥ 2.4V                 | 1.44 | 1.8 | 2.16 |       |

# DBS Direct Downconverter

MAX2114

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +4.75V$  to  $+5.25V$ ,  $V_{FB} = +2.4V$ ,  $C_{IOUT\_} = C_{QOUT\_} = 10pF$ ,  $f_{FLCLK} = 2MHz$ ,  $R_{FIN\_} =$  unconnected,  $R_{IOUT\_} = R_{QOUT\_} = 10k\Omega$ ,  $V_{LOBUSEL} = +0.5V$ ,  $V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V$ ,  $V_{PLLIN+} = V_{MOD+} = +1.3V$ ,  $V_{PLLIN-} = V_{MOD-} = +1.1V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5V$ , unless otherwise noted.)

| PARAMETER                                                | SYMBOL     | CONDITIONS                                  | MIN   | TYP  | MAX   | UNITS   |
|----------------------------------------------------------|------------|---------------------------------------------|-------|------|-------|---------|
| Charge-Pump Output Low Measured at FB                    |            | $V_{CPG1} \leq 0.5V$ , $V_{CPG2} \leq 0.5V$ | -0.12 | -0.1 | -0.08 | mA      |
|                                                          |            | $V_{CPG1} \leq 0.5V$ , $V_{CPG2} \geq 2.4V$ | -0.36 | -0.3 | -0.24 |         |
|                                                          |            | $V_{CPG1} \geq 2.4V$ , $V_{CPG2} \leq 0.5V$ | -0.72 | -0.6 | -0.48 |         |
|                                                          |            | $V_{CPG1} \geq 2.4V$ , $V_{CPG2} \geq 2.4V$ | -2.16 | -1.8 | -1.44 |         |
| Charge-Pump Output Current Matching Positive to Negative |            | Measured at FB                              | -5    |      | 5     | %       |
| Charge-Pump Output Leakage                               |            | Measured at FB                              | -25   |      | 25    | nA      |
| Charge-Pump Output Current Drive (Note 1)                |            | Measured at CP                              | 100   |      |       | $\mu A$ |
| <b>ANALOG CONTROL INPUTS</b> (GC1, GC2)                  |            |                                             |       |      |       |         |
| Input Current                                            | $I_{GC\_}$ | $V_{GC\_} = 1V$ to $4V$                     | -50   |      | 50    | $\mu A$ |
| <b>BASEBAND OUTPUTS</b> (IOUT+, IOUT-, QOUT+, QOUT-)     |            |                                             |       |      |       |         |
| Differential Output Voltage Swing                        |            | $R_L = 2k\Omega$ differential               | 1     |      |       | Vp-p    |
| Common-Mode Output Voltage (Note 1)                      |            |                                             | 0.65  |      | 0.85  | V       |
| Offset Voltage (Note 1)                                  |            |                                             | -50   |      | 50    | mV      |

## AC ELECTRICAL CHARACTERISTICS

(IC driven single-ended with  $R_{FIN\_}$  AC-terminated in  $75\Omega$  to GND,  $V_{CC} = +4.75V$  to  $+5.25V$ ,  $V_{IOUT\_} = V_{QOUT\_} = 0.59V_{p-p}$ ,  $C_{IOUT\_} = C_{QOUT\_} = 10pF$ ,  $f_{CLK} = 500kHz$ ,  $R_{IOUT\_} = R_{QOUT\_} = 10k\Omega$ ,  $V_{LOBUSEL} = 0.5V$ ,  $V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V$ ,  $V_{PLLIN+} = V_{MOD+} = +1.3V$ ,  $V_{PLLIN-} = V_{MOD-} = +1.1V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{CC} = +5V$ .)

| PARAMETER                                        | SYMBOL         | CONDITIONS                                                                           | MIN                                  | TYP  | MAX  | UNITS |
|--------------------------------------------------|----------------|--------------------------------------------------------------------------------------|--------------------------------------|------|------|-------|
| RFIN_ Input Frequency Range                      | $f_{RFIN\_}$   | Inferred by quadrature gain and phase-error test                                     | 925                                  |      | 2175 | MHz   |
| RFIN_ Input Power for 0.59Vp-p Baseband Levels   |                | Single carrier                                                                       | $V_{GC1} = V_{GC2} = +4V$ (min gain) | -25  |      | dBm   |
|                                                  |                |                                                                                      | $V_{GC1} = V_{GC2} = +1V$ (max gain) |      | -68  |       |
| RFIN_ Input Third-Order Intercept Point (Note 3) | $IP3_{RFIN\_}$ | $PR_{FIN\_} = -25dBm$ per tone                                                       | $f_{LO} = 2175MHz$                   | 8.0  |      | dBm   |
|                                                  |                |                                                                                      | $f_{LO} = 1550MHz$                   | 10.7 |      |       |
|                                                  |                |                                                                                      | $f_{LO} = 950MHz$                    | 11.1 |      |       |
|                                                  |                | $PR_{FIN\_} = -65dBm$ per tone                                                       | $f_{LO} = 2175MHz$                   | -29  |      |       |
|                                                  |                |                                                                                      | $f_{LO} = 1550MHz$                   | -26  |      |       |
|                                                  |                |                                                                                      | $f_{LO} = 950MHz$                    | -30  |      |       |
| RFIN_ Input Second-Order Intercept (Note 4)      | $IP2_{RFIN\_}$ | $PR_{FIN\_} = -25dBm$ per tone, $f_{LO} = 951MHz$                                    |                                      | 16.1 |      | dBm   |
| Output-Referred 1dB Compression Point (Note 5)   | $P1_{dBOUT}$   | $PR_{FIN\_} = -40dBm$ , signals within filter bandwidth                              |                                      | 2    |      | dBV   |
| Noise Figure                                     | NF             | $f_{RFIN\_} = 1550MHz$ , $V_{GC1} = 1V$ , $V_{GC2}$ adjusted 0.59Vp-p baseband level | $PR_{FIN\_} = -65dBm$                | 10.6 |      | dB    |
|                                                  |                |                                                                                      | $PR_{FIN\_} = -25dBm$                | 44.8 |      |       |

# DBS Direct Downconverter

## AC ELECTRICAL CHARACTERISTICS (continued)

(R<sub>FIN+</sub> IC driven single-ended with R<sub>FIN-</sub> AC-terminated in 75Ω to GND, V<sub>CC</sub> = +4.75V to +5.25V, V<sub>IOUT-</sub> = V<sub>QOUT-</sub> = 0.59Vp-p, C<sub>IOUT-</sub> = C<sub>QOUT-</sub> = 10pF, f<sub>CLK</sub> = 500kHz, R<sub>IOUT-</sub> = R<sub>QOUT-</sub> = 10kΩ, V<sub>LOBUSEL</sub> = 0.5V, V<sub>RFBAND</sub> = V<sub>INSEL</sub> = V<sub>CPG1</sub> = V<sub>CPG2</sub> = +2.4V, V<sub>PLLIN+</sub> = V<sub>MOD+</sub> = +1.3V, V<sub>PLLIN-</sub> = V<sub>MOD-</sub> = +1.1V, T<sub>A</sub> = +25°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = +5V.)

| PARAMETER                                           | SYMBOL | CONDITIONS                                                                           | MIN  | TYP  | MAX | UNITS   |
|-----------------------------------------------------|--------|--------------------------------------------------------------------------------------|------|------|-----|---------|
| R <sub>FIN+</sub> Return Loss (Note 6)              |        | f <sub>RFIN-</sub> = 925MHz, Z <sub>SOURCE</sub> = 75Ω                               |      | +13  |     | dB      |
|                                                     |        | f <sub>RFIN-</sub> = 2175MHz, Z <sub>SOURCE</sub> = 75Ω                              |      | +14  |     |         |
| LO 2nd Harmonic Rejection (Note 7)                  |        | Average level of V <sub>IOUT-</sub> , V <sub>QOUT-</sub>                             |      | 45   |     | dB      |
| LO Half Harmonic Rejection (Note 8)                 |        | Average level of V <sub>IOUT-</sub> , V <sub>QOUT-</sub>                             |      | 43   |     | dB      |
| LO Leakage Power (Notes 6, 9)                       |        | Measured at R <sub>FIN+</sub>                                                        |      | -66  |     | dBm     |
| <b>RFOUT PORT (LOOPTHROUGH)</b>                     |        |                                                                                      |      |      |     |         |
| R <sub>FIN+</sub> to RFOUT Gain (Note 10)           |        | f = 925MHz                                                                           |      | 0.5  |     | dB      |
|                                                     |        | f = 1550MHz                                                                          |      | 1.0  |     |         |
|                                                     |        | f = 2175MHz                                                                          |      | 2.0  |     |         |
| RFOUT Output Third-Order Intercept Point (Note 10)  |        | f = 925MHz                                                                           |      | 9.5  |     | dBm     |
|                                                     |        | f = 1550MHz                                                                          |      | 7.7  |     |         |
|                                                     |        | f = 2175MHz                                                                          |      | 5.4  |     |         |
| RFOUT Noise Figure (Note 10)                        |        | f = 925MHz                                                                           |      | 12   |     | dB      |
|                                                     |        | f = 1550MHz                                                                          |      | 10.6 |     |         |
|                                                     |        | f = 2175MHz                                                                          |      | 10.8 |     |         |
| RFOUT Return Loss (Notes 6, 10)                     |        | 925MHz < f < 2175MHz, Z <sub>LOAD</sub> = 75Ω                                        |      | 12   |     | dB      |
| Output Real Impedance (Notes 1)                     |        | I <sub>OUT-</sub> , Q <sub>OUT-</sub>                                                |      |      | 50  | Ω       |
| Baseband Highpass -3dB Frequency (Note 1)           |        | C <sub>IDC-</sub> = C <sub>QDC-</sub> = 0.22μF                                       |      |      | 750 | Hz      |
| LPF -3dB Cutoff-Frequency Range (Note 1)            |        | Controlled by FLCLK signal                                                           | 8    |      | 33  | MHz     |
| Baseband Frequency Response (Note 1)                |        | Deviation from ideal 7th order, Butterworth, up to 0.7 × f <sub>C</sub>              | -0.5 |      | 0.5 | dB      |
| LPF -3dB Cutoff-Frequency Accuracy (Note 1)         |        | f <sub>FLCLK</sub> = 0.5MHz, f <sub>C</sub> = 8MHz                                   | -5.5 |      | 5.5 | %       |
|                                                     |        | f <sub>FLCLK</sub> = 1.25MHz, f <sub>C</sub> = 19.3MHz                               | -10  |      | 10  |         |
|                                                     |        | f <sub>FLCLK</sub> = 2.0625MHz, f <sub>C</sub> = 31.4MHz                             | 10   |      | 10  |         |
| Ratio of In-Filter-Band to Out-of-Filter-Band Noise |        | f <sub>IN_BAND</sub> = 100Hz to 22.5MHz, f <sub>OUT_BAND</sub> = 67.5MHz to 112.5MHz |      | 23   |     | dB      |
| Quadrature Gain Error                               |        | Includes effects from baseband filters, measured at 125kHz baseband                  |      |      | 1.2 | dB      |
| Quadrature Phase Error                              |        | Includes effects from baseband filters, measured at 125kHz baseband                  |      |      | 4   | degrees |

# DBS Direct Downconverter

MAX2114

## AC ELECTRICAL CHARACTERISTICS (continued)

(IC driven single-ended with RFIN- AC-terminated in 75Ω to GND, VCC = +4.75V to +5.25V, VIOUT\_ = VQOUT\_ = 0.59Vp-p, CIOUT\_ = CQOUT\_ = 10pF, fCLK = 500kHz, RIOUT\_ = RQOUT\_ = 10kΩ, VLOBUFSEL = 0.5V, VRFBAND = VINSEL = VCPG1 = VCPG2 = +2.4V, VPLLIN+ = VMOD+ = +1.3V, VPLLIN- = VMOD- = +1.1V, TA = +25°C, unless otherwise noted. Typical values are at VCC = +5V.)

| PARAMETER                            | SYMBOL | CONDITIONS                                   | MIN | TYP | MAX  | UNITS  |
|--------------------------------------|--------|----------------------------------------------|-----|-----|------|--------|
| <b>SYNTHESIZER</b>                   |        |                                              |     |     |      |        |
| XTLOUT Output Voltage Swing          |        | Load = 10pF    10kΩ, fXTLOUT = 4MHz          | 0.8 | 1   | 1.5  | Vp-p   |
| Crystal Frequency Range (Note 1)     |        |                                              | 4   |     | 7.26 | MHz    |
| MOD+, MOD- Setup Time (Note 1)       | tSUM   | Figure 1                                     | 7   |     |      | ns     |
| MOD+, MOD- Hold Time (Note 1)        | tHM    | Figure 1                                     | 0   |     |      | ns     |
| <b>LOCAL OSCILLATOR</b>              |        |                                              |     |     |      |        |
| LO Tuning Range (Note 11)            |        |                                              | 590 |     | 1180 | MHz    |
| LO Buffer Output Voltage (Note 1)    |        | VLOBUFSEL ≥ 2.4V,<br>fLO = 925 MHz + 2175MHz | 70  |     |      | mVRMS  |
| LO Phase Noise (Notes 6, 12)         |        | At 1kHz offset, fLO = 2175MHz                |     | -60 |      | dBc/Hz |
|                                      |        | At 10kHz offset, fLO = 2175MHz               |     | -75 |      |        |
|                                      |        | At 100kHz offset, fLO = 2175MHz              |     | -96 |      |        |
| RFIN+ to LO Input Isolation (Note 9) |        | fRFIN = 2175MHz                              |     | 58  |      | dB     |

**Note 1:** Minimum and maximum values are guaranteed by design and characterization over supply voltage.

**Note 2:** Driving differential load of 10kΩ || 15pF.

**Note 3:** Two signals are applied to RFIN\_ at (fLO - 100MHz) and (fLO - 199MHz). VGC2 = 1V, VGC1 is set so that the baseband outputs are at 590mVp-p. IM products are measured at baseband outputs but are referred to RF inputs.

**Note 4:** Two signals are applied to RFIN\_ at 1200MHz and 2150MHz. VGC2 = 1V, VGC1 is set so that the baseband outputs are at 590mVp-p. IM products are measured at baseband outputs but are referred to RF inputs.

**Note 5:** PRFIN\_ = -40dBm so that front-end IM contributions are minimized.

**Note 6:** Using L64733/L64734 demo board from LSI Logic.

**Note 7:** Downconverted level, in dBc, of carrier present at fLO × 2, fLO = 1180MHz, fVCO = 590MHz, VRFBAND = unconnected.

**Note 8:** Downconverted level, in dBc, of carrier present at fO / 2, fLO = 2175MHz, fVCO = 1087.5MHz, VRFBAND = 2.4V.

**Note 9:** Leakage is dominated by board parasitics.

**Note 10:** VCPG1 = VCPG2 = VRFBAND = VINSEL = 0.5V, fCLK = 0.5MHz.

**Note 11:** Guaranteed by design and characterization over supply and temperature.

**Note 12:** Measured at tuned frequency with PLL locked. PLL loop bandwidth = 3kHz. All phase noise measurements assume tank components have a Q > 50.

# DBS Direct Downconverter

## Pin Description

| PIN                  | NAME            | FUNCTION                                                                                                                                                                                                          |
|----------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 6, 17, 27, 36, 41 | V <sub>CC</sub> | V <sub>CC</sub> Power-Supply Input. Connect each pin to a +5V $\pm$ 5% low-noise supply. Bypass each V <sub>CC</sub> pin to the nearest GND with a ceramic chip capacitor.                                        |
| 2                    | CFLT            | External Bypass for Internal Bias. Bypass this pin with a 0.22 $\mu$ F ceramic chip capacitor to GND.                                                                                                             |
| 3                    | XTL-            | Inverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.                                                                                                             |
| 4                    | XTL+            | Noninverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.                                                                                                          |
| 5, 9, 42             | GND             | Ground. Connect each of these pins to a solid ground plane. Use multiple vias to reduce inductance where possible.                                                                                                |
| 7                    | RFIN-           | RF Inverting Input. Bypass RFIN- with 47pF capacitor in series with a 75 $\Omega$ resistor to GND.                                                                                                                |
| 8                    | RFIN+           | RF Noninverting Input. Connect to 75 $\Omega$ source with a 47pF ceramic chip capacitor.                                                                                                                          |
| 10                   | QDC-            | Baseband Offset Correction. Connect a 0.22 $\mu$ F ceramic chip capacitor from QDC- to QDC+ (pin 11).                                                                                                             |
| 11                   | QDC+            | Baseband Offset Correction. Connect a 0.22 $\mu$ F ceramic chip capacitor from QDC+ to QDC- (pin 10).                                                                                                             |
| 12                   | IDC-            | Baseband Offset Correction. Connect a 0.22 $\mu$ F ceramic chip capacitor from IDC- to IDC+ (pin 13).                                                                                                             |
| 13                   | IDC+            | Baseband Offset Correction. Connect a 0.22 $\mu$ F ceramic chip capacitor from IDC+ to IDC- (pin 12).                                                                                                             |
| 14                   | LOBUFSEL        | Local Oscillator Buffer Select. Connect to GND to select DIV32/33 prescaler output; connect V <sub>CC</sub> to DIV1 to select DIV2 LO buffer output.                                                              |
| 15                   | RFOUT           | Buffered RF Output. Enabled when INSEL is low.                                                                                                                                                                    |
| 16                   | CPG1            | Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See <i>DC Electrical Characteristics</i> for available gain settings.                                                 |
| 18                   | XTLOUT          | Buffered Crystal Oscillator Output                                                                                                                                                                                |
| 19                   | CPG2            | Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See <i>DC Electrical Characteristics</i> for available gain settings.                                                 |
| 20                   | GC1             | Gain Control Input for RF Front End. High-impedance analog input, with an input range of +1V to +4V. See <i>AC Electrical Characteristics</i> for transfer function.                                              |
| 21                   | GC2             | Gain Control Input for Baseband Signals. High-impedance analog input, with an input range of +1V to +4V. See <i>AC Electrical Characteristics</i> for transfer function.                                          |
| 22                   | INSEL           | Loophrough Mode Enable. High-impedance digital input. Drive low to enable the RFOUT buffer and disable the LO converters. Drive high for normal tuner operation.                                                  |
| 23                   | FLCLK           | Baseband Filter Cutoff Adjust. Connect to a slew-rate-limited clock source. See <i>AC Electrical Characteristics</i> for transfer function.                                                                       |
| 24                   | RFBAND          | RF Input Band Select Input. Drive high to enable 1680MHz to 2175MHz band. Leave unconnected to enable 1180MHz to 1680MHz band. Connect to GND to enable 925MHz to 1180MHz band.                                   |
| 25                   | QOUT-           | Baseband Quadrature Output. Connect to inverting input of high-speed ADC.                                                                                                                                         |
| 26                   | QOUT+           | Baseband Quadrature Output. Connect to noninverting input of high-speed ADC.                                                                                                                                      |
| 28                   | IOUT-           | Baseband In-Phase Output. Connect to inverting input of high-speed ADC.                                                                                                                                           |
| 29                   | IOUT+           | Baseband In-Phase Output. Connect to noninverting input of high-speed ADC.                                                                                                                                        |
| 30                   | MOD+            | PECL Modulus Control. A PECL high on MOD+ sets the dual-modulus prescaler to divide by 32. A PECL logic low sets the divide ratio to 33. Drive with a differential PECL signal in conjunction with MOD- (pin 31). |

# DBS Direct Downconverter

MAX2114

## Pin Description (continued)

| PIN | NAME          | FUNCTION                                                                                                                                                                                                                         |
|-----|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | MOD-          | PECL Modulus Control. A PECL low on MOD- sets the dual-modulus prescaler to divide by 32. A PECL logic high sets the divide ratio to 33. Drive with a differential PECL signal in conjunction with MOD+ (pin 30).                |
| 32  | PLLIN+        | PECL Phase-Locked Loop Input. Drive with a differential PECL signal in conjunction with PLLIN- (pin 33).                                                                                                                         |
| 33  | PLLIN-        | PECL Phase-Locked Loop Input. Drive with a differential PECL signal in conjunction with PLLIN+ (pin 32).                                                                                                                         |
| 34  | LOBUF+/PSOUT+ | LOBUFSEL = GND: PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used in conjunction with PSOUT-. Requires PECL-compatible termination. LOBUFSEL = V <sub>CC</sub> : 50Ω LO buffer noninverting output. |
| 35  | LOBUF-/PSOUT- | LOBUFSEL = GND: PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used in conjunction with PSOUT+. Requires PECL-compatible termination. LOBUFSEL = V <sub>CC</sub> : 50Ω LO buffer inverting output.    |
| 37  | LODIVSEL      | LO Buffer Divider Ratio Input. Drive high to enable divide-by-one LO buffer output. Connect to GND to enable divide-by-two buffer output.                                                                                        |
| 38  | TANK-         | LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.                                                                                                                                                   |
| 39  | VRLO          | LO Internal Regulator. Bypass with a 1000pF ceramic chip capacitor to GND.                                                                                                                                                       |
| 40  | TANK+         | LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.                                                                                                                                                   |
| 43  | FB            | Feedback Input for Loop Filter                                                                                                                                                                                                   |
| 44  | CP            | Voltage Drive Output. Control of external charge-pump transistor.                                                                                                                                                                |

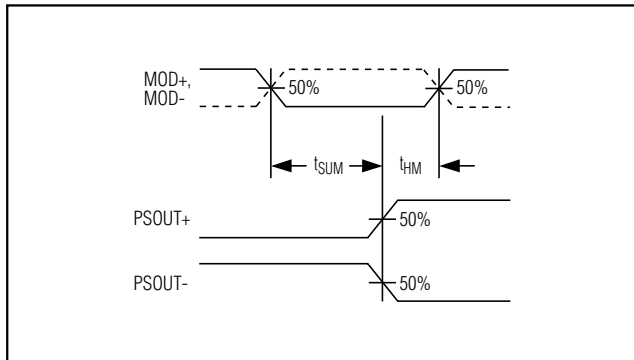
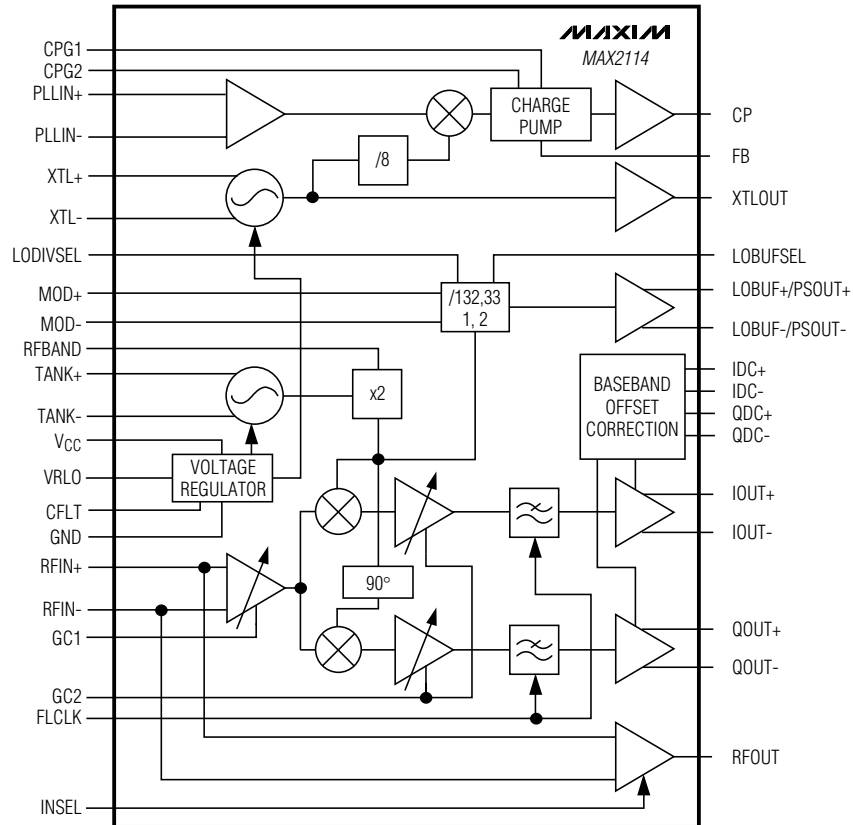


Figure 1. Modulus Control Timing Diagram

# DBS Direct Downconverter

## Functional Diagram



## Package Information

For the latest package outline information, go to  
[www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

8 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600