National Semiconductor

January 2002

LMH6639
190MHz Rail-to-Rail Output Amplifier with Disable

General Description

The LMH6639 is a voltage feedback operational amplifier with a rail-to-rail output drive capability of 110mA. Employing National's patented VIP10 process, the LMH6639 delivers a bandwidth of 190MHz at a current consumption of only 3.6mA. An input common mode voltage range extending to 0.2V below the V^- and to within 1V of V^+, makes the LMH6639 a true single supply op-amp. The output voltage range extends to within 30mV of either supply rail providing the user with a dynamic range that is especially desirable in low voltage applications.

The LMH6639 offers a slew rate of 172V/µs resulting in a full power bandwidth of approximately 28MHz. The T_{ON} value of 83nsec combined with a settling time of 33nsec makes this device ideally suited for multiplexing applications. Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic for any gain setting including +1, and excellent specifications for driving video cables including harmonic distortion of 65.8dBc, differential gain of 0.065% and differential phase of 0.05˚

Features

(V_S = 5V, Typical values unless specified)

■ Supply current (no load)	3.6mA
■ Supply current (off mode)	400µA
■ Output resistance (closed loop 1MHz)	0.186Ω
■ −3dB BW (A_V = 1)	190MHz
■ Settling time	33nsec
■ Input common mode voltage	−0.2V to 4V
■ Output voltage swing	40mV from rails
■ Linear output current	110mA
■ Total harmonic distortion	65.8dBc
■ Fully characterized for 3V, 5V and ±5V	
■ No output phase reversal with CMVR exceeded	
■ Excellent overdrive recovery	
■ Off Isolation 1MHz	−70dB
■ Differential Gain	0.065%
■ Differential Phase	0.05%

Applications

- Active filters
- CD/DVD ROM
- ADC buffer amplifier
- Portable video
- Current sense buffer

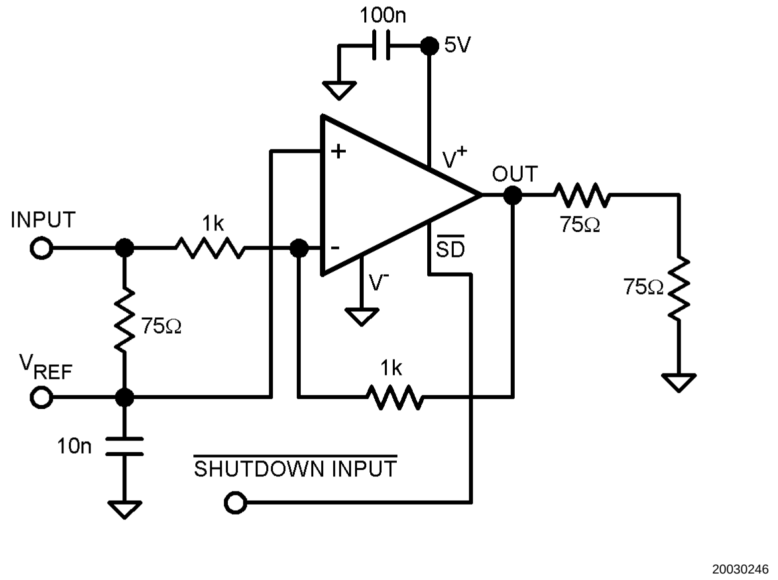


FIGURE 1. Typical Single Supply Schematic

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2) 200V (Note 9)
V_{IN} Differential	±2.5V
Input Current	±10mA
Supply Voltage ($V^+ - V^-$)	12.6V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering (10 sec)	260˚C

Operating Ratings (Note 1)

Operating Temperature Range (Note 4)	−40˚C to +85˚C
Package Thermal Resistance (θ_{JA}) (Note 4)	
SOT23-6	265˚C/W
SOIC-8	190˚C/W

3V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 3V, V^- = 0V, $V_O = V_{CM} = V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
BW	−3dB BW	A_V = +1		120	170		MHz
		A_V = −1			63		
$BW_{0.1dB}$	0.1dB Gain Flatness	R_F = 2.65kΩ , R_L = 1kΩ,			16.4		MHz
FPBW	Full Power Bandwidth	A_V = +1, V_{OUT} = $2V_{PP}$, −1dB V^+ = 1.8V, V^- = 1.2V			21		MHz
GBW	Gain Bandwidth product	A_V = +1			83		MHz
e_n	Input-Referred Voltage Noise	R_F = 33kΩ	f = 10kHz		16.1		nV/ $\sqrt{Hz}$
			f = 1MHz		6.71		
i_n	Input-Referred Current Noise	R_F = 1mΩ	f = 10kHz		1.30		pA/ $\sqrt{Hz}$
			f = 1MHz		0.36		
THD	Total Harmonic Distortion	f = 5MHz, V_O = $2V_{PP}$, A_V = −1, R_L = 100Ω to $V^+/2$			50		dBc
T_S	Settling Time	V_O = $2V_{PP}$, ±0.1%			37		ns
SR	Slew Rate	A_V = −1 (Note 8)		120	167		V/µs
V_{OS}	Input Offset Voltage				1.01	5 **7**	mV
TC V_{OS}	Input Offset Average Drift	(Note 11)			8		µV/˚C
I_B	Input Bias Current	(Note 7)			−1.02	−2.6 **−3.5**	µA
I_{OS}	Input Offset Current				20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance	A_V = +1, f = 1kHz, R_S = 1MΩ			6.1		MΩ
C_{IN}	Common Mode Input Capacitance	A_V = +1, R_S = 100kΩ			1.35		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB			−0.3	−0.2 **−0.1**	V
				1.8 **1.6**	2		
CMRR	Common Mode Rejection Ratio	(Note 12)		72	93		dB
A_{VOL}	Large Signal Voltage Gain	V_O = $2V_{PP}$, R_L = 2kΩ to $V^+/2$		80 **76**	100		dB
		V_O = $2V_{PP}$, R_L = 150Ω to $V^+/2$		74 **70**	78		

3V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ C$, $V^+ = 3V$, $V^- = 0V$, $V_O = V_{CM} = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_O	Output Swing High	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = 200mV$	2.90	2.98		V
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = 200mV$	2.75	2.93		
		$R_L = 50\Omega$ to $V^+/2$, $V_{ID} = 200mV$	2.6	2.85		
	Output Swing Low	$R_L = 2k\Omega$ to $V^+/2$, $V_{ID} = -200mV$		25	75	mV
		$R_L = 150\Omega$ to $V^+/2$, $V_{ID} = -200mV$		75	200	
		$R_L = 50\Omega$ to $V^+/2$, $V_{ID} = -200mV$		130	300	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$, (Note 10)	50 **35**	120		mA
		Sinking to $V^+/2$, (Note 10)	67 **40**	140		
I_{OUT}	Output Current	$V_O = 0.5V$ from either supply		99		mA
PSRR	Power Supply Rejection Ratio	(Note 12)	72	96		dB
I_S	Supply Current (Enabled)	No Load		3.5	5.6 **7.5**	mA
	Supply Current (Disabled)			0.3	0.5 **0.7**	
TH_SD	Threshold Voltage for Shutdown Mode			$V^+-1.59$		V
I_SD PIN	Shutdown Pin Input Current	SD Pin Connect to 0V (Note 7)		−13		μA
T_{ON}	On Time After Shutdown			83		nsec
T_{OFF}	Off Time to Shutdown			160		nsec
R_{OUT}	Output Resistance Closed Loop	$R_F = 10k\Omega$, f = 1kHz, $A_V = -1$		27		mΩ
		$R_F = 10k\Omega$, f = 1MHz, $A_V = -1$		266		

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ C$, $V^+ = 5V$, $V^- = 0V$, $V_O = V_{CM} = V^+/2$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
BW	−3dB BW	$A_V = +1$	130	190		MHz
		$A_V = -1$		64		
$BW_{0.1dB}$	0.1dB Gain Flatness	$R_F = 2.51k\Omega$, $R_L = 1k\Omega$,		16.4		MHz
FPBW	Full Power Bandwidth	$A_V = +1$, $V_{OUT} = 2V_{PP}$, −1dB		28		MHz
GBW	Gain Bandwidth Product	$A_V = +1$		86		MHz
e_n	Input-Referred Voltage Noise	$R_F = 33k\Omega$ f = 10kHz		16.17		$nV/\sqrt{Hz}$
		f = 1MHz		6.63		
i_n	Input-Referred Current Noise	$R_F = 1M\Omega$ f = 10KHz		1.35		$pA/\sqrt{Hz}$
		f = 1MHz		0.35		
THD	Total Harmonic Distortion	f = 5MHz, $V_O = 2V_{PP}$, $A_V = -1$ $R_L = 100\Omega$ to $V^+/2$		65.8		dBc
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.065		%
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$ to $V^+/2$		0.05		deg
T_S	Settling Time	$V_O = 2V_{PP}$, ±0.1%		33		ns
SR	Slew Rate	$A_V = -1$, (Note 8)	130	172		V/μs
V_{OS}	Input Offset Voltage			1.02	5 **7**	mV

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$, and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
TC V_{OS}	Input Offset Average Drift	(Note 11)		8		µV/°C
I_B	Input Bias Current	(Note 7)		−1.2	−2.6 **−3.25**	µA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance	A_V = +1, f = 1kHz, R_S = 1MΩ		6.88		MΩ
C_{IN}	Common Mode Input Capacitance	A_V = +1, R_S = 100kΩ		1.32		pF
CMVR	Common-Mode Input Voltage Range	CMRR ≥ 50dB		−0.3	−0.2 **−0.1**	V
				4	3.8 **3.6**	
CMRR	Common Mode Rejection Ratio	(Note 12)	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 4V_{PP} R_L = 2kΩ to $V^+/2$	86 **82**	100		dB
		V_O = 3.75V_{PP} R_L = 150Ω to $V^+/2$	74 **70**	77		
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	4.90	4.97		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	4.65	4.90		
		R_L = 50Ω to $V^+/2$, V_{ID} = 200mV	4.40	4.77		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	100	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		85	200	
		R_L = 50Ω to $V^+/2$, V_{ID} = −200mV		190	400	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$, (Note 10)	100 **79**	160		mA
		Sinking from $V^+/2$, (Note 10)	120 **85**	190		
I_{OUT}	Output Current	V_O = 0.5V from either supply		110		mA
PSRR	Power Supply Rejection Ratio	(Note 12)	72	96		dB
I_S	Supply Current (Enabled)	No Load		3.6	5.8 **8.0**	mA
	Supply Current (Disabled)			0.40	0.8 **1.0**	
TH_SD	Threshold Voltage for Shutdown Mode			V^+ −1.65		V
I_SD PIN	Shutdown Pin Input Current	SD Pin Connected to 0V (Note 7)		−30		µA
T_{ON}	On Time after Shutdown			83		nsec
T_{OFF}	Off Time to Shutdown			160		nsec
R_{OUT}	Output Resistance Closed Loop	R_F = 10kΩ, f = 1kHz, A_V = −1		29		mΩ
		R_F = 10kΩ, f = 1MHz, A_V = −1		253		

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_J = 25^\circ C$, $V_{SUPPLY} = \pm 5V$, $V^- = 0V$, $V_O = V_{CM} = GND$, and $R_L = 2k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
BW	−3dB BW	$A_V = +1$		150	228		MHz
		$A_V = -1$			65		
$BW_{0.1dB}$	0.1dB Gain Flatness	$R_F = 2.26k\Omega$, $R_L = 1k\Omega$			18		MHz
FPBW	Full Power Bandwidth	$A_V = +1$, $V_{OUT} = 2V_{PP}$, −1dB			29		MHz
GBW	Gain Bandwidth Product	$A_V = +1$			90		MHz
e_n	Input-Referred Voltage Noise	$R_F = 33k\Omega$	f = 10kHz		15.74		$nV/\sqrt{Hz}$
			f = 1MHz		6.94		
i_n	Input-Referred Current Noise	$R_F = 1M\Omega$	f = 10kHz		1.13		$pA/\sqrt{Hz}$
			f = 1MHz		0.34		
THD	Total Harmonic Distortion	f = 5MHz, $V_O = 2V_{PP}$, $A_V = -1$, $R_L = 100\Omega$			71.2		dBc
DG	Differential Gain	NTSC, $A_V = +2$ $R_L = 150\Omega$			0.065		%
DP	Differential Phase	NTSC, $A_V = +2$ $R_L = 150\Omega$			0.045		deg
T_S	Settling Time	$V_O = 2V_{PP}$, ±0.1%			33		ns
SR	Slew Rate	$A_V = -1$ (Note 8)		140	200		V/µs
V_{OS}	Input Offset Voltage				1.03	5 **7**	mV
TC V_{OS}	Input Offset Voltage Drift	(Note 11)			8		µV/°C
I_B	Input Bias Current	(Note 7)			−1.40	−2.6 **−3.25**	µA
I_{OS}	Input Offset Current				20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance	A_V +1, f = 1kHz, $R_S = 1M\Omega$			7.5		MΩ
C_{IN}	Common Mode Input Capacitance	$A_V = +1$, $R_S = 100k\Omega$			1.28		pF
CMVR	Common Mode Input Voltage Range	CMRR ≥ 50dB			−5.3	−5.2 **−5.1**	V
				3.8 **3.6**	4.0		
CMRR	Common Mode Rejection Ratio	(Note 12)		72	95		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 9V_{PP}$, $R_L = 2k\Omega$		88 **84**	100		dB
		$V_O = 8V_{PP}$, $R_L = 150\Omega$		74 **70**	77		
V_O	Output Swing High	$R_L = 2k\Omega$, $V_{ID} = 200mV$		4.85	4.96		V
		$R_L = 150\Omega$, $V_{ID} = 200mV$		4.55	4.80		
		$R_L = 50\Omega$, $V_{ID} = 200mV$		3.60	4.55		
	Output Swing Low	$R_L = 2k\Omega$, $V_{ID} = -200mV$			−4.97	−4.90	V
		$R_L = 150\Omega$, $V_{ID} = -200mV$			−4.85	−4.55	
		$R_L = 50\Omega$, $V_{ID} = -200mV$			−4.65	−4.30	
I_{SC}	Output Short Circuit Current	Sourcing to Ground, (Note 10)		100 **80**	168		mA
		Sinking to Ground, (Note 10)		110 **85**	190		

±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V_{SUPPLY} = ±5V, V^- = 0V, V_O = V_{CM} = GND, and R_L = 2kΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{OUT}	Output Current	V_O = 0.5V from either supply		112		mA
PSRR	Power Supply Rejection Ratio	(Note 12)	72	96		dB
I_S	Supply Current (Enabled)	No Load		4.18	6.5 **8.5**	mA
	Supply Current (Disabled)			0.758	1.0 **1.3**	
TH_SD	Threshold Voltage for Shutdown Mode			V^+ − 1.67		V
I_SD PIN	Shutdown Pin Input Current	SD Pin Connected to −5V (Note 7)		−84		µA
T_{ON}	On Time after Shutdown			83		nsec
T_{OFF}	Off Time to Shutdown			160		nsec
R_{OUT}	Output Resistance Closed Loop	R_F = 10kΩ, f = 1kHz, A_V = −1		32		mΩ
		R_F = 10kΩ, f = 1MHz, A_V = −1		226		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the average of the rising and falling slew rates.

Note 9: Machine Model, 0Ω in series with 200pF.

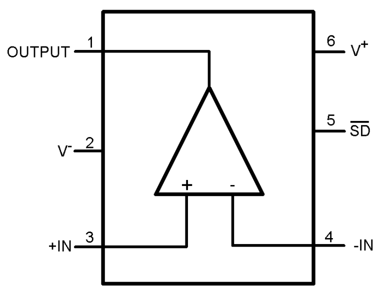
Note 10: Short circuit test is a momentary test.

Note 11: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Note 12: f ≤ 1kHz (see typical performance Characteristics)

Connection Diagrams

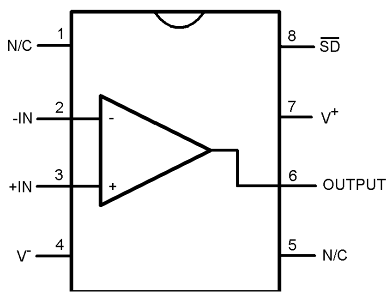
SOT23-6



20030201

Top View

SOIC-8



20030202

Top View

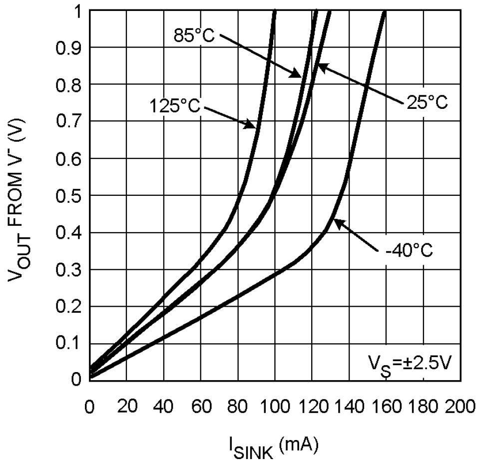
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Pin SOT-23	LMH6639MF	A81A	1k Units Tape and Reel	MF06A
	LMH6639MFX		3k Units Tape and Reel	
8-Pin SOIC	LMH6639MA	LMH6639MA	Rails	M08A
	LMH6639MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics

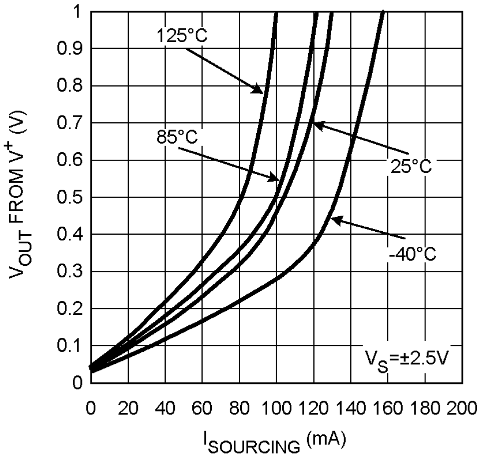
At T_J = 25˚C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified.

Output Sinking Saturation Voltage vs. I_{OUT} for Various Temperature



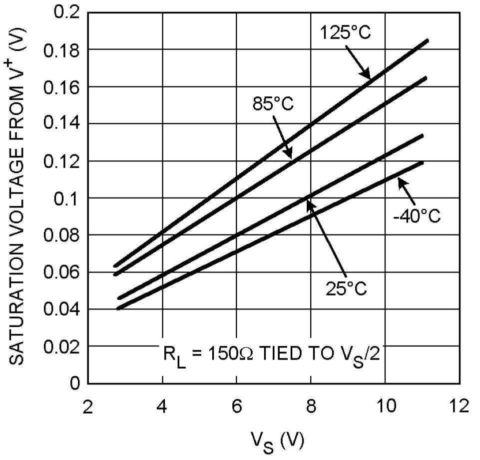
20030239

Output Sourcing Saturation Voltage vs. I_{OUT} for Various Temperature



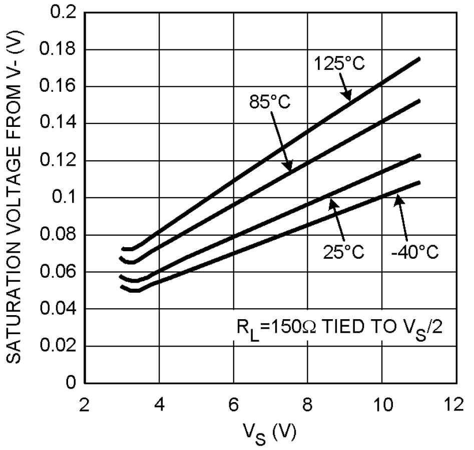
20030237

Positive Output Saturation Voltage vs. V_{SUPPLY} for Various Temperature



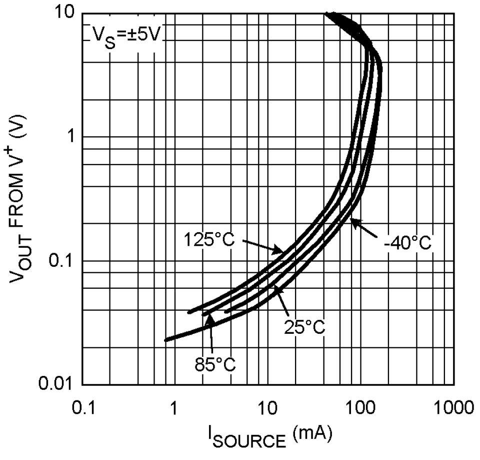
20030233

Negative Output Saturation Voltage vs. V_{SUPPLY} for Various Temperature



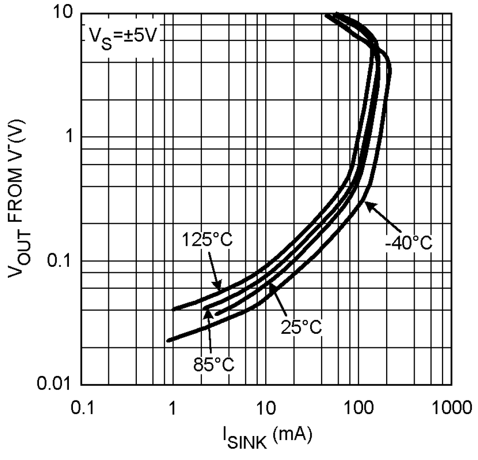
20030234

V_{OUT} from V^+ vs. I_{SOURCE}



20030238

V_{OUT} from V^- vs. I_{SINK}

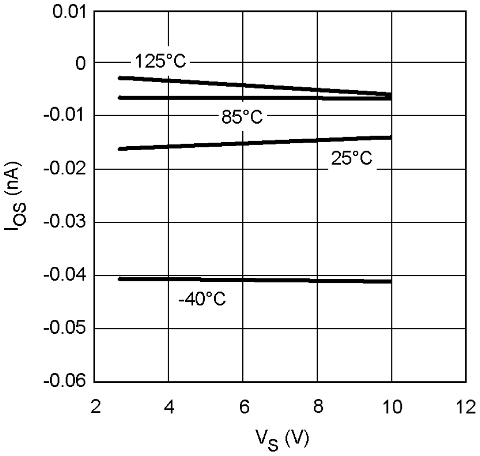


20030236

Typical Performance Characteristics

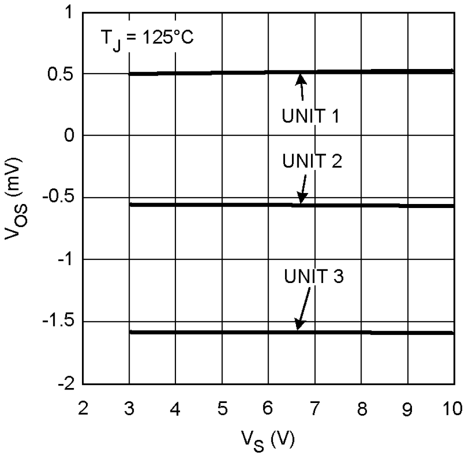
At T_J = 25˚C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified. (Continued)

I_{OS} vs. V_S for Various Temperature



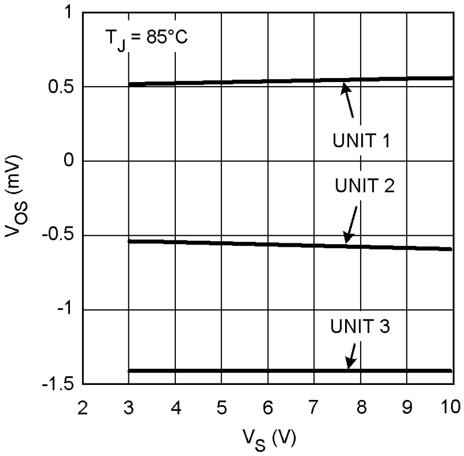
20030232

V_{OS} vs. V_S for 3 Representative Units



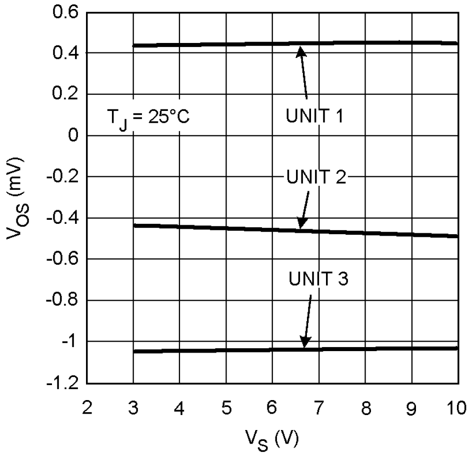
20030245

V_{OS} vs. V_S for 3 Representative Units



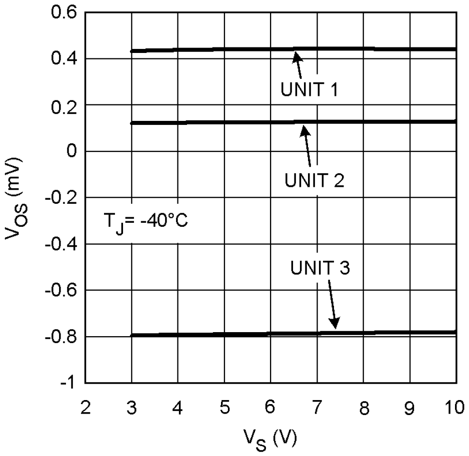
20030244

V_{OS} vs. V_S for 3 Representative Units



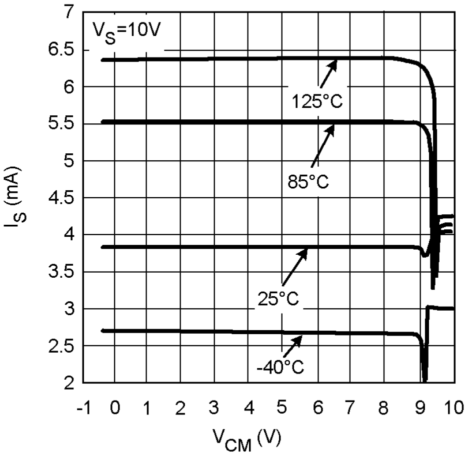
20030243

V_{OS} vs. V_S for 3 Representative Units



20030242

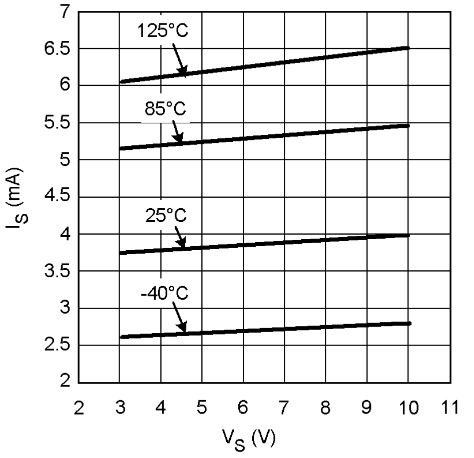
I_{SUPPLY} vs. V_{CM} for Various Temperature



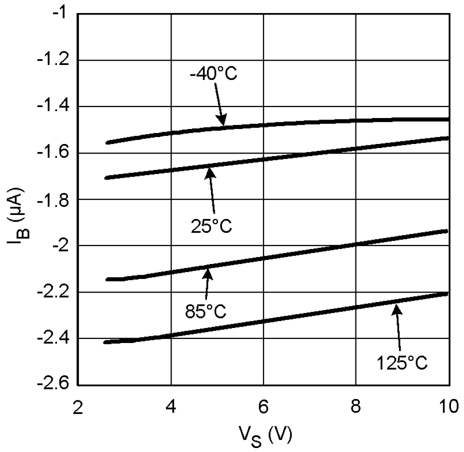
20030240

Typical Performance Characteristics

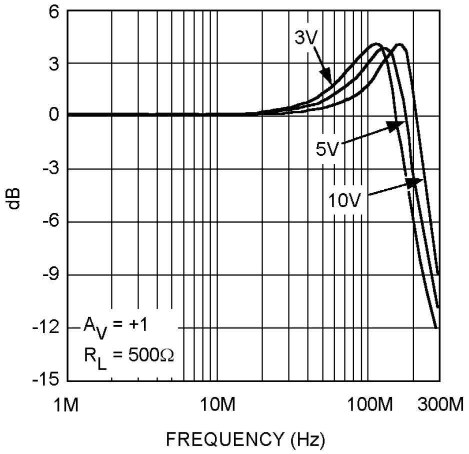
At T_J = 25˚C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified. (Continued)


I_{SUPPLY} vs. V_S for Various Temperature

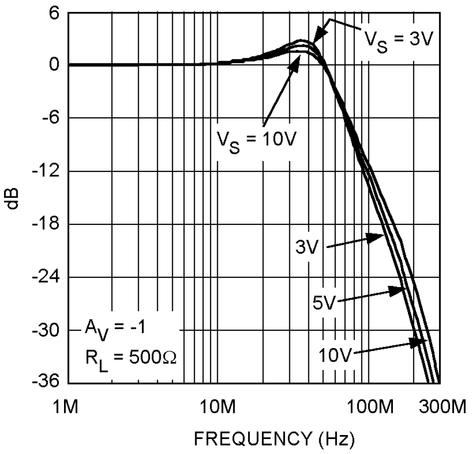
20030241


I_B vs. V_S for Various Temperature

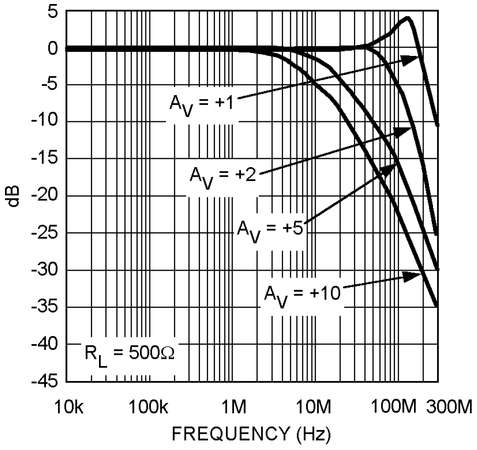
20030235


Bandwidth for Various V_S

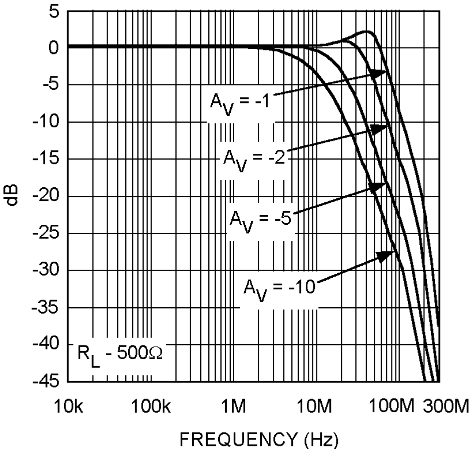
20030206


Bandwidth for Various V_S

20030205


Gain vs. Frequency Normalized

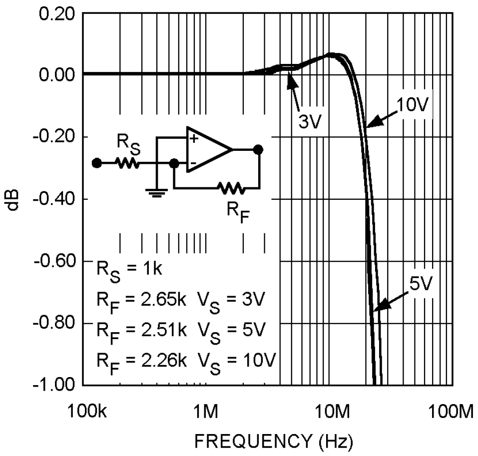
20030207


Gain vs. Frequency Normalized

20030208

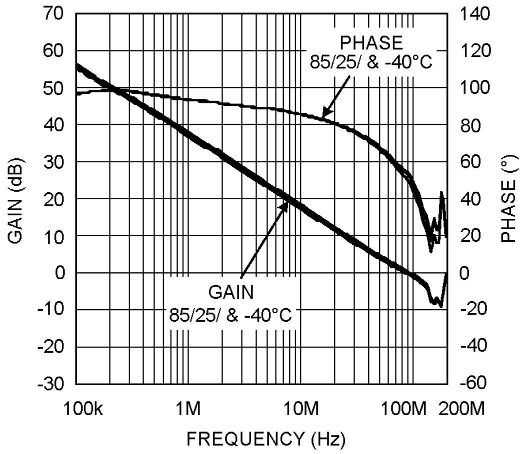
Typical Performance Characteristics At T_J = 25˚C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified. (Continued)

0.1dB Gain Flatness



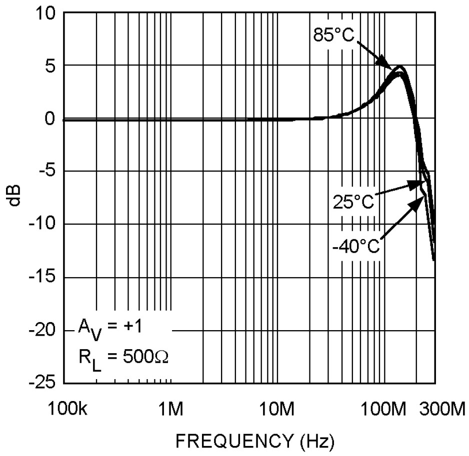
20030209

Gain and phase vs. Frequency for Various Temperature



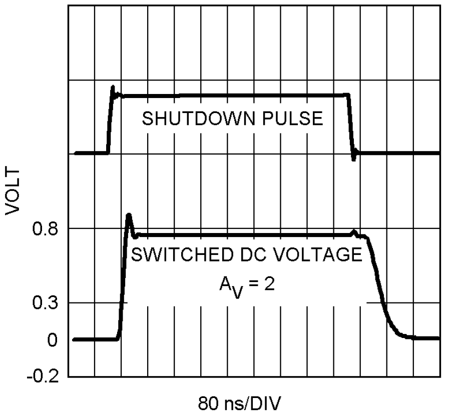
20030204

Frequency Response vs. Temperature



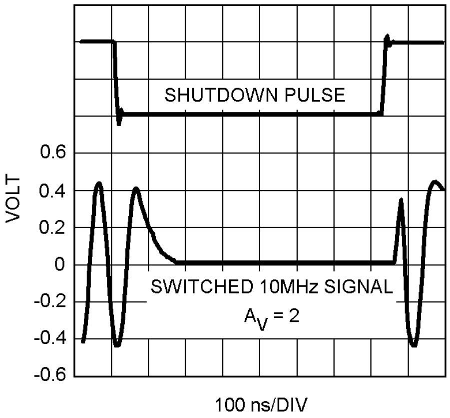
20030210

On-Off Switching DC Voltage



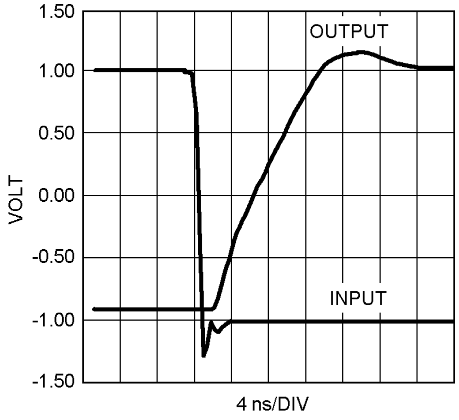
20030211

On-Off Switching 10MHz



20030212

Slew Rate (Positive)

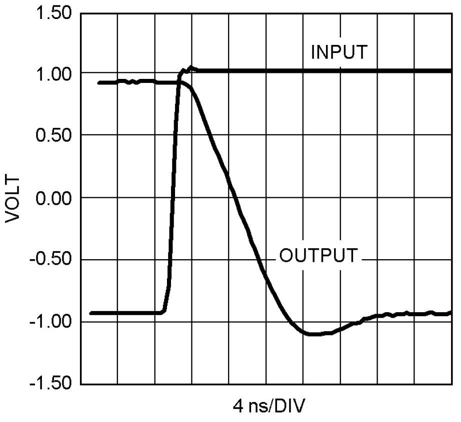


20030214

Typical Performance Characteristics

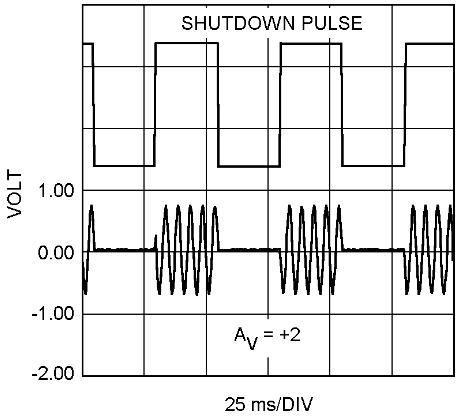
At T_J = 25˚C, V^+ = +2.5, V^- = −2.5V, R_F = 330Ω for A_V = +2, R_F = 1kΩ for A_V = −1. Unless otherwise specified. (Continued)

Slew Rate (Negative)



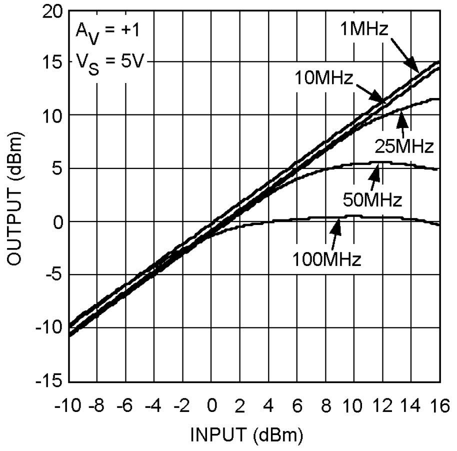
20030213

On-Off Switching of Sinewave



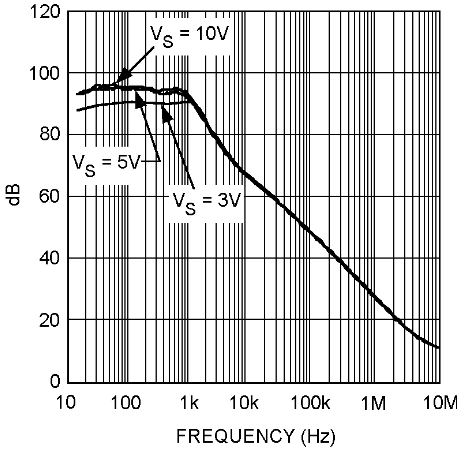
20030215

Power Sweep



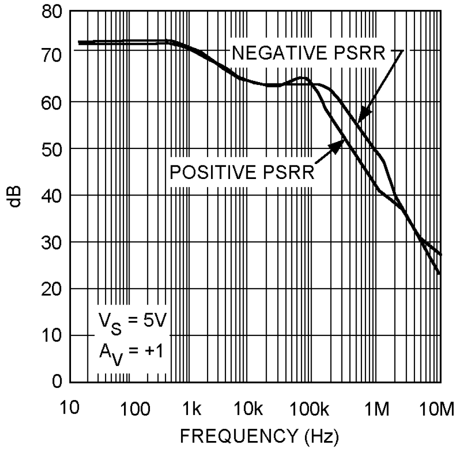
20030216

CMRR vs. Frequency



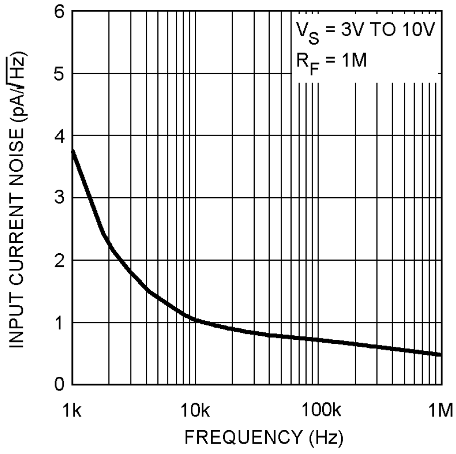
20030218

PSRR vs. Frequency



20030217

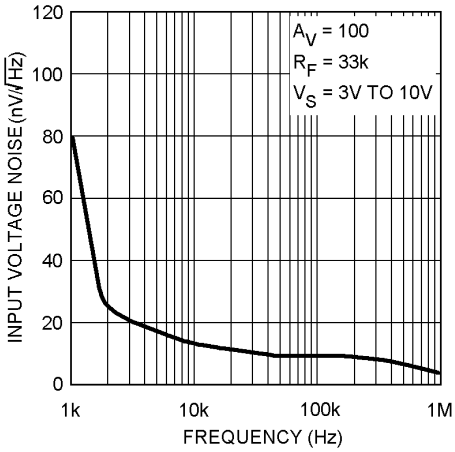
Current Noise



20030220

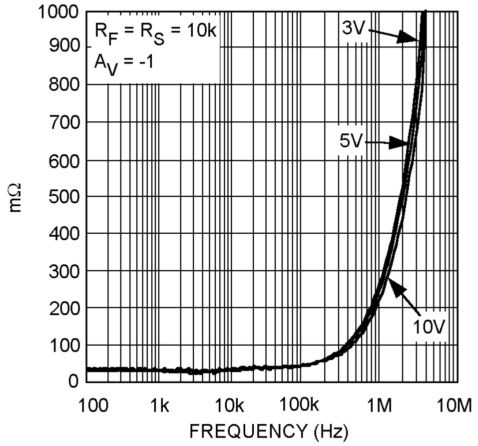
Typical Performance Characteristics At $T_J = 25^\circ C$, $V^+ = +2.5$, $V^- = -2.5V$, $R_F = 330\Omega$ for $A_V = +2$, $R_F = 1k\Omega$ for $A_V = -1$. Unless otherwise specified. (Continued)

Voltage Noise



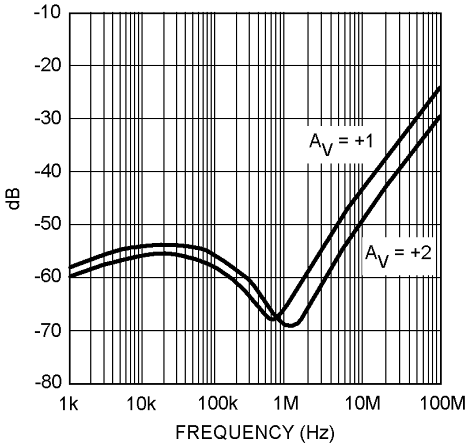
20030219

Closed Loop Output Resistance vs. Frequency



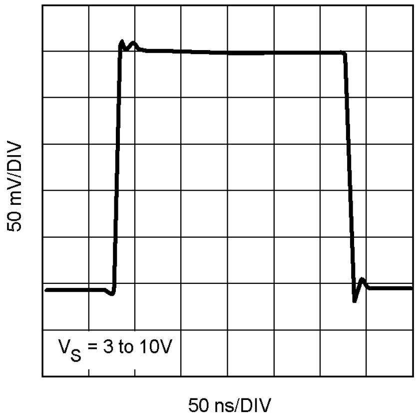
20030221

Off Isolation



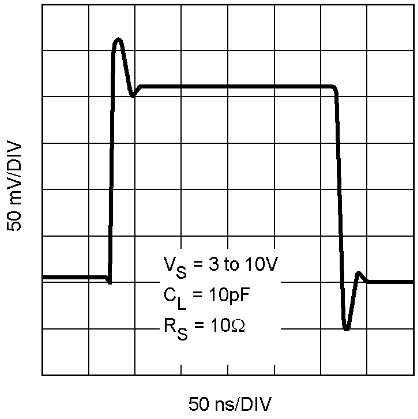
20030222

Small Signal Pulse Response ($A_V = +1$)



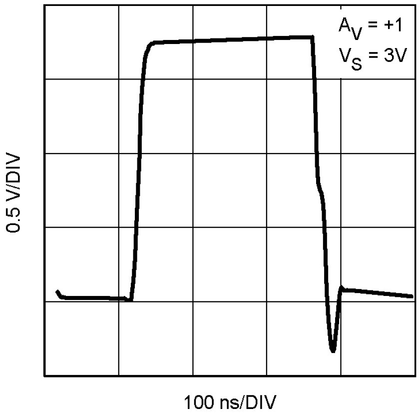
20030250

Small Signal Pulse Response ($A_V = -1$)



20030249

Large Signal Pulse Response

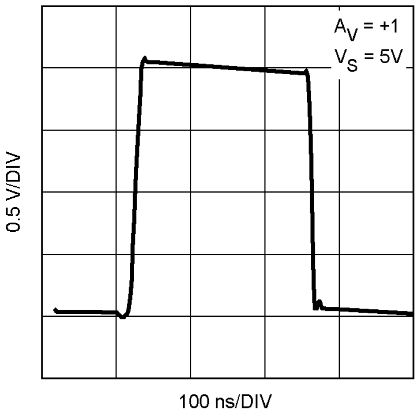


20030226

Typical Performance Characteristics

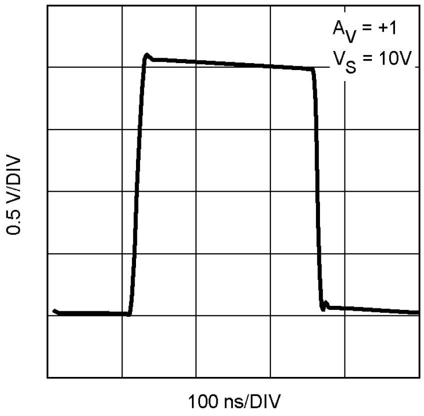
At $T_J = 25^\circ C$, $V^+ = +2.5$, $V^- = -2.5V$, $R_F = 330\Omega$ for $A_V = +2$, $R_F = 1k\Omega$ for $A_V = -1$. Unless otherwise specified. (Continued)

Large Signal Pulse Response



20030227

Large Signal Pulse Response

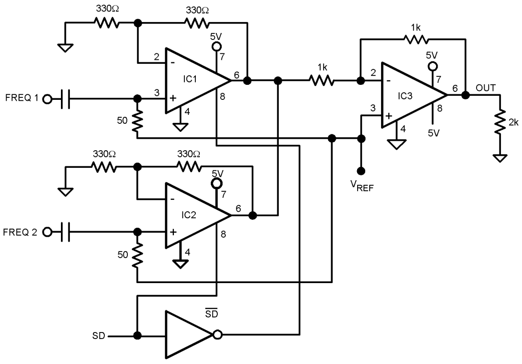


20030228

Application Notes

Multiplexing 5 and 10MHz

The LMH6639 may be used to implement a circuit which multiplexes two signals of different frequencies. Three LMH6639 high speed op-amps are used in the circuit of *Figure 2* to accomplish the multiplexing function. Two LMH6639 are used to provide gain for the input signals, and the third device is used to provide output gain for the selected signal.

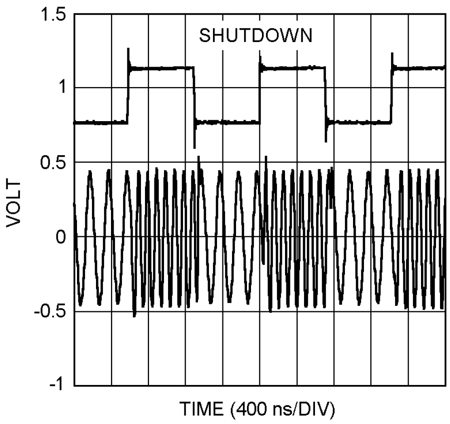


20030247

Note: Pin numbers pertain to SOIC-8 package

FIGURE 2. Multiplexer

Multiplexing signals “FREQ 1” and “FREQ 2” exhibit closed loop non-inverting gain of +2 each based upon identical 330Ω resistors in the gain setting positions of IC1 and IC2. The two multiplexing signals are combined at the input of IC3, which is the third LMH6639. This amplifier may be used as a unity gain buffer or may be used to set a particular gain for the circuit.



20030248

FIGURE 3. Switching between 5 and 10MHz

1k resistors are used to set an inverting gain of −1 for IC3 in the circuit of *Figure 2*. *Figure 3* illustrates the waveforms produced. The upper trace shows the switching waveform used to switch between the 5MHz and 10MHz multiplex signals. The lower trace shows the output waveform consisting of 5MHz and 10MHz signals corresponding to the high or low state of the switching signal.

In the circuit of *Figure 2*, the outputs of IC1 and IC2 are tied together such that their input impedances are placed in parallel at the input of IC3. The output impedance of the disabled amplifier is high compared both to the output impedance of the active amplifier and the 330Ω gain setting resistors. The closed loop output resistance for the LMH6639 is around 0.2Ω. Thus the active state amplifier output impedance dominates the input node to IC3, while the disabled amplifier is assured of a high level of suppression of unwanted signals which might be present at the output.

Shutdown Operation

With $\overline{SD}$ pin left floating, the device enters normal operation. However, since the $\overline{SD}$ pin has high input impedance, it is best tied to V^+ for normal operation. This will avoid inadvertent shutdown due to capacitive pick-up from nearby nodes. LMH6639 will typically go into shutdown when $\overline{SD}$ pin is more than 1.7V below V^+, regardless of operating supplies.

PCB Layout Consideration and Components selection

Care should be taken while placing components on a PCB. All standard rules should be followed especially the ones for high frequency and/ or high gain designs. Input and output pins should be separated to reduce cross-talk, especially under high gain conditions. A groundplane will be helpful to avoid oscillations. In addition, a ground plane can be used to create micro-strip transmission lines for matching purposes. Power supply, as well as shutdown pin de-coupling will reduce cross-talk and chances of oscillations.

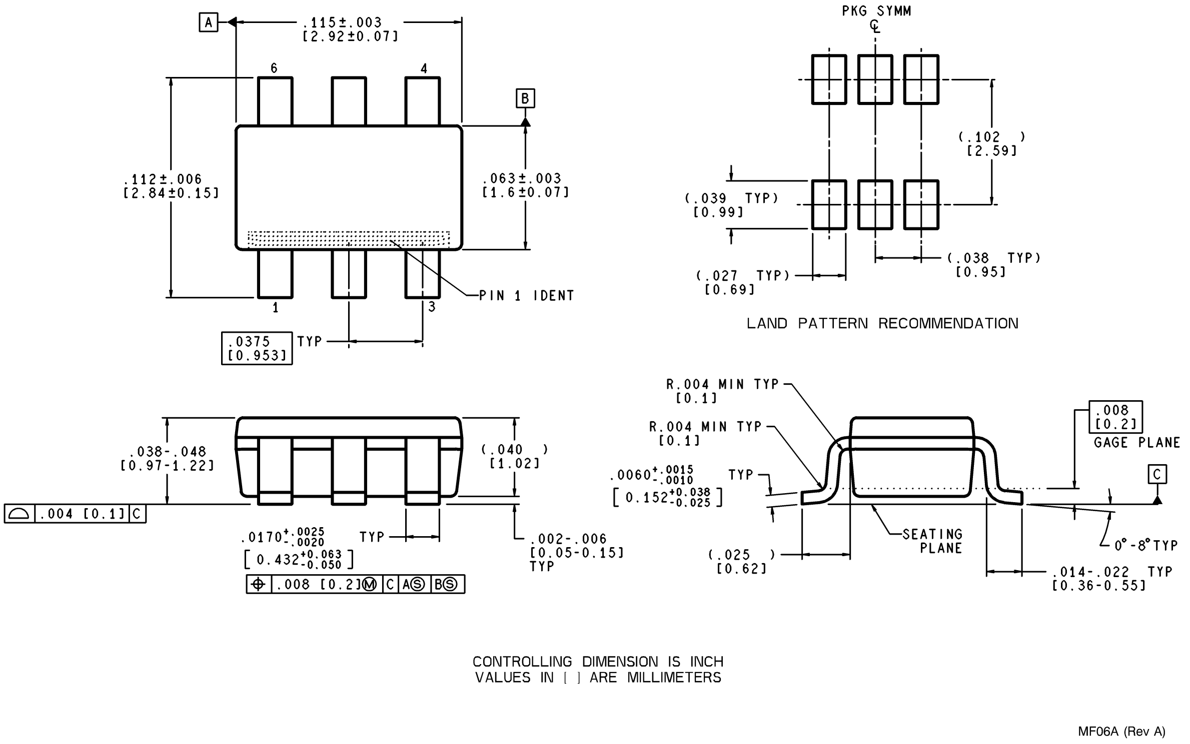
Another important parameter in working with high speed amplifiers is the component values selection. Choosing high value resistances reduces the cut-off frequency because of the influence of parasitic capacitances. On the other hand choosing the resistor values too low could ’load down’ the nodes and will contribute to higher overall power dissipation. Keeping resistor values at several hundreds of ohms up to several kΩ will offer good performance.

National Semiconductor suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

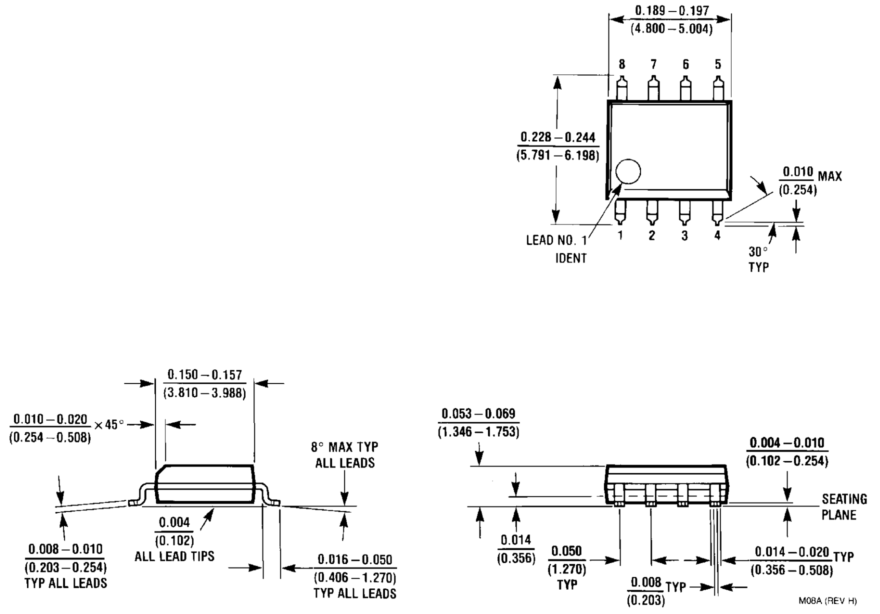
Device	Package	Evaluation Board PN
LMH6639MA	8-Pin SOIC	CLC730027
LMH6639MF	SOT23-6	CLC730116

These free evaluation boards are shipped when a device sample request is placed with National Semiconductor. For normal operation, tie the SD pin to V^+.

Physical Dimensions inches (millimeters) unless otherwise noted



6-Pin SOT23
NS Package Number MF06A



8-Pin SOIC
NS Package Number M08A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507