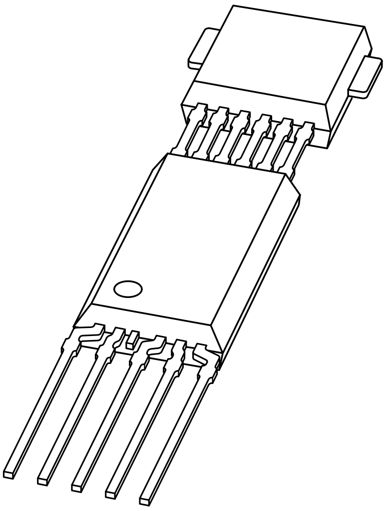
DATA SHEET



KMA200
Programmable angle sensor

Objective specification
Supersedes data of 2001 Jun 20

2002 Mar 25

Philips Semiconductors

PHILIPS

Programmable angle sensor KMA200

FEATURES

- Magnetic field angular sensing
- Resolution 0.1°
- Accuracy better than 0.6°
- Maximum angular range 0° to 180°
- Programmable angle range
- Temperature range from –40 to +125 °C
- User programmable EEPROM
- Ratiometric analog output
- 13-bit digital output
- Bi-directional digital Serial Peripheral Interface (SPI)
- Adjustable zero point offset
- On-line diagnosis for all main functional blocks
- Switch-off function at persistent overvoltage
- Temperature supervision
- Pre-calibrated delivery.

DESCRIPTION

The KMA200 is a programmable angle sensor, employing the magnetoresistive effect of thin-film permalloy for sensing the angle between an external magnetic field in the sensor plane and the sensor. The sensor consists of two galvanic separated wheatstone bridges and an integrated circuit.

The KMA200 is user programmable. This allows user specific adjustment of the angular range and zero point, and the storage of a 32-bit identifier. The data is held permanently in an EEPROM.

The device can be programmed to work either in analog or digital (SPI) output. One of four different analog output characteristics may be selected. The implemented on-line diagnosis monitors the input and output signals as well as the data processing. Deviations and failures of the angle value are indicated in the output signal. An overall temperature supervision is implemented.

PINNING

PIN	SYMBOL	DESCRIPTION
1	V_{DD}	supply voltage
2	DATA/V_{OUT1}	data I/O, analog output
3	CLK/V_{OUT2}	data clock, analog output
4	GND	ground
5	$\overline{CS}$	chip select, data transfer I/O

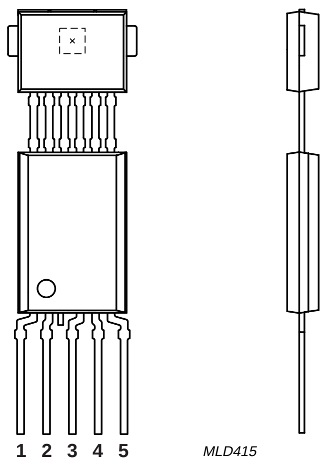


Fig.1 Simplified outline (SOT637).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating voltage	4.5	5	5.5	V
I_{DD}	supply current	–	10	–	mA
RES	resolution	–	0.1	–	deg
A_{80}	accuracy in temperature range –40 to +80 °C; note 1	–	–	0.6	deg
A_{125}	accuracy in temperature range –40 to +125 °C; note 1	–	–	1.3	deg
T_{amb}	ambient temperature	–40	–	+125	°C
f_{oper}	operating frequency of the SPI; note 2	–	–	1	MHz

Notes

1. In (homogenous) magnetic field at saturation field strength.
2. With optimized application circuit.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	operating voltage; note 1	–16.5	+26.5	V
V_{pin}	voltage at all external pins; note 1	–16.5	+26.5	V
T_{stg}	storage temperature	–40	+150	°C
T_{amb}	ambient operating temperature	–40	+125	°C
NVR	EEPROM, non volatile retention	17	–	years
NVE	EEPROM, non volatile endurance	10^4	–	cycles

Note

1. Up to a maximum of 32 V for t < 400 ms.

CHARACTERISTICS

T_{amb} = 25 °C; $H_{rotation}$ = 30 kA/m; central sensor positioning in homogenous field; V_{DD} = 5 V; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
General					
V_{DD}	operating voltage	4.5	5	5.5	V
I_{DD}	supply current	–	10	–	mA
RES	resolution	–	0.1	–	deg
I_O	constant output current	–	–	2	mA
$I_{I(Z)}$	input current when output driver is in high-impedance state	–	–	10	μA
C_L	capacitance load at outputs	0.1	–	100	nF
R_L	output pull-up or pull-down load; note 1	5	–	6	kΩ
$V_{sw(on)}$	on threshold; device switch on if $V_{DD} > V_{sw(on)}$	3.1	3.75	4.4	V
$V_{sw(off)}$	off threshold; device switch on if $V_{DD} > V_{sw(off)}$	2.9	–	4.2	V
$V_{sw(hys)}$	hysteresis	–	0.2	–	V
f_{CLK}	internal clock frequency	3.3	4.096	4.9	MHz
Δf_{CLK}	frequency shift over temperature and ageing	–10	–	+10	$\%f_{CLK}$
T_{sens}	temperature range of internal sensor	–50	–	+180	°C
RES_{temp}	resolution of internal sensor	–	0.8	–	°C/cnt
ΔT_{sens}	accuracy of internal sensor	–5	–	+5	°C
t_{on}	Power-on time; until first valid result	–	–	10	ms
f_{upd}	measurement update rate at nominal oscillator frequency	–	4	–	kHz
t_{delay}	dead time of step response	–	–	0.5	ms
t_s	settling time after ideal input angle step; time until analog standard output reaches 90% of final value at nominal oscillator frequency; C_L = 5 nF	–	1	–	ms
$t_{(g)}$	group delay at nominal oscillator frequency; C_L = 5 nF	–	0.65	–	ms
Rep	reproducibility of output signals	–	–	0.15	deg
Analog output V_{out1}; standard output					
A_{80}	accuracy in temperature range –40 to 80 °C; note 2	–	–	0.6	deg
A_{125}	accuracy in temperature range –40 to 125 °C; note 2	–	–	1.3	deg
$V_{out1(nom)}$	nominal output voltage range	5	–	95	$\%V_{DD}$
CL_{lo}	programmable clamping level low	5	–	30.5	$\%V_{DD}$
CL_{hi}	programmable clamping level high	69.5	–	95	$\%V_{DD}$
LDR	lower diagnostic range	0	–	4	$\%V_{DD}$
UDR	upper diagnostic range	96	–	100	$\%V_{DD}$
RES	resolution; 4608 counts in nominal output voltage range	–	0.02	–	$\%V_{DD}$
DNL	differential non linearity; guaranteed monotonic	–	–	1	LSB
INL	integral non linearity; normal operation mode	–0.15	±0.12	+0.15	$\%V_{DD}$
$V_{n(o)}$	output referred noise; peak-to-peak; 2.5 ms or 10 measurements in sequence; note 3	–	–	0.02	$\%V_{DD}$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Analog output V_{out2}; mode 1					
A_{80}	accuracy in temperature range –40 to 80 °C; note 2	–	–	0.6	deg
A_{125}	accuracy in temperature range –40 to 125 °C; note 2	–	–	1.3	deg
$V_{out2(nom)}$	nominal output voltage range	95	–	5	$\%V_{DD}$
CL_{lo}	programmable clamping level low	5	–	30.5	$\%V_{DD}$
CL_{hi}	programmable clamping level high	69.5	–	95	$\%V_{DD}$
LDR	lower diagnostic range	0	–	4	$\%V_{DD}$
UDR	upper diagnostic range	96	–	100	$\%V_{DD}$
RES	resolution; 4608 counts in nominal output voltage range	–	0.02	–	$\%V_{DD}$
DNL	differential non linearity; guaranteed monotonic	–	–	1	LSB
INL	integral non linearity; normal operation mode	–0.15	±0.12	+0.15	$\%V_{DD}$
$V_{n(o)}$	output referred noise; peak-to-peak; 2.5 ms or 10 measurements in sequence; note 3	–	–	0.02	$\%V_{DD}$
Analog output V_{out2}; mode 2					
A_{80}	accuracy in temperature range –40 to 80 °C; note 2	–	–	0.6	deg
A_{125}	accuracy in temperature range –40 to 125 °C; note 2	–	–	1.3	deg
$V_{out2(nom)}$	nominal output voltage range	2.5	–	47.5	$\%V_{DD}$
CL_{lo}	programmable clamping level low	2.5	–	15.25	$\%V_{DD}$
CL_{hi}	programmable clamping level high	34.75	–	47.5	$\%V_{DD}$
LDR	lower diagnostic range	0	–	2	$\%V_{DD}$
UDR	upper diagnostic range	50	–	100	$\%V_{DD}$
RES	resolution; 2304 counts in nominal output voltage range	–	0.02	–	$\%V_{DD}$
DNL	differential non linearity; guaranteed monotonic	–	–	1	LSB
INL	integral non linearity; normal operation mode	–0.15	±0.12	+0.15	$\%V_{DD}$
$V_{n(o)}$	output referred noise; peak-to-peak; 2.5 ms or 10 measurements in sequence; note 3	–	–	0.02	$\%V_{DD}$
Analog output V_{out2}; mode 3					
$V_{out2(low)}$	output low voltage range; I_{sink} < 2 mA	0	–	10	$\%V_{DD}$
$V_{out2(high)}$	output high voltage range; I_{source} < 2 mA	90	–	100	$\%V_{DD}$
A_{th}	accuracy of threshold; normal operation mode	–0.1	–	+0.1	deg

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Digital output (SPI); modes 5 and 6					
f_{oper}	operating frequency of the SPI; note 4	–	–	1	MHz
RES_D	resolution; 13-bit	–	0.022	–	deg/cnt
DNL_D	differential non linearity; guaranteed monotonic	–	–	1	LSB
INL_D	integral non linearity; normal operation mode	–5	–	+5	LSB
N_D	noise level; peak-to-peak; 2.5 ms or 10 measurements in sequence	–	–	2	LSB
V_{OL}	output low voltage; I_{sink} < 2 mA	0	–	0.3	V
V_{OH}	output high voltage; I_{source} < 2 mA	V_{DD} – 0.3	–	V_{DD}	V
I_{OM}	peak output current; current limitation	10	–	20	mA
t_r	rise time				
	bit SL = 0; from 5 %V_{DD} to 95 %V_{DD}; C_L = 100 pF	100	–	200	ns
	bit SL = 1; from 5 %V_{DD} to 95 %V_{DD}; C_L = 100 pF	500	–	1000	ns
t_f	fall time				
	bit SL = 0; from 95 %V_{DD} to 5 %V_{DD}; C_L = 100 pF	100	–	200	ns
	bit SL = 1; from 95 %V_{DD} to 5 %V_{DD}; C_L = 100 pF	500	–	1000	ns
C_i	input capacitance at any pin	–	–	10	pF

Notes

1. Up to a maximum voltage of 32 V for t < 400 ms.
2. In (homogenous) magnetic field at saturation field strength.
3. Analog outputs low-pass filtered (corner frequency approximately 1.3 kHz).
4. With optimized application circuit.

FUNCTIONAL DESCRIPTION

The KMA200 consists of a MR sensor element and a signal conditioning IC as shown in Fig.2.

The sensor element produces two sinusoidal signals with a phase shift of 90° depending on the angular orientation of a stimulating magnetic field to the input of the IC.

The IC converts the sinusoidal input signals into a linear representation of the angular value by means of two 13 bit ADC's and a ROM-code controlled data processing unit.

Sensor voltage offset compensation, zero point, clamping levels and angular range adjustment, customization of DATA output rise and fall times, on-line diagnosis and the selection of different output characteristics are also incorporated.

Offset and configuration parameters are stored in a user programmable EEPROM that is accessed via a Serial Peripheral Interface (SPI).

Data output may be selected as either an analog or a digital signal.

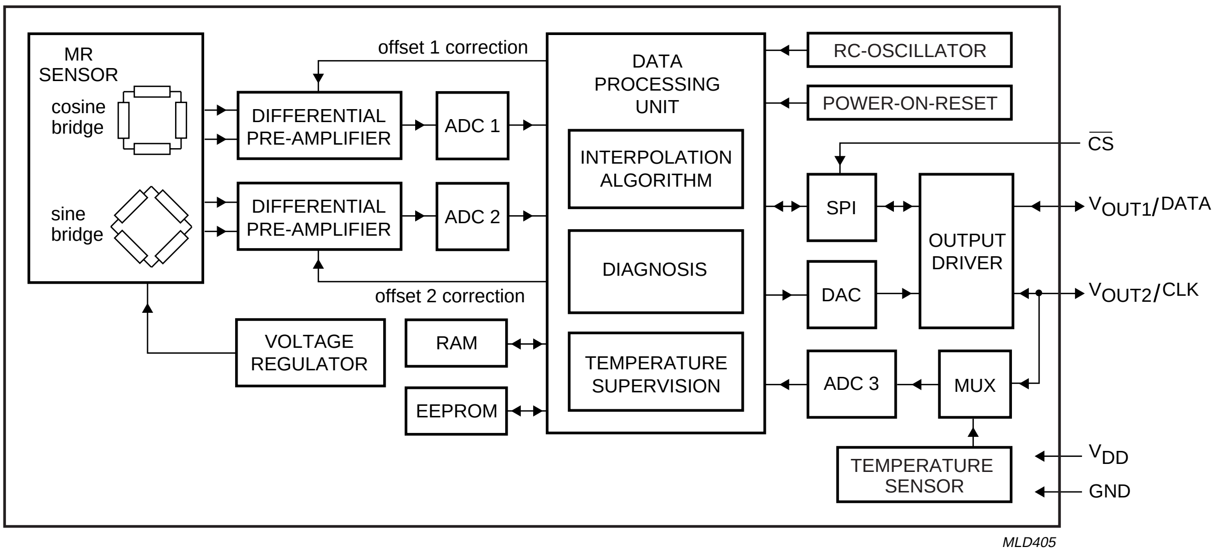


Fig.2 Functional block diagram.

Analog output

The KMA200 provides two output pins. These are set to work either in digital or analog output mode, depending on the user defined control word stored in the EEPROM.

In analog output mode the measured angle value is converted into a linear voltage value that is ratiometric to the supply voltage V_{DD}.

This voltage is driven by the standard output stage to pin V_{OUT1}. Supporting redundancy requirements, the same value is supplied to a second output stage which is connected to pin V_{OUT2}. This second output stage is programmable to one of four different output characteristics; mode 1, mode 2, mode 3 or a high-impedance state (see Table 1).

The analog output voltage range codes linear angle value as well as diagnostic information.

A valid angle value is nominally mapped to an output voltage range of CL_{lo} (default 5% of V_{DD}) to CL_{hi} (default 95% of $V_{DD)}$ at the standard output V_{OUT1} (see Fig.3).

If set to mode 1, the inverted voltage range of CL_{hi} to CL_{lo} is available at the second output V_{OUT2} (see Fig.4). In mode 2 (see Fig.5) the valid output range at pin V_{OUT2} is nominally $CL_{lo}/2$ to $CL_{hi}/2$ (half range). When programmed to mode 3, the second output V_{OUT2} functions as a comparator depending on the angle value (see Fig.6).

Output voltages above or below these ranges are used for diagnostics.

Table 1 Setting the KMA200 output characteristics

OUTPUT CHARACTERISTICS		PIN ASSIGNMENT		MODE SETTING		
MODE	**TYPE**	**V_{OUT1}/DATA**	**V_{OUT2}/CLK**	**OM2**	**OM1**	**OM0**
Mode 1	analog	standard	inverted	1	0	0
Mode 2	analog	standard	half range	1	0	1
Mode 3	analog	standard	comparator	1	1	0
Mode 4	analog	standard	high impedance	1	1	1
Mode 5	digital	serial data (SPI)	serial clock (SPI)	0	0	0
Mode 6	digital	serial data (SPI) bit complement	serial clock (SPI)	0	0	1

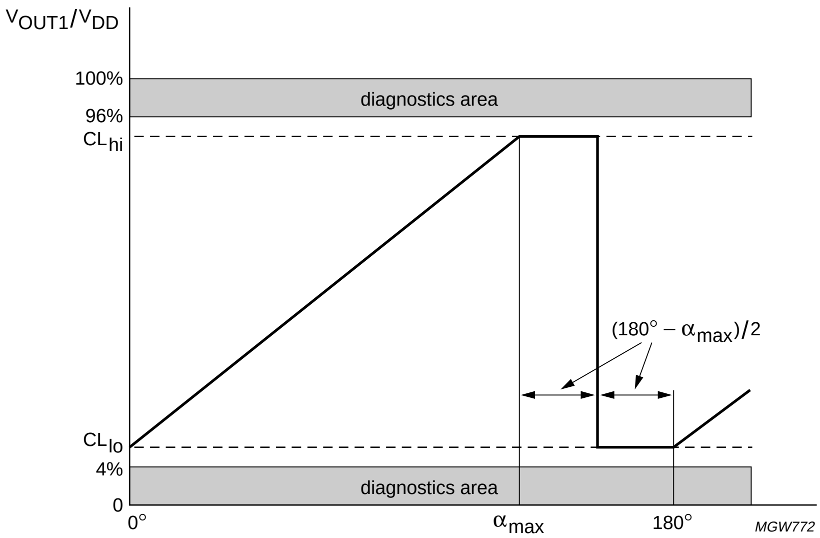


Fig.3 Standard analog output mode.

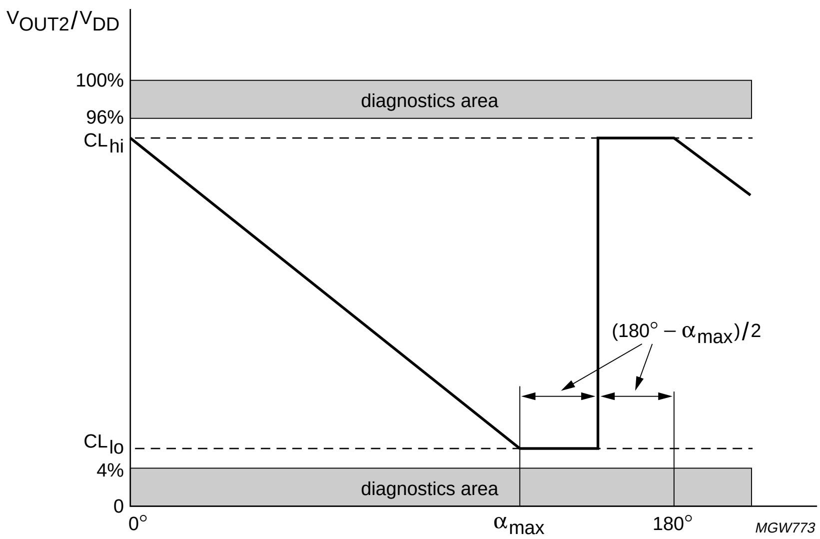


Fig.4 Inverted analog output mode (mode 1).

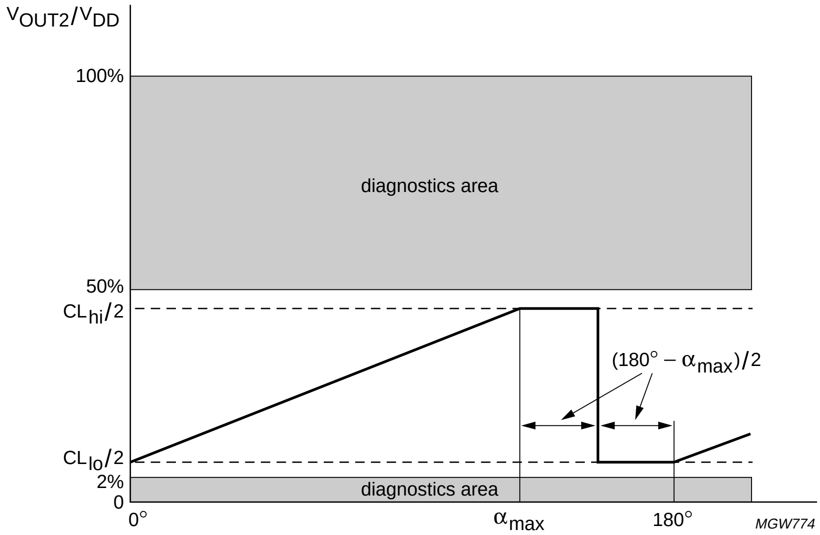


Fig.5 Half range analog output mode (mode 2).

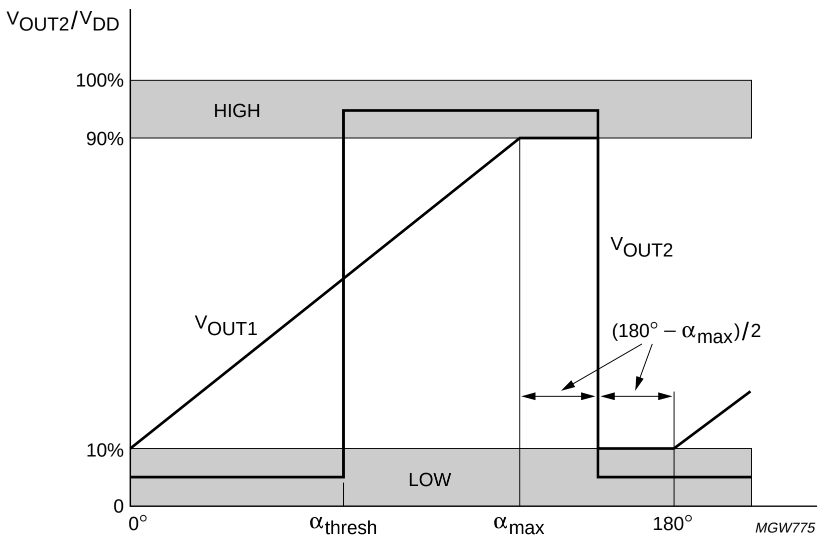


Fig.6 Comparator analog output mode (mode 3).

Digital output (SPI)

The serial programmable interface is compatible with the Motorola SPI specification. The sensor signal comprises 14 bits (D13 to D0) as shown in Fig.7. Bits D12 to D0 are used for coding the angle value while bit D13 is reserved for indicating error and diagnostic conditions as defined below. The 14 data bits are arranged in 2 bytes. Bit D13 is the MSB of the sensor signal and bit D0 is the LSB of the sensor signal. Byte 2, which is sent first, contains data bits D13 to D7 and parity bit P2 which is added to allow recognition of disturbed messages. Bit P2 gives the odd parity of data bits D13 to D7. Similarly, byte 1 comprises data bits D6 to D0 and parity bit P1, which gives the odd parity of data bits D6 to D0.

The odd parity is chosen to detect failure modes when pin DATA is short-circuited to GND or V_{DD} or when the connection between data-out of the slave and data-in of the master is interrupted (e.g. in the event of a broken wire).

The error and diagnostic conditions are indicated by a logic 1 in bit D13 (active HIGH). In an error situation bits D1 and D0 contain the error code (see Table 2). All other bits (D12 to D2) still show the current measurement value, but as the last two bits are lost for error representation the resolution is reduced to 11 bit. Whether the measurement value is reliable or not depends on the specific error and has to be evaluated by the master unit.

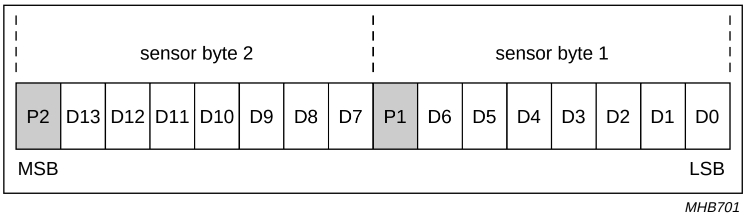


Fig.7 Digital output coding.

Table 2 Error codes

D1	D0	DESCRIPTION	ANGLE VALID
0	0	diagnosis error	no
0	1	diagnosis error (input stage)	no
1	0	over-temperature warning	yes
1	1	(not used)	–

Timings characteristics (serial interface)

The SPI is a byte-orientated synchronous serial master-slave bus system. The KMA200 requires a SPI that operates in slave mode only. In output mode, data bits are sampled by the master using the rising edge of the clock as shown in Figure 8.

The falling edge indicates that the next data bit has to be provided by the slave device (shift operation). Data in the input mode is also sampled on the rising edge of the clock. The timing requirements of the SPI interface are given in Table 3.

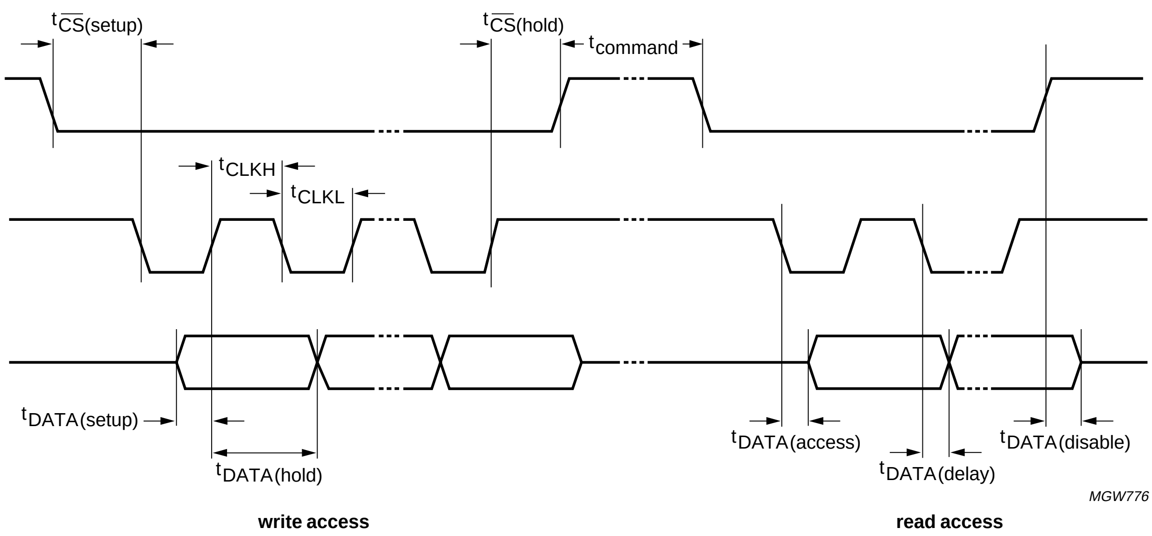


Fig.8 Bit timing of the serial interface (SPI).

Table 3 Timing of the serial interface

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{oper}	operating frequency		–	1	MHz
t_{CLKH}	clock HIGH time		100	–	ns
t_{CLKL}	clock LOW time		100	–	ns
$t_{\overline{CS}(setup)}$	$\overline{CS}$ fall to CLK fall set-up time		400	–	ns
$t_{\overline{CS}(hold)}$	CLK rise to $\overline{CS}$ HIGH hold time		50	–	ns
$t_{DATA(setup)}$	DATA valid to CLK rise set-up time		50	–	ns
$t_{DATA(hold)}$	DATA valid after CLK rise hold time		50	–	ns
$t_{DATA(access)}$	DATA access time	CLK fall to DATA out			
	bit SL = 0		–	250	ns
	bit SL = 1		–	1050	ns
$t_{DATA(disable)}$	DATA disable time	$\overline{CS}$ rise to DATA high-Z	–	50	ns
$t_{DATA(delay)}$	DATA delay time	DATA valid after CLK fall			
	bit SL = 0		–	250	ns
	bit SL = 1		–	1050	ns
t_{POR}	Power-on reset time		–	3	ms
t_{INIT_CMD1}	initialization of command mode - clock LOW time		1	–	ms
t_{INIT_CMD2}	initialization of command mode - initialization time		1	–	ms
$t_{FB(norm)}$	fall back time to normal operation mode (EEPROM FB = 1)		–	100	ms
t_{ICS}	inter command space		20	–	µs

Programming

The normal operation mode is configured with sixteen 16-bit registers (constants) stored in the on-chip EEPROM. Two 16-bit EEPROM constants are available for sensor identification.

On Power-on, these constants are written into the RAM and evaluated by the calibration microcontroller. See Table 4 for a listing of the constants and their descriptions.

Table 4 Output mode configuration

ADDRESS (HEX)	NAME	DESCRIPTION
0	sensor_offset_1	offset of sensor bridge 1; used for offset compensation
1	sensor_offset_2	offset of sensor bridge 2; used for offset compensation
2	zero_angle	mechanical 0° position relative to the zero point of the sensor output; used for zero-angle calibration
3	angular_range	definition of the angular input range that is mapped to the whole analog output signal range
4	comp_threshold	threshold for programmable output/mode 3
5	temp_vref; temp_offs	reference voltage level and offset of temperature measurement; used for temperature calibration
6	temp_err; temp_warn	temperature warning and error level; used for temperature supervision
7	ctrl1	control information word 1; used for selection of various operating modes
8	ctrl2	control Information word 2; configures the diagnostic functions
9	clamp_lo; clamp_hi	clamping levels of analog outputs
A	id1	sensor identifier 1; this data is not evaluated by the ASIC and can be used for sensor identification
B	id2	sensor identifier 2; this data is not evaluated by the ASIC and can be used for sensor identification
C	anom; tc_anom	nominal amplitude and temperature coefficient; used for input stage diagnosis
D	tc_offset_1	temperature coefficient of sensor offset 1
E	tc_offset_2	temperature coefficient of sensor offset 2
F	crc16	CRC16 checksum of all EEPROM constants

Table 5 sensor_offset_1 and sensor_offset_2 register

MSB							BIT								LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

$$\text{Offset voltage} = 2^{-15} \times \text{sensor\_offset\_n} \times \frac{V_{DDS}}{44} \approx \text{sensor\_offset\_n} \times 0.694\ \mu\text{V/V}$$

Table 6 zero_angle, angular_range and comp_threshold register

MSB							BIT								LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

$$\alpha = A[15:0] \times \frac{180^\circ}{2^{16}} \approx A[15:0] \times 0.00275^\circ$$

Table 7 temp_vref and temp_offs register

MSB								**BIT**							**LSB**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
temp_vref								temp_offs							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table 8 temp_err and temp_warn register

MSB								**BIT**							**LSB**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
temp_err								temp_warn							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$$\text{Temperature} = -50^\circ C + T[7:0] \times 1^\circ C$$

Table 9 ctrl1 register

MSB								**BIT**							**LSB**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RS1	RS0	EP	EC	SL	DO1	DO0	DI1	DI0	OM2	OM1	OM0	CF1	CF0	G1	G0

Table 10 Description of ctrl1 bits

BIT	SYMBOL	DESCRIPTION
15,14	RS[1:0]	resolution of AD conversions in command mode; default value: 01
13	EP	EEPROM write protection; default value: 0
12	EC	external clock; default value: 0
11	SL	rise and fall time of DATA output; default value: 0 0 = nominal 150 ns 1 = nominal 750 ns
10,9	DO[1:0]	diagnoses of output stage; default value: 00 00 = level 0; $V_{OUT,meas} - V_{OUT,nom}$; < 10 %$V_{DD}$ 01 = level 1; $V_{OUT,meas} - V_{OUT,nom}$; < 5 %$V_{DD}$ 10 = level 2; $V_{OUT,meas} - V_{OUT,nom}$; < 2 %$V_{DD}$ 11 = level 3; $V_{OUT,meas} - V_{OUT,nom}$; < 1 %$V_{DD}$
8,7	DI[1:0]	diagnoses of input stage; default value: 000; note 1 000 = level 0; $A_{meas} - A_{nom}$; < 7.8 mV/V 001 = level 1; $A_{meas} - A_{nom}$; < 6.24 mV/V 010 = level 2; $A_{meas} - A_{nom}$; < 4.68 mV/V 011 = level 3; $A_{meas} - A_{nom}$; < 3.12 mV/V 100 = level 4; $A_{meas} - A_{nom}$; < 1.56 mV/V

BIT	SYMBOL	DESCRIPTION
6,5,4	OM[2:0]	output mode; default value: 000 000 = digital output 001 = complement digital output 100 = analog output; standard + programmable output mode 1 101 = analog output; standard + programmable output mode 2 110 = analog output; standard + programmable output mode 3 111 = analog output; standard output only
3,2	CF[1:0]	chopper frequency of instrumentation amplifiers; default value: 01
1,0	G[1:0]	gain of instrumentation amplifiers; default value: 10

Note

1. The ctrl1 register contains DI0 and DI1, DI2 is located in the ctrl2 register as bit 11 (see Tables 11 and 12).

Table 11 ctrl2 register

MSB							BIT								LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	DI2	OC	FB	ETS	TC1	TC0	EDO	CO1	CO0	EDI	CI1	CI0

Table 12 Description of ctrl2 bits

BIT	SYMBOL	DESCRIPTION
15 to 12	–	not used
11	DI2	third bit of DI[2:0], diagnoses of input stage; see Table 10; default value: 0
10	OC	offset compensation of analog outputs; default value: 1
9	FB	automatic fall back into command mode; default value: 0
8	ETS	enable temperature supervision; default value: 1 0 = disabled 1 = enabled
7,6	TC[1:0]	error counter temperature supervision; default value: 00 00 = 0 01 = 2 10 = 4 11 = 8
5	EDO	enable diagnosis output stage; default value: 1 0 = disabled 1 = enabled
4,3	CO[1:0]	error counter diagnosis output stage; default value: 00 00 = 0 01 = 2 10 = 4 11 = 8

BIT	SYMBOL	DESCRIPTION
2	EDI	enable diagnosis input stage; default value: 1 0 = disabled 1 = enabled
1,0	CI[1:0]	error counter diagnosis input stage; default value: 00 00 = 0 01 = 2 10 = 4 11 = 8

Table 13 clamp_lo and clamp_hi register

MSB							BIT								LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
clamp_lo								clamp_hi							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$$\text{Lower clamping level} = 5\% + \text{clamp\_lo} \times 0.1\%$$

$$\text{Upper clamping level} = 69.5\% + \text{clamp\_hi} \times 0.1\%$$

Table 14 anom and tc_anom register

MSB							BIT								LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
anom								tc_anom							
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$$\text{Nominal amplitude,0} = \text{anom} \times \frac{1}{2^8 \times 22 \times K_{Trig}} \approx \text{anom} \times 0.1078 \text{ mV/V}$$

$$\text{Temperature coefficient nominal amplitude} = \text{tc\_anom} \times 2^{-14} K^{-1} \approx \text{tc\_anom} \times 0.0061\% \times K^{-1}$$

Table 15 tc_offset_1 and tc_offset_2 register

MSB							BIT								LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

$$\text{Temperature coefficient} = 2^{-23} \times \text{sensor\_offset\_n} \times \frac{V_{DDS}}{44} K^{-1} \approx \text{tc\_offset\_n} \times 2.709 \text{ (nV/V)/K}$$

Programming of the EEPROM is possible in command mode only. To activate the command mode, the following initialization procedure (see Fig.9) must be executed during Power-on reset. During Power-on, pin $\overline{CS}$ must be held on a HIGH level and pin CLK must be held on a LOW level. This condition has to start during reset and must be valid during the following initialization phase of the ASIC for at least 1 ms. $\overline{CS}$ and CLK are internally weak pull-up, therefore at least pin CLK must be actively driven. If these conditions are valid, the ASIC will start in command mode. For all other combinations, or if the levels are not constant for the minimum time of 1 ms, the ASIC will start in normal operation mode.

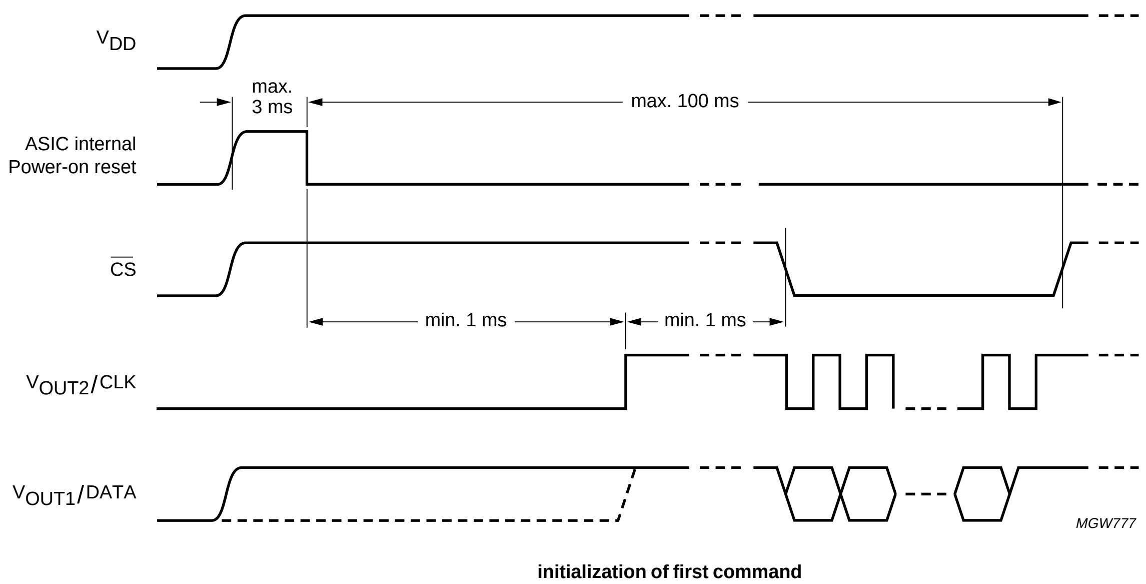


Fig.9 Procedure to enter the command mode.

WRITE RAM (0nH), READ RAM (1nH)

To write data to the RAM, the command byte 0nH (where n is the HEX address of the data), followed by the 16-bit data has to be sent. To read data from the RAM, the command byte 1nH has to be sent. If $\overline{CS}$ is activated again, the RAM contents at the specified address is clocked out. Note that on Power-on only the EEPROM constants at address 00H to 0FH are read from the EEPROM into the RAM. It is not possible to read from the EEPROM directly.

CALCULATE CRC16 AND PROGRAM EEPROM (30H)

To program the EEPROM, the configuration data has to be written to the RAM addresses 00H to 0EH. The EEPROM programming voltage then has to be applied at pin V_{DD} and the command byte 30H has to be sent. The ASIC calculates the CRC16 checksum and writes the RAM constants at address 00H to 0FH to the EEPROM. This command is only executed when bit EP in the control information word is logic 0 on Power-on. If bit EP is logic 1, this command is ignored. Writing a new value to the control information word in RAM does not cancel the write protection.

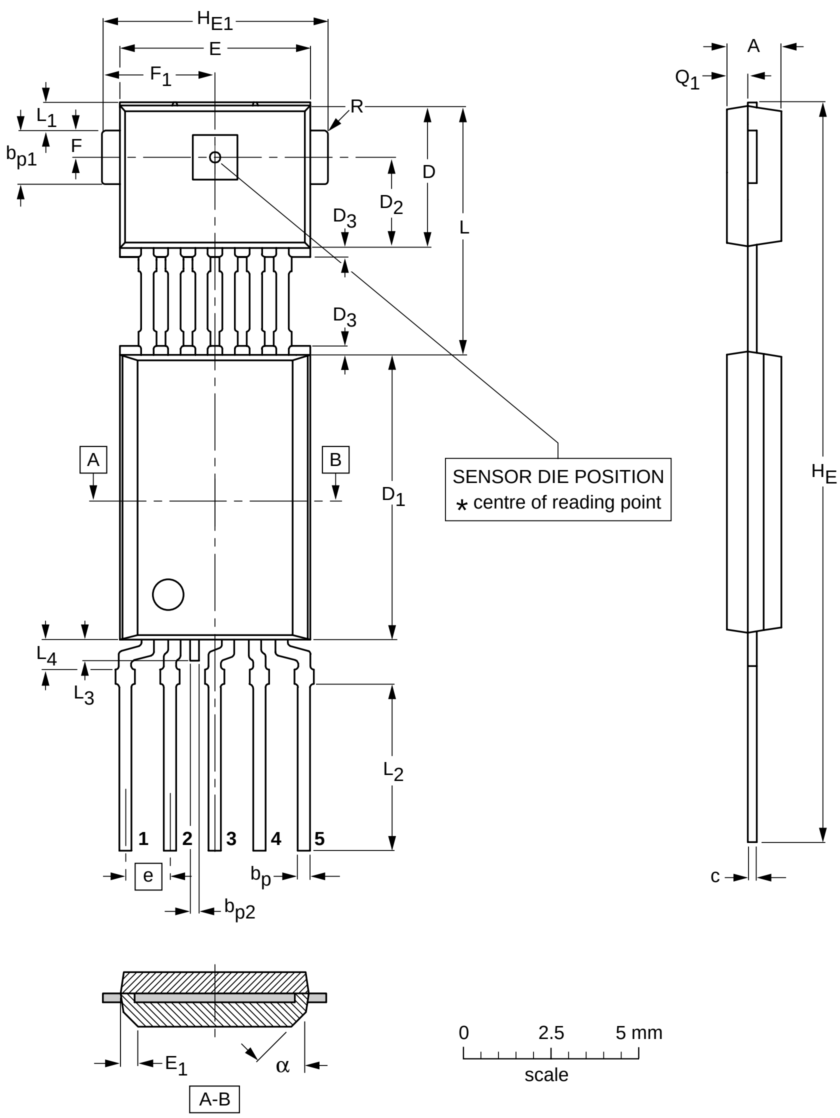
NOTES TO THE PROGRAMMING

The EEPROM addresses 0, 1, 5, C, D and E are device dependent and pre-calibrated for each device. Changing the contents of these addresses to another value is not allowed as specific behaviour could then no longer be guaranteed.

The EEPROM addresses A and B are used to store production related information. Changing these values should be avoided.

PACKAGE OUTLINE

Plastic single-ended multi-chip package; 6 interconnections; 5 in-line leads **SOT637**



Q1	α	R max.
0.65 0.55	45°	0.2

DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	b_{p1}	b_{p2}	c	D	D_1	D_2	$D_3^{(1)}$ max.	E	E_1	e	F	F_1	H_E	H_{E1}	L	L_1	L_2 min.	L_3	$L_4^{(1)}$ max.
mm	1.65 1.45	0.41 0.34	1.57 1.47	0.31 0.24	0.30 0.24	4.1 3.9	8.1 7.9	2.55	0.35	5.45 5.25	0.5	1.27	0.85 0.65	3.275 3.075	21.2 20.8	6.42 6.32	7.1 6.9	0.85 0.75	4.75	0.7 0.5	0.95

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic between and besides the leads.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT637						~~01-04-04~~ 02-01-18

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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SCA74

Printed in The Netherlands 613520/04/pp20 Date of release: 2002 Mar 25 Document order number: 9397 750 09313

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