Data Sheet No. PD60208_A

IR2175(S)

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low I_{QBS} allows the boot strap power supply
- Independent fast overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs

Description

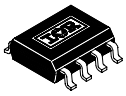
The IR2175 is a monolithic current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM to eliminate need for the A/D input interface for the IR2175. The dedicated overcurrent trip ($\overline{OC}$) signal facilitates IGBT short circuit protection. The open-drain outputs make easy for any interface from 3.3V to 15V. S

Product Summary

V_{OFFSET}	600Vmax
I_{QBS}	2mA
V_{in}	+/-260mVmax
Gain temp.drift	20ppm/^{o}C (typ.)
f_o	130kHz (typ.)
Overcurrent trip signal delay	2µsec (typ)
Overcurrent trip level	+/-260mV (typ.)

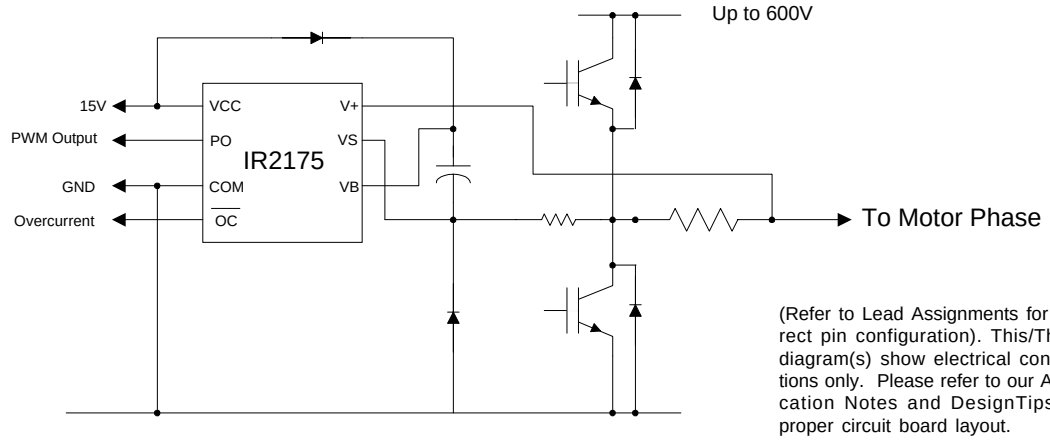
Packages

8 Lead PDIP



8 Lead SOIC

Block Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		-0.3	25	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Maximum input voltage between V_{IN+} and V_S		-5	5	
V_{PO}	Digital PWM output voltage		COM -0.3	VCC +0.3	
V_{OC}	Overcurrent output voltage		COM -0.3	VCC +0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: Capacitors are required between V_B and Vs when bootstrap power is used. The external power supply, when used, is required between V_B and Vs pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +13.0	V_S +20	V
V_S	High side floating supply offset voltage	0.3	600	
V_{PO}	Digital PWM output voltage	COM	VCC	
V_{OC}	Overcurrent output voltage	COM	VCC	
V_{CC}	Low side and logic fixed supply voltage	9.5	20	
V_{IN}	Input voltage between V_{IN+} and V_S	-260	+260	mV
T_A	Ambient temperature	-40	125	°C

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25° unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Nominal input voltage range before saturation $V_{IN+} - V_S$	-260	—	260	mV	
V_{OC+}	Overcurrent trip positive input voltage	—	260	—		
V_{OC-}	Overcurrent trip negative input voltage	—	-260	—		
V_{OS}	Input offset voltage	-10	0	10		V_{IN} = 0V (Note 1)
$\Delta V_{OS}/\Delta T_A$	Input offset voltage temperature drift	—	25	—	µV/°C	
G	Gain (duty cycle % per V_{IN})	155	160	165	%/V	max gain error=5% (Note 2)
$\Delta G/\Delta T_A$	Gain temperature drift	—	20	—	ppm/°C	
I_{LK}	Offset supply leakage current	—	—	50	µA	$V_B = V_S$ = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	2	—	mA	V_S = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	—	0.5		
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta V_{LIN}/\Delta T_A$	Linearity temperature drift	—	.005	—	%/°C	
I_{OPO}	Digital PWM output sink current	20	—	—	mA	V_O = 1V
		2	—	—		V_O = 0.1V
I_{OCC}	OC output sink current	10	—	—		V_O = 1V
		1	—	—		V_O = 0.1V

Note 1: ±10mV offset represents ±1.5% duty cycle fluctuation
Note 2: Gain = (full range of duty cycle in %) / (full input voltage range).

AC Electrical Characteristics

V_{CC} = V_{BS} = 15V, and T_A = 25° unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
fo	Carrier frequency output	95	130	165	kHz	figure 1
$\Delta f/\Delta T_A$	Temperature drift of carrier frequency	—	500	—	ppm/°C	V_{IN} = 0 & 5V
Dmin	Minimum duty	—	9	—	%	V_{IN}+=-260mV,
Dmax	Maximum duty	—	91	—	%	V_{IN}+=+260mV
BW	fo bandwidth	—	15	—	kHz	V_{IN}+ = 100mVpk -pk sine wave, gain=-3dB
PHS	Phase shift at 1kHz	—	-10	—	°	V_{IN}+ =100mVpk-pk sine wave
tdoc	Propagation delay time of OC	1	2	—	µsec	
twoc	Low true pulse width of OC	—	1.5	—		

Timing Waveforms

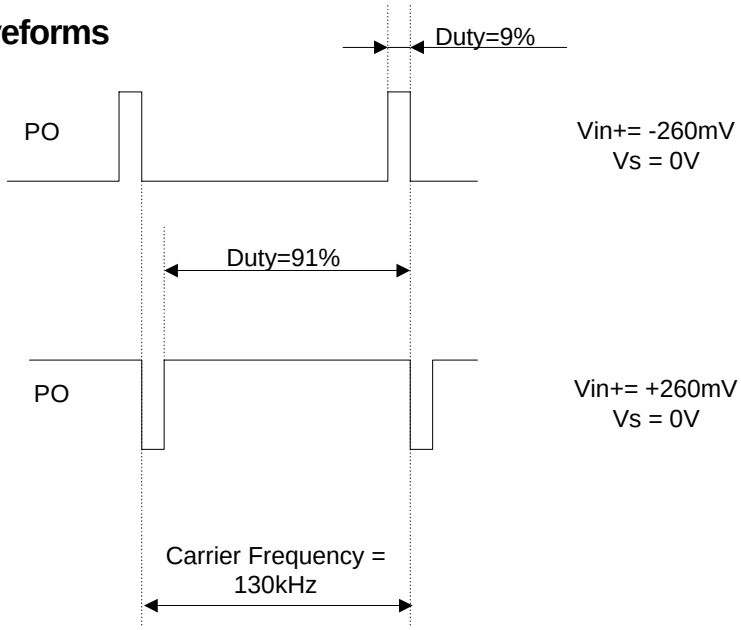


Figure 1 Output waveform

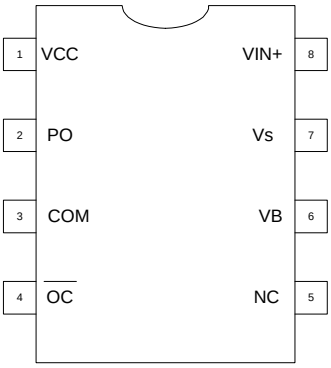
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at the same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM period gives consistent measurement of the current feedback over the temperature drift.

Lead Definitions

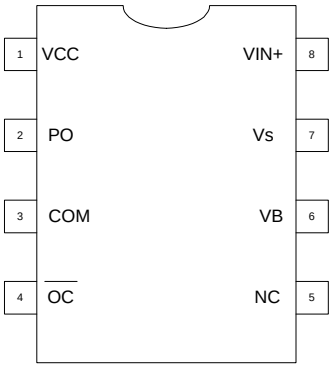
Symbol	Description
V_{CC}	Low side and logic supply voltage
COM	Low side logic ground
V_{IN+}	Positive sense input
V_B	High side supply
V_S	High side return
PO	Digital PWM output
$\overline{OC}$	Overcurrent output (negative logic)
N.C.	No connection

Lead Assignment



8 lead SOIC

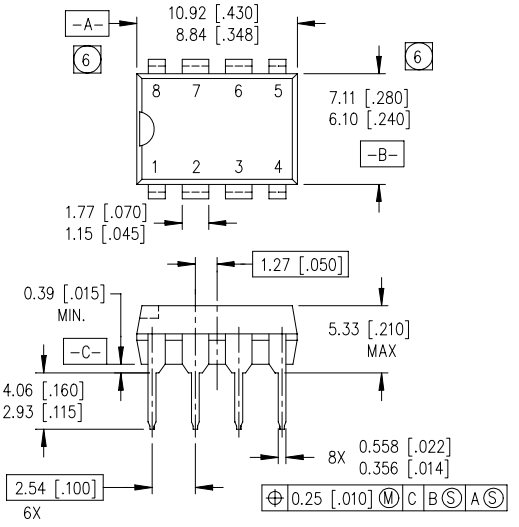
IR2175S



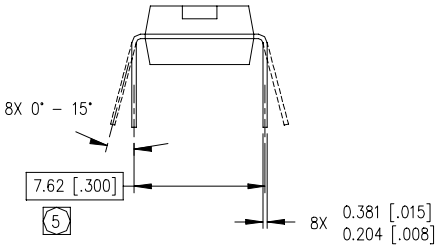
8 lead PDIP

IR2175

Case Outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



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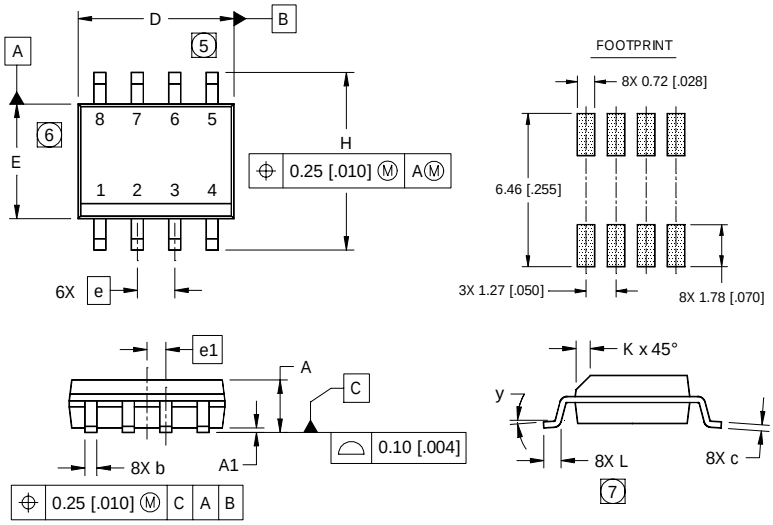

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

8 Lead SOIC

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