ICS8535-21

LOW SKEW, 1-TO-2 LVCMOS/LVTTL-TO-3.3V LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

ICS HiPerClockS™

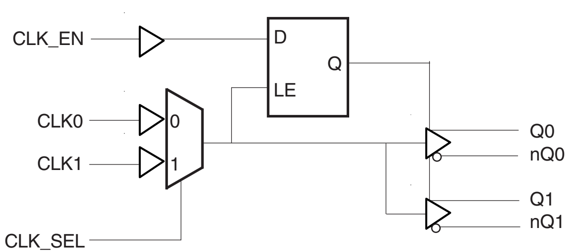
The ICS8535-21 is a low skew, high performance 1-to-2 LVCMOS/LVTTL-to-3.3V LVPECL fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8535-21 has two single-ended clock inputs. The single-ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The clock enable is internally synchronized to eliminate runt clock pulses on the output during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8535-21 ideal for those applications demanding well defined performance and repeatability.

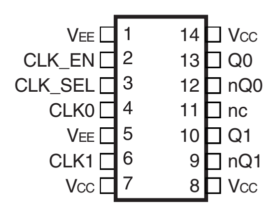
FEATURES

- 2 differential 3.3V LVPECL outputs
- Selectable CLK0 or CLK1 inputs for redundant and multiple frequency fanout applications
- CLK0 or CLK1 can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 266MHz
- Translates LVCMOS and LVTTL levels to 3.3V LVPECL levels
- Output skew: 20ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 1.6ns (maximum)
- Additive phase jitter, RMS: 0.03ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8535-21
14-Lead TSSOP
4.4mm x 5.0mm x 0.92mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5	V_{EE}	Power		Negative supply pins.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
4	CLK0	Input	Pulldown	LVCMOS / LVTTL clock input.
6	CLK1	Input	Pulldown	LVCMOS / LVTTL clock input.
7, 8, 14	V_{CC}	Power		Positive supply pins.
9, 10	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
11	nc	Unused		No connect.
12, 13	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0, Q1**	**nQ0, nQ1**
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in *Figure 1.*
In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 3B.

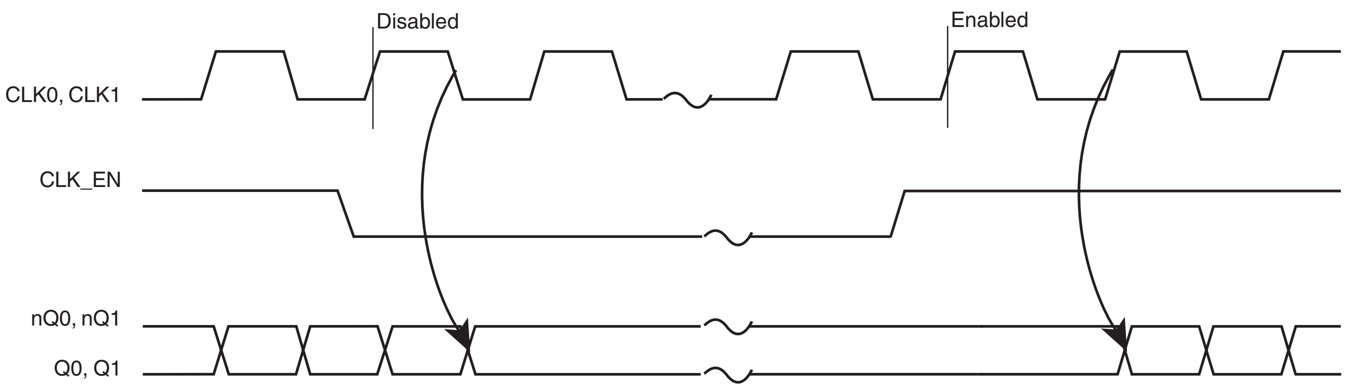


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs	Outputs	
CLK0 or CLK1	**Q0, Q1**	**nQ0, nQ1**
0	LOW	HIGH
1	HIGH	LOW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	93.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK0, CLK1		2		V_{CC} + 0.3	V
		CLK_EN, CLK_SEL		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

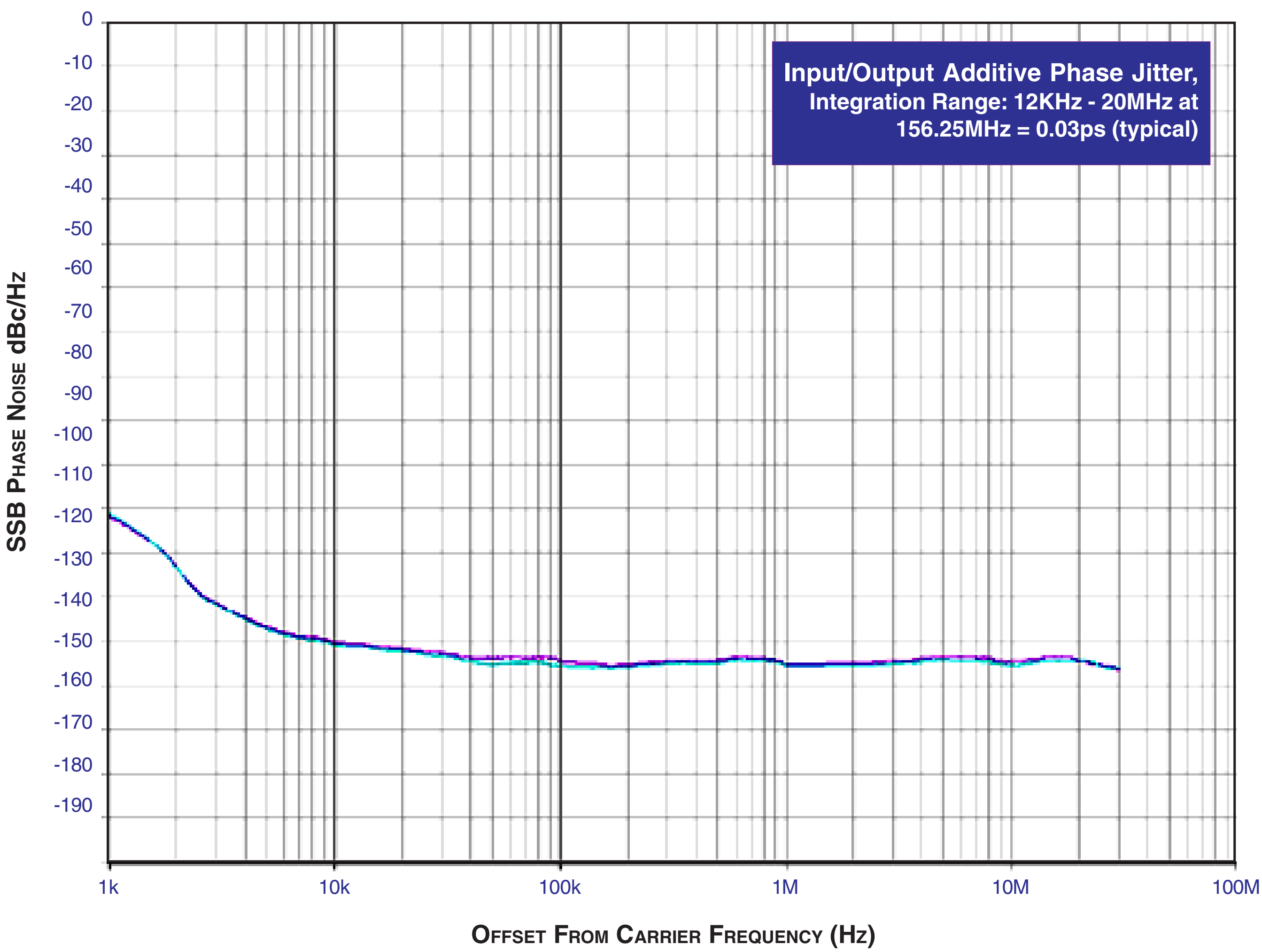
TABLE 5. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 266MHz	1.0		1.6	ns
*t*sk(o)	Output Skew; NOTE 2, 5				20	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				300	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 4	156.25MHz @ Integration Range: 12KHz - 20MHz		0.03		ps
t_R/t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		600	ps
odc	Output Duty Cycle	f ≤ 200MHz	45		55	%

All parameters measured at f ≤ 266MHz unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the $V_{CC}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Driving only one input clock.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

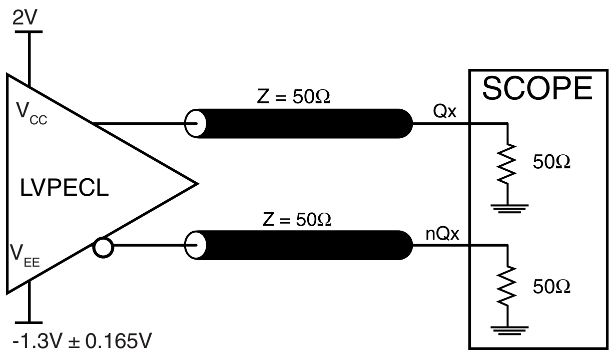
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

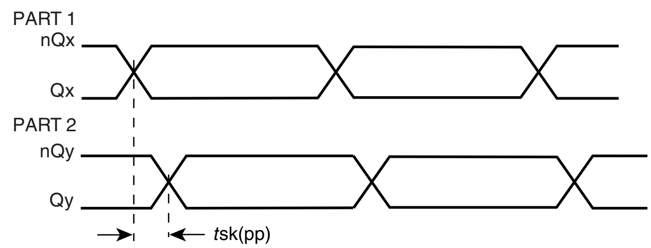


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

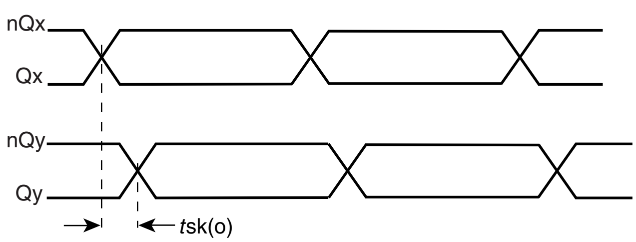
PARAMETER MEASUREMENT INFORMATION



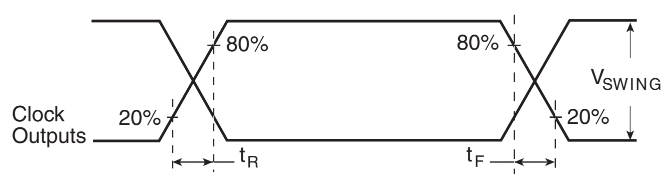
3.3V OUTPUT LOAD AC TEST CIRCUIT



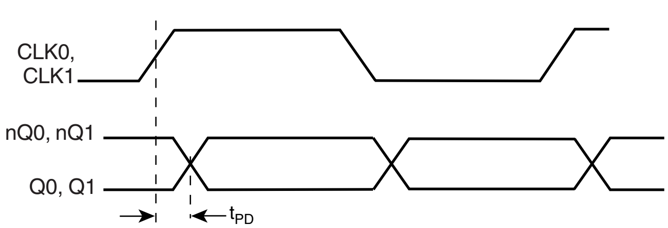
PART-TO-PART SKEW



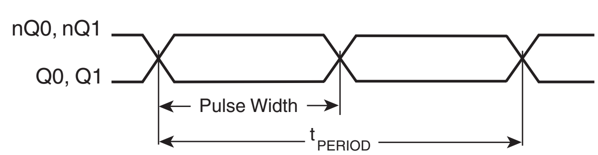
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

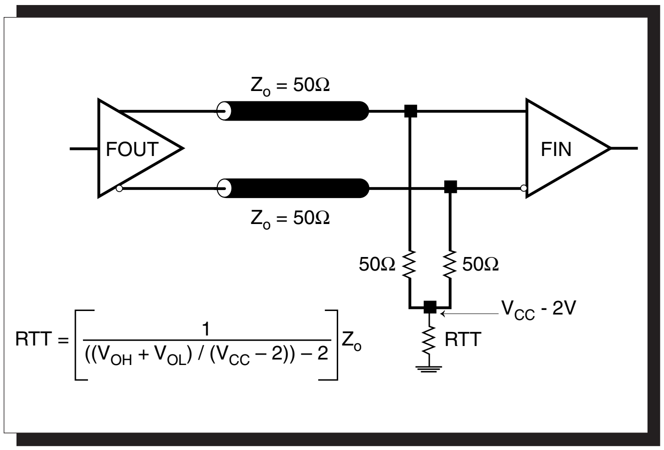


FIGURE 2A. LVPECL OUTPUT TERMINATION

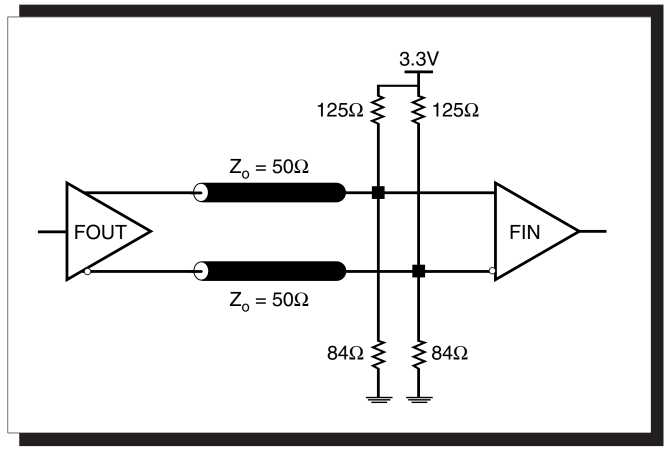


FIGURE 2B. LVPECL OUTPUT TERMINATION

SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of the ICS8535-21. The decoupling capacitors should be physically located near the power pin. For ICS8535-21, the unused clock outputs can be left floating.

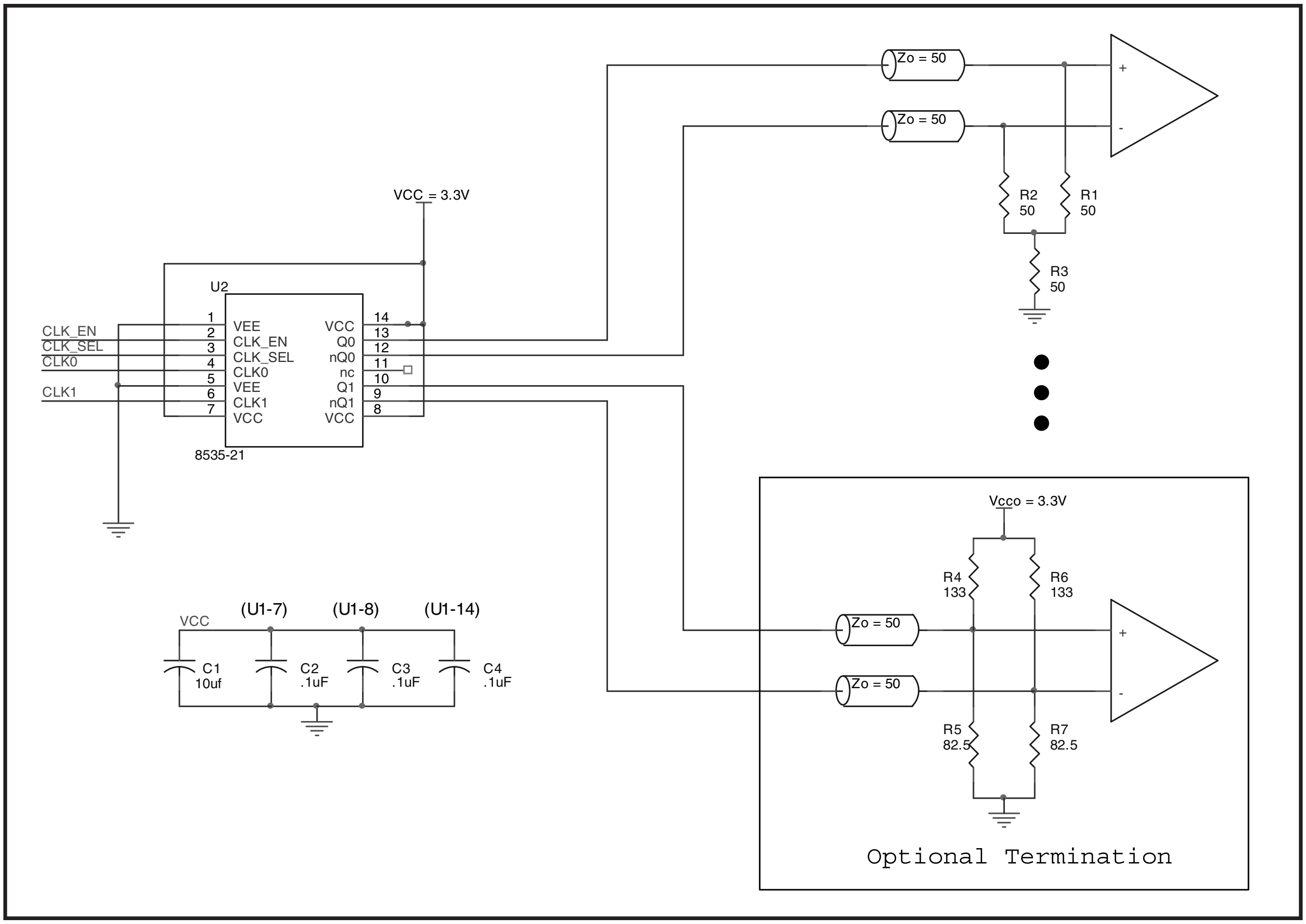


FIGURE 3. ICS8535-21 LVPECL BUFFER SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8535-21.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8535-21 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 50mA = **173.25mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 x 30mW = **60mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 173.25mW + 60mW = **233.25mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air low of 200 linear feet per minute and a multi-layer board, the appropriate value is 85.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.233W * 85.5°C/W = 90°C. This is well below the limit of 125°C.

This calculation is only an example, and the Tj will obviously vary depending on the number of outputs that are loaded, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 14-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	146.4°C/W	125.2°C/W	112.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	93.2°C/W	85.5°C/W	81.2°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

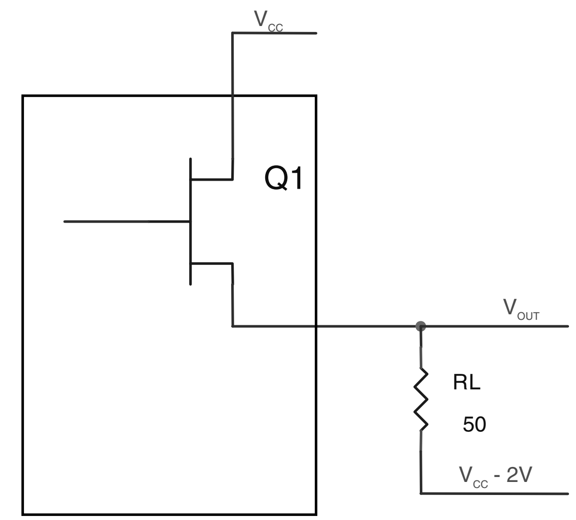


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 14 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	146.4°C/W	125.2°C/W	112.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	93.2°C/W	85.5°C/W	81.2°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8535-21 is: 412

PACKAGE OUTLINE - G SUFFIX FOR 14 LEAD TSSOP

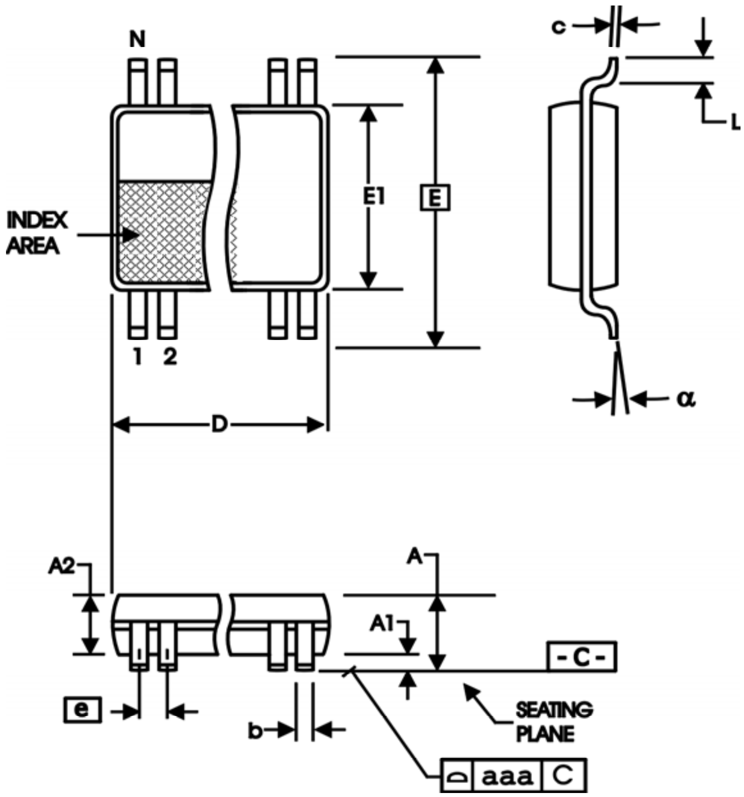


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	14	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8535AG-21	8535AG21	14 lead TSSOP	94 per tube	0°C to 70°C
ICS8535AG-21T	8535AG21	14 lead TSSOP on Tape and Reel	2500	0°C to 70°C