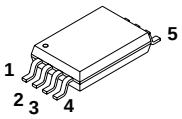
Data Sheet | July 2000 | File Number 4811.3

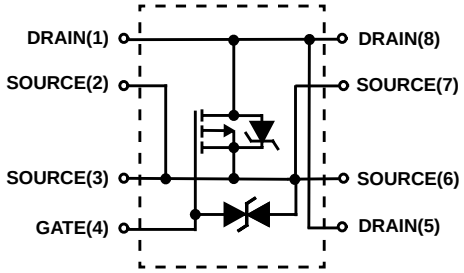
9A, 20V, 0.015 Ohm, P-Channel, 2.5V Specified Power MOSFET

Packaging

TSSOP-8



Symbol



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)}$ = 0.015Ω, V_{GS} = –4.5V
  - $r_{DS(ON)}$ = 0.016Ω, V_{GS} = –4.0V
  - $r_{DS(ON)}$ = 0.023Ω, V_{GS} = –2.5V
- 2.5V Gate Drive Capability
- Gate to Source Protection Diode
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.intersil.com
- Peak Current vs Pulse Width Curve
- Transient Thermal Impedance Curve vs Board Mounting Area
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
ITF87068SQT	TSSOP-8	87068

NOTE: When ordering, use the entire part number. ITF87068SQT2 is available only in tape and reel.

Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		ITF87068SQT	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	-20	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	-20	V
Gate to Source Voltage	V_{GS}	±12	V
Drain Current			
Continuous ($T_A = 25^oC$, V_{GS} = -4.5V) (Note 2)	I_D	9.0	A
Continuous ($T_A = 25^oC$, V_{GS} = -4.0V) (Note 2)	I_D	9.0	A
Continuous ($T_A = 100^oC$, V_{GS} = -4.0V) (Note 2)	I_D	5.5	A
Continuous ($T_A = 100^oC$, V_{GS} = -2.5V) (Note 2)	I_D	4.5	A
Pulsed Drain Current	I_{DM}	Figure 4	
Power Dissipation (Note 2)	P_D	2.0	W
Derate Above 25^oC		16	$mW/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief TB370	T_{pkg}	260	^oC

NOTES:

1. $T_J = 25^oC$ to 125^oC.
2. $62.5^oC/W$ measured using FR-4 board with 1.0 in^2 (645.2 mm^2) copper pad at 10s.

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V Figure 11	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20V, V_{GS} = 0V	-	-	-10	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±12V	-	-	±10	µA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA Figure 10	-0.5	-	-1.5	V
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 9.0A, V_{GS} = -4.5V Figures 8,9	-	0.012	0.015	Ω
		I_D = 5.5A, V_{GS} = -4.0V Figure 8	-	0.013	0.016	Ω
		I_D = 4.5A, V_{GS} = -2.5V Figure 8	-	0.017	0.023	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 1.0 in^2 (645.2 mm^2) (Note 2)	-	-	62.5	$^oC/W$
		Pad Area = 0.035 in^2 (22.4 mm^2) Figure 20	-	-	165.4	$^oC/W$
		Pad Area = 0.0045 in^2 (2.88 mm^2) Figure 20	-	-	206.8	$^oC/W$
SWITCHING SPECIFICATIONS V_{GS} = -2.5V						
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -10V, I_D = 4.5A V_{GS} = -2.5V, R_{GS} = 5Ω Figures 14, 18, 19	-	25	-	ns
Rise Time	t_r		-	120	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	-	ns
Fall Time	t_f		-	68	-	ns
SWITCHING SPECIFICATIONS V_{GS} = -4.5V						
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = -10V, I_D = 9.0A V_{GS} = -4.5V, R_{GS} = 5Ω Figures 15, 18, 19	-	17	-	ns
Rise Time	t_r		-	110	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	68	-	ns
Fall Time	t_f		-	92	-	ns
GATE CHARGE SPECIFICATIONS						
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to -4.5V; V_{DD} = -10V, I_D = 9.0A, $I_{g(REF)}$ = -1.0mA Figures 13, 16, 17	-	28	-	nC
Gate Charge at -2V	$Q_{g(-2)}$	V_{GS} = 0V to -2V	-	14	-	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to -0.5V	-	1.5	-	nC
Gate to Source Gate Charge	Q_{gs}		-	3.5	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	5.5	-	nC
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz Figure 12	-	3000	-	pF
Output Capacitance	C_{OSS}		-	685	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	315	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = -9.0A	-	-0.8	-	V
Reverse Recovery Time	t_{rr}	I_{SD} = -9.0A, dI_{SD}/dt = 100A/µs	-	26	-	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = -9.0A, dI_{SD}/dt = 100A/µs	-	12	-	nC

Typical Performance Curves

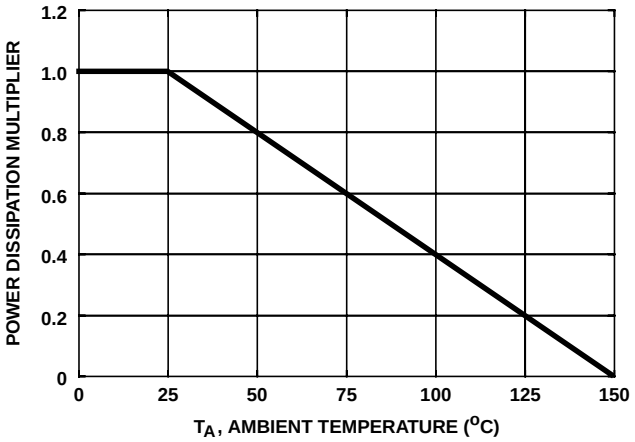


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

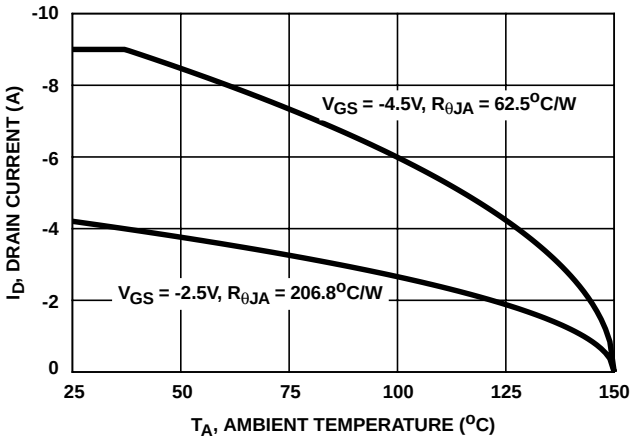


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

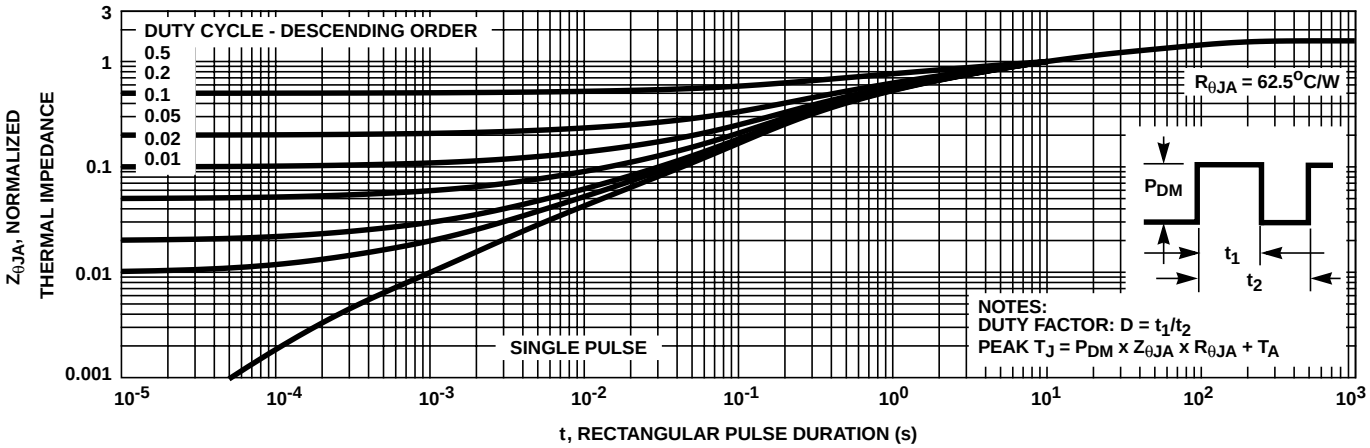


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

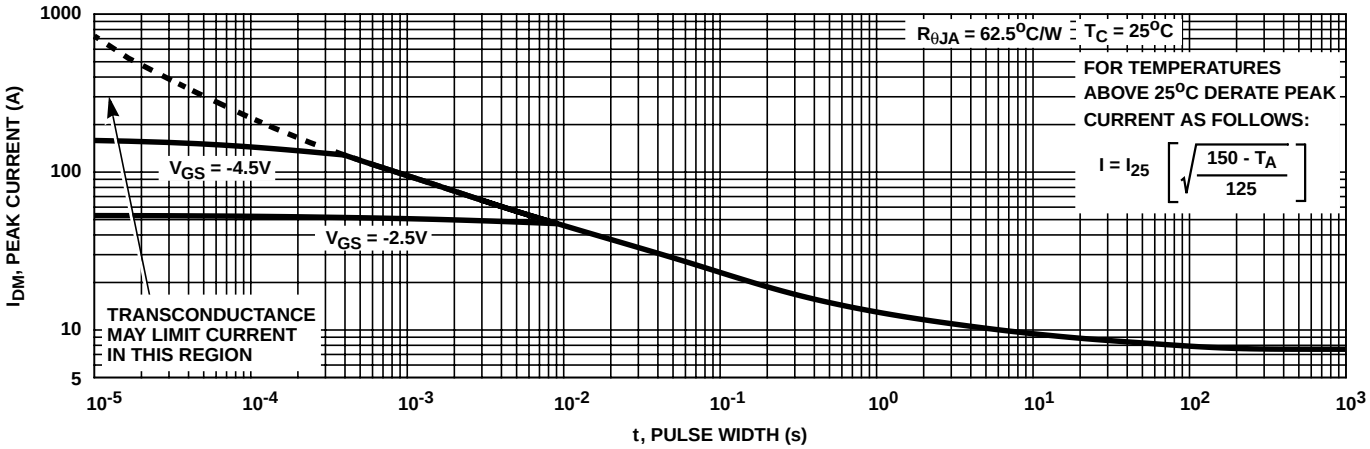


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

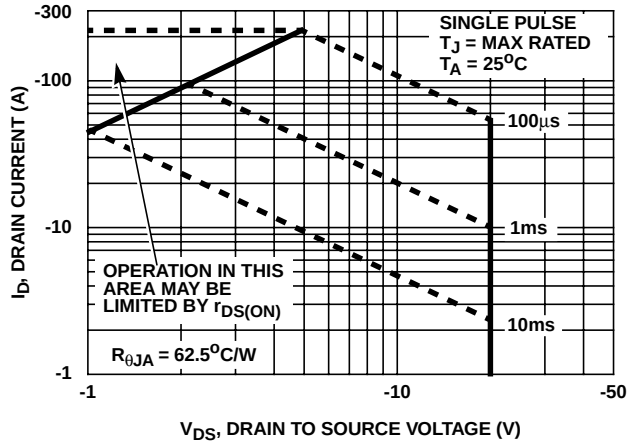


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

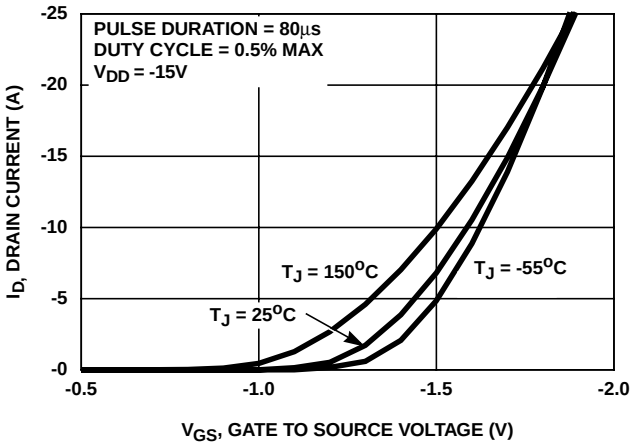


FIGURE 6. TRANSFER CHARACTERISTICS

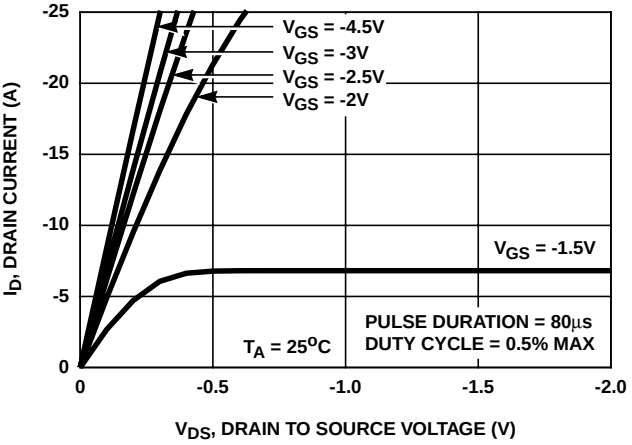


FIGURE 7. SATURATION CHARACTERISTICS

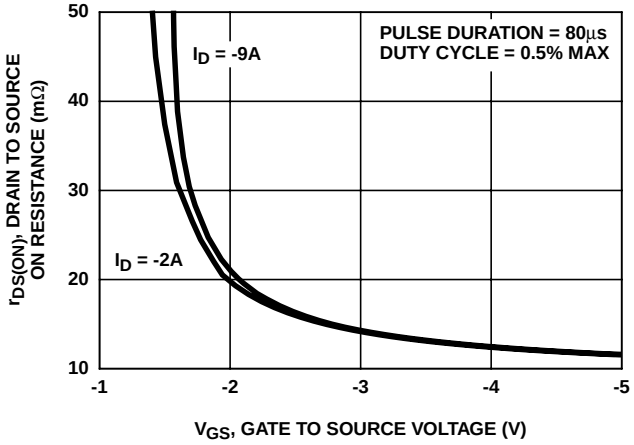


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

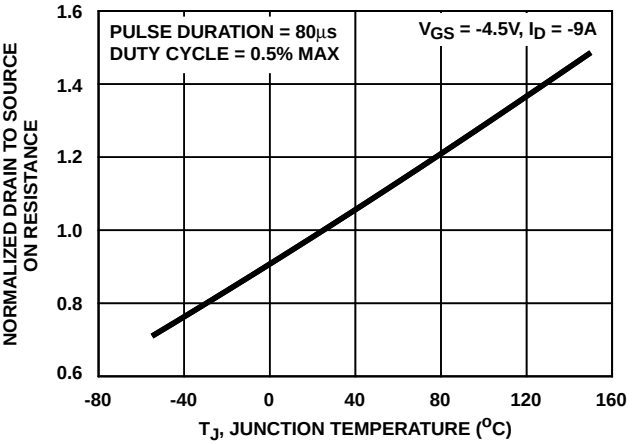


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

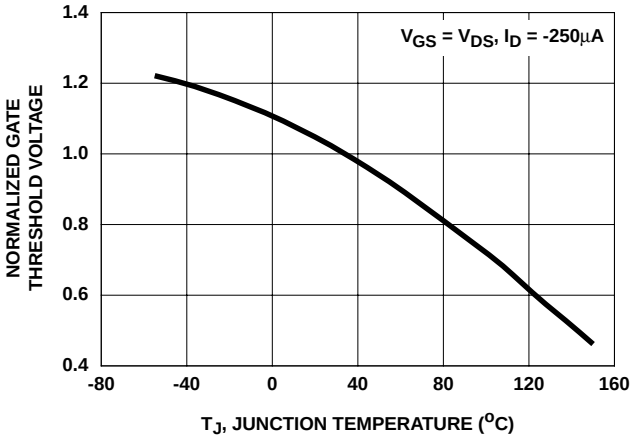


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

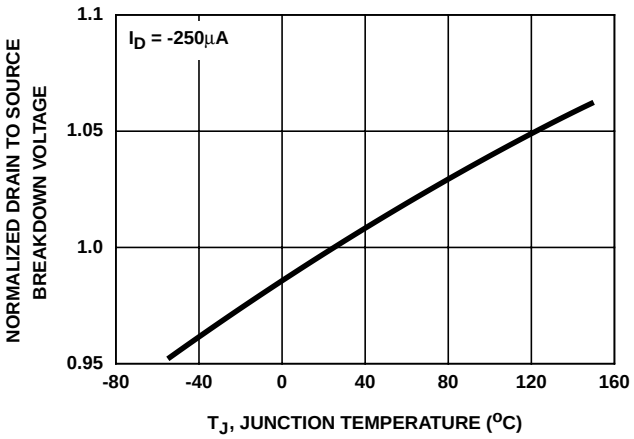


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

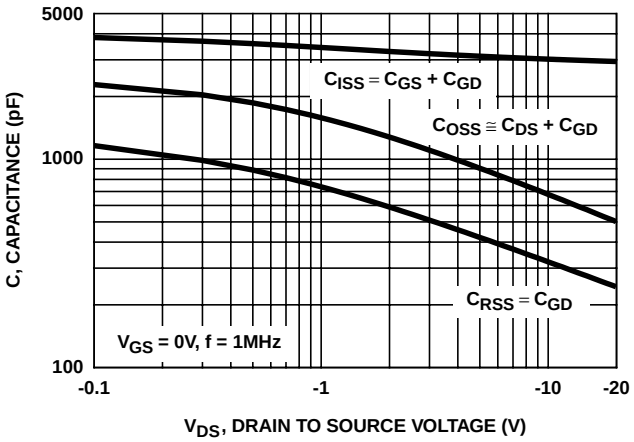
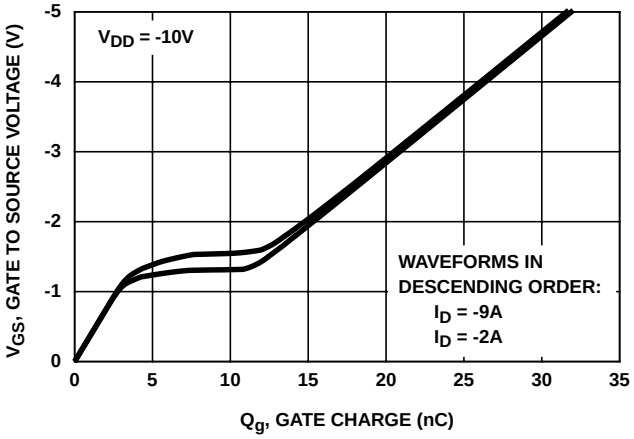


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

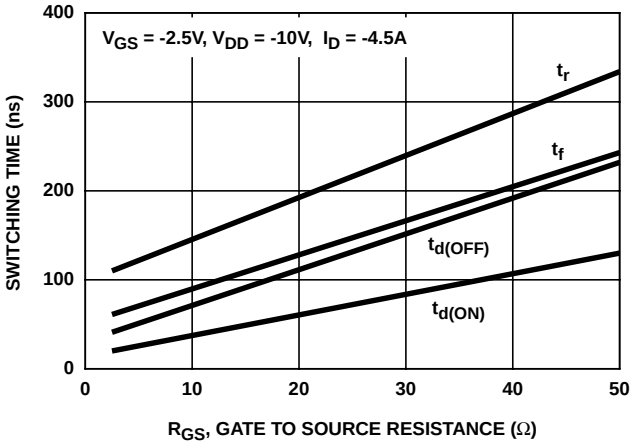


FIGURE 14. SWITCHING TIME vs GATE RESISTANCE

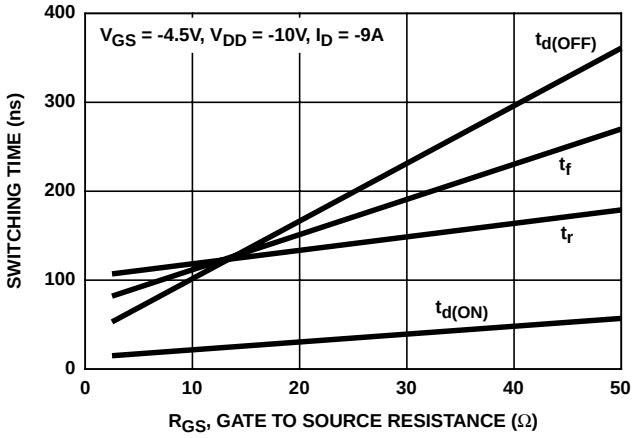


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

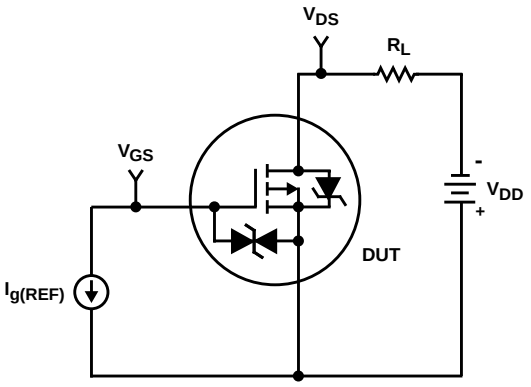


FIGURE 16. GATE CHARGE TEST CIRCUIT

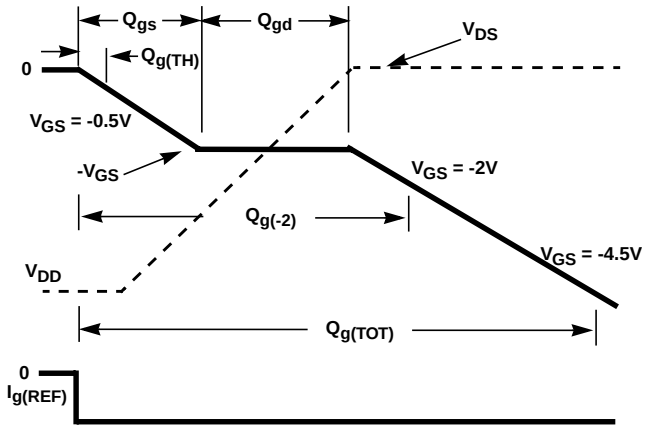


FIGURE 17. GATE CHARGE WAVEFORMS

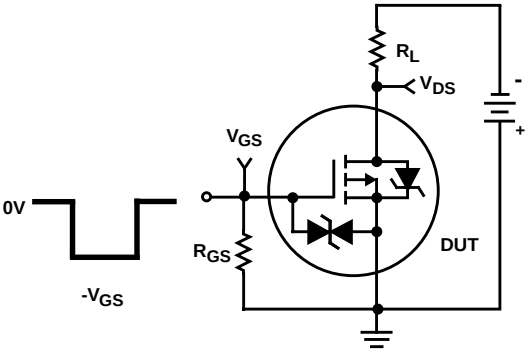


FIGURE 18. SWITCHING TIME TEST CIRCUIT

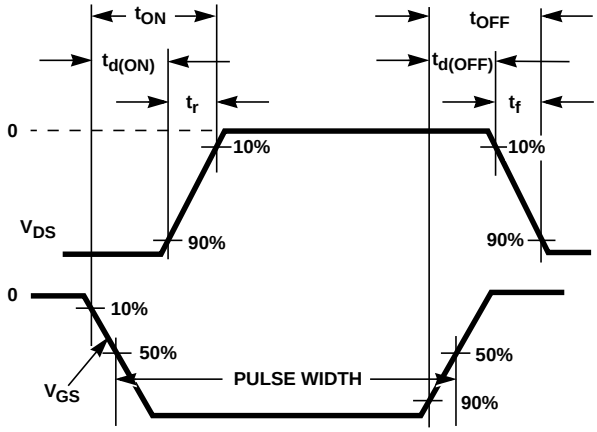


FIGURE 19. SWITCHING TIME WAVEFORM

Thermal Resistance vs Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^{0}C), and thermal resistance $R_{\theta JA}$ (^{0}C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \quad \text{(EQ. 1)}$$

In using surface mount devices such as the TSSOP-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Intersil provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the

necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Intersil device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

Thermal resistances corresponding to other copper areas can be obtained from Figure 20 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 97.5 - 20.2 \times ln(Area) \quad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 21 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

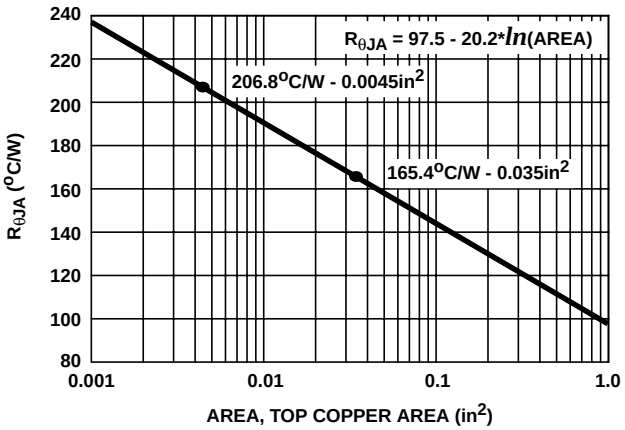


FIGURE 20. THERMAL RESISTANCE vs MOUNTING PAD AREA

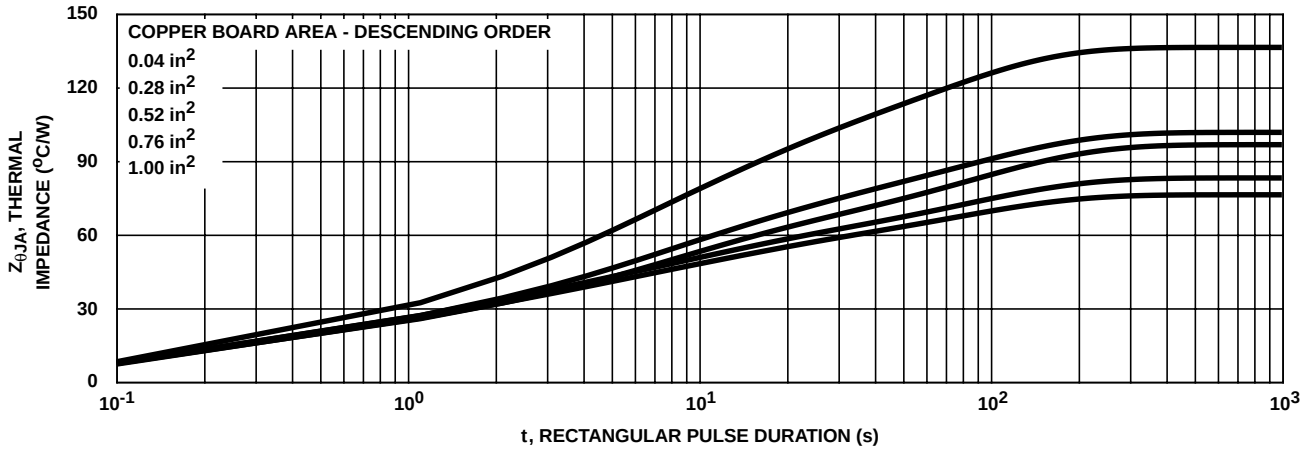


FIGURE 21. THERMAL IMPEDANCE vs MOUNTING PAD AREA

PSPICE Electrical Model

.SUBCKT ITF87068SQ 2 1 3 ; REV 25 Jan 2000

CA 12 8 2.8e-9
CB 15 14 2.8e-9
CIN 6 8 2.7e-9

DBODY 5 7 DBODYMOD
DBREAK 7 11 DBREAKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -31.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTHRES 6 21 19 8 1
EVTEMP 6 20 18 22 1

IT 8 17 1

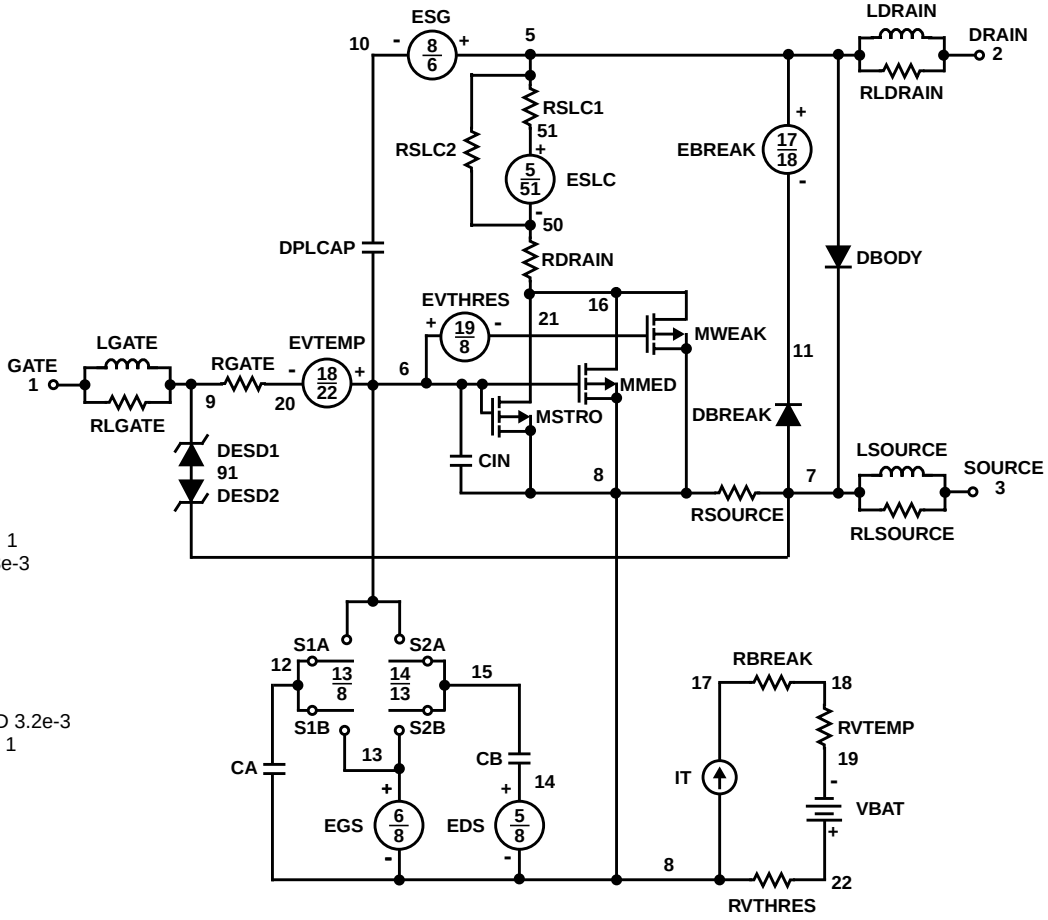
LDRAIN 2 5 1.0e-9
LGATE 1 9 4.4e-9
LSOURCE 3 7 4.5e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 5.8e-3
RGATE 9 20 3.5
RLDRAIN 2 5 10
RLGATE 1 9 9 44
RLSOURCE 3 7 45
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3.2e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*200),2.8))}

.MODEL DBODYMOD D (IS = 2.8e-10 RS = 4.7e-3 TRS1 = 1.75e-3 TRS2 = -1.0e-6 N = 1.08 IKF = 0.8 CJO = 1.2e-9 TT = 1.0e-9 M = 0.5)
.MODEL DBREAKMOD D (RS = 3.5e-1 TRS1 = 1.0e-3 TRS2 = -2.0e-5)
.MODEL DESD1MOD D (BV=12.2 TBV1= -2.0e-3 RS=35 N=12.4)
.MODEL DESD2MOD D (BV=12.4 TBV1= -2.0e-3 RS=35 N=12.5)
.MODEL DPLCAPMOD D (CJO = 1.25e-9 IS = 1e-30 N=10 VJ=0.39 M = 0.41)
.MODEL MMEDMOD PMOS (VTO = -1.0 KP = 35 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.5 RS = 0.1)
.MODEL MSTROMOD PMOS (VTO = -1.16 KP = 100 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD PMOS (VTO = -0.7 KP = 0.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 35 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 6.3e-4 TC2 = -5.0E-7)
.MODEL RDRAINMOD RES (TC1 = 5.0e-3 TC2 = 1.2e-6)
.MODEL RSLCMOD RES (TC1 = 1.0e-3 TC2 = 1.0e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = 1.2e-3 TC2 = 4.9e-6)
.MODEL RVTEMPMOD RES (TC1 = -3.3e-4 TC2 = -1.0e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.5 VOFF= 1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.5 VOFF= 2.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.75 VOFF= -0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF= 0.75)

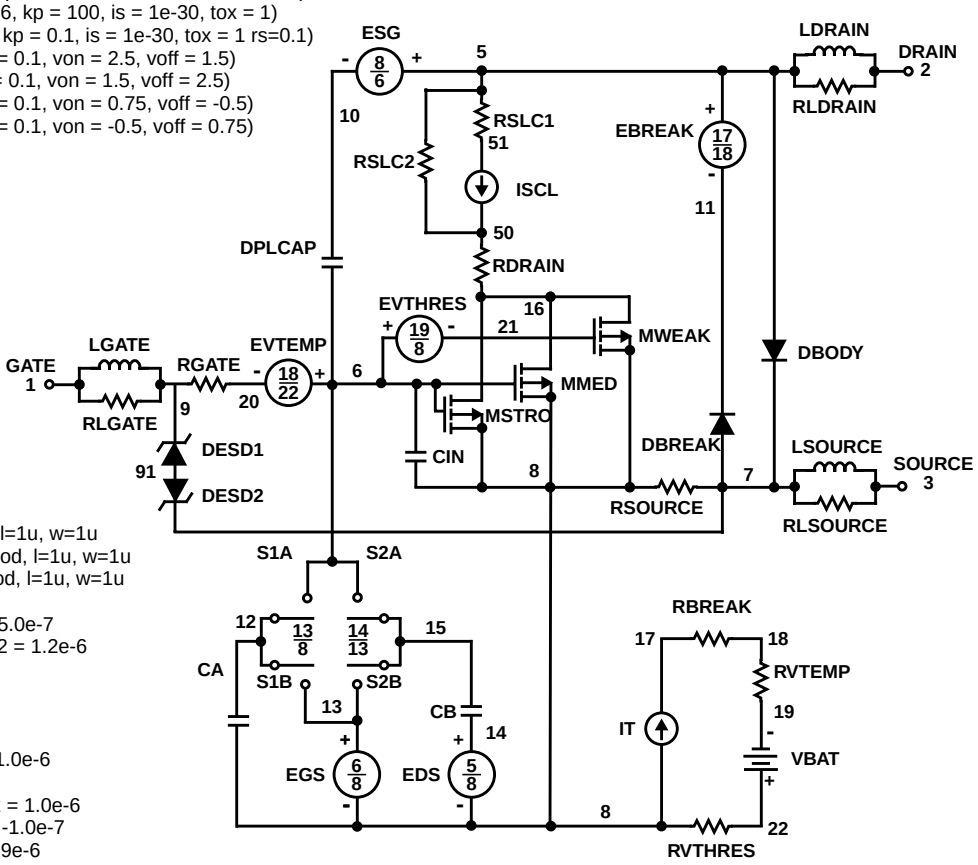
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 25 Jan 2000

```
template ITF87068SQ n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl = 2.8e-10, nl = 1.08, cjo = 1.2e-9, tt = 1.0e-9, m = 0.5, rs = 4.7e-3, trs1 = 1.75e-3, trs2 = -1.0e-6, ikf = 0.8)
dp..model dbreakmod = (rs = 3.5e-1, trs1 = 1.0e-3, trs2 = -2.0e-5)
dp..desd1mod = (bv = 12.2, tbv1 = -2.0e-3, rs = 35, nl = 12.4)
dp..desd2mod = (bv = 12.4, tbv1 = -2.0e-3, rs = 35, nl = 12.5)
dp..model dplcapmod =  (cjo = 1.25e-9, isl = 10e-30, nl = 10, vj=0.39, m = 0.41 )
m..model mmedmod = (type=_p, vto = -1.0, kp = 35, is = 1e-30, tox = 1, rs=0.1)
m..model mstrongmod = (type=_p, vto = -1.16, kp = 100, is = 1e-30, tox = 1)
m..model mweakmod = (type=_p, vto = -0.7, kp = 0.1, is = 1e-30, tox = 1 rs=0.1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = 2.5, voff = 1.5)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = 1.5, voff = 2.5)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = 0.75, voff = -0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.75)

c.ca n12 n8 = 2.8e-9
c.cb n15 n14 = 2.8e-9
c.cin n6 n8 = 2.7e-9

dp.dbody n5 n7 = model=dbodymod
dp.dbreak n7 n11 = model=dbreakmod
dp.dplcap n10 n6 = model=dplcapmod
dp.desd1 n91 n9 = model=desd1mod
dp.desd2 n91 n7 = model=desd2mod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.0e-9
l.lgate n1 n9 = 4.4e-9
l.lsource n3 n7 = 4.5e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 6.3e-4, tc2 = -5.0e-7
res.rdrain n50 n16  = 5.8e-3, tc1 = 5.0e-3, tc2 = 1.2e-6
res.rgate n9 n20 = 3.5
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 44
res.rlsource n3 n7 = 45
res.rslc1 n5 n51  = 1e-6, tc1 = 1.0e-3, tc2 = 1.0e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 3.2e-3, tc1 = 1.0e-3, tc2 = 1.0e-6
res.rvtemp n18 n19  = 1, tc1 = -3.3e-4, tc2 = -1.0e-7
res.rvthres n22 n8  = 1, tc1 = 1.2e-3, tc2 = 4.9e-6

spe.ebreak n11 n7 n17 n18 = -31.3
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n5 n10 n8 n6 = 1
spe.evtemp n6 n20 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/200))** 2.8))
}
}
```



SPICE Thermal Model

REV 27 December 1999
ITF87068SQT
Copper Area = 1.0 in^2
CTHERM1 th 8 1.5e-3
CTHERM2 8 7 5.0e-3
CTHERM3 7 6 1.0e-2
CTHERM4 6 5 2.0e-2
CTHERM5 5 4 5.0e-2
CTHERM6 4 3 0.2
CTHERM7 3 2 0.5
CTHERM8 2 tl 3.0

RTHERM1 th 8 0.15
RTHERM2 8 7 0.5
RTHERM3 7 6 1.25
RTHERM4 6 5 8
RTHERM5 5 4 12
RTHERM6 4 3 12
RTHERM7 3 2 18
RTHERM8 2 tl 25

SABER Thermal Model

Copper Area = 1.0 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 = 1.5e-3
ctherm.ctherm2 8 7 = 5.0e-3
ctherm.ctherm3 7 6 = 1.0e-2
ctherm.ctherm4 6 5 = 2.0e-2
ctherm.ctherm5 5 4 = 5.0e-2
ctherm.ctherm6 4 3 = 0.2
ctherm.ctherm7 3 2 = 0.5
ctherm.ctherm8 2 tl = 3.0

rtherm.rtherm1 th 8 = 0.15
rtherm.rtherm2 8 7 = 0.5
rtherm.rtherm3 7 6 = 1.25
rtherm.rtherm4 6 5 = 8
rtherm.rtherm5 5 4 = 12
rtherm.rtherm6 4 3 = 12
rtherm.rtherm7 3 2 = 18
rtherm.rtherm8 2 tl = 25
}

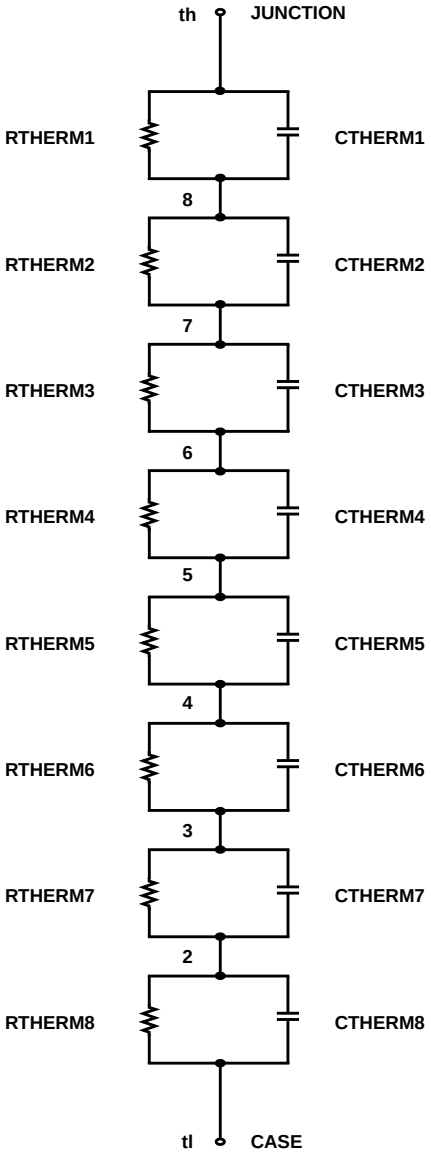
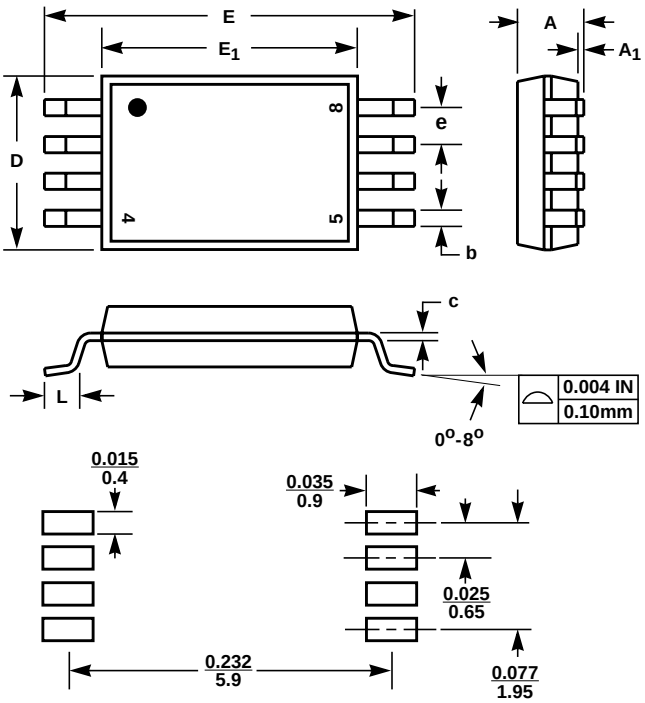


TABLE 1. THERMAL MODELS

COMPONENT	0.04 in^2	0.28 in^2	0.52 in^2	0.76 in^2	1.0 in^2
CTHERM6	0.12	0.2	0.28	0.19	0.2
CTHERM7	0.25	0.48	0.45	0.39	0.5
CTHERM8	1.3	2.3	2.2	2.7	3.0
RTHERM6	26	20	15	11	12
RTHERM7	39	24	21	21	18
RTHERM8	49.5	36.8	39	29.5	25

MO-153AA (TSSOP-8)

8 LEAD JEDEC MO-153AA TSSOP PLASTIC PACKAGE



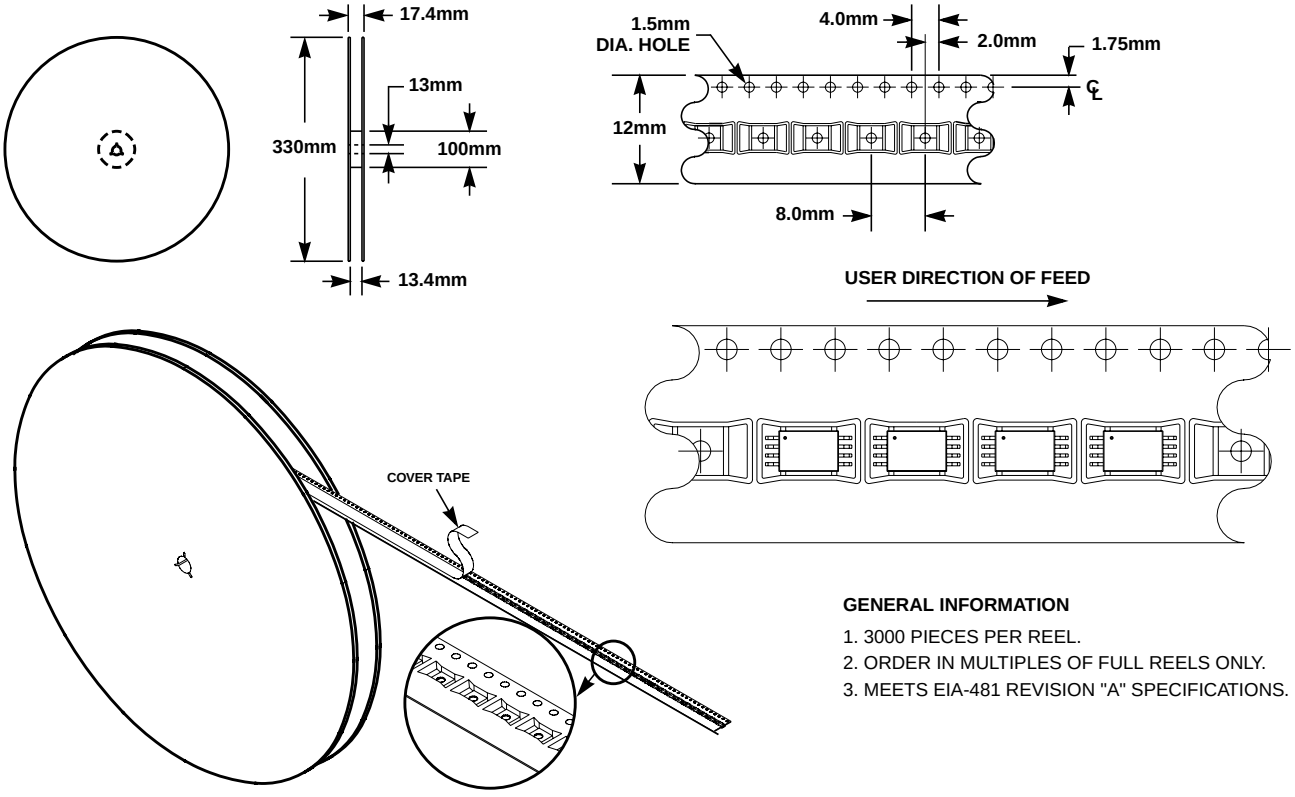
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A_1	0.002	0.006	0.05	0.15	-
b	0.010	0.012	0.25	0.30	-
c	0.005		0.127		-
D	0.114	0.122	2.90	3.10	2
E	0.244	0.260	6.20	6.60	-
E_1	0.170	0.177	4.30	4.50	3
e	0.025 BSC		0.65 BSC		-
L	0.020	0.028	0.50	0.70	4

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC MO-153AA outline dated 10-97.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension “E_1” does not include inter-lead flash or protrusions. Interlead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. “L” is the length of terminal for soldering.
5. Controlling dimension: Millimeter
6. Revision 3 dated: 5-00.

MO-153AA (TSSOP-8)

12mm TAPE AND REEL



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