HM-65642

8K x 8 Asynchronous CMOS Static RAM

March 1997

Features

- **Full CMOS Design**
- **Six Transistor Memory Cell**
- **Low Standby Supply Current 100µA**
- **Low Operating Supply Current. 20mA**
- **Fast Address Access Time 150ns**
- **Low Data Retention Supply Voltage. 2.0V**
- **CMOS/TTL Compatible Inputs/Outputs**
- **JEDEC Approved Pinout**
- **Equal Cycle and Access Times**
- **No Clocks or Strobes Required**
- **Gated Inputs**
- **No Pull-Up or Pull-Down Resistors Required**
- **Easy Microprocessor Interfacing**
- **Dual Chip Enable Control**

Description

The HM-65642 is a CMOS 8192 x 8-bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8-bit wide standard, which allows easy memory board layouts which accommodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Intersil 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

The HM-65642 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices.

Ordering Information

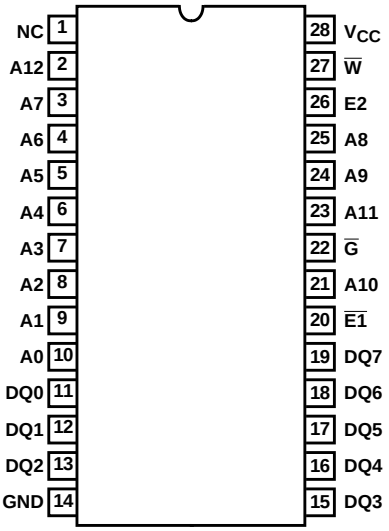
PACKAGE	TEMPERATURE RANGE	(NOTE 1) 150ns/75µA	(NOTE 1) 150ns/150µA	(NOTE 1) 200ns/250µA	PKG. NO.
CERDIP	-40°C to +85°C	-	HM1-65642-9	-	F28.6
JAN#	-55°C to +125°C	29205BXA	-	-	F28.6

NOTE:

1. Access Time/Data Retention Supply Current.

Pinout

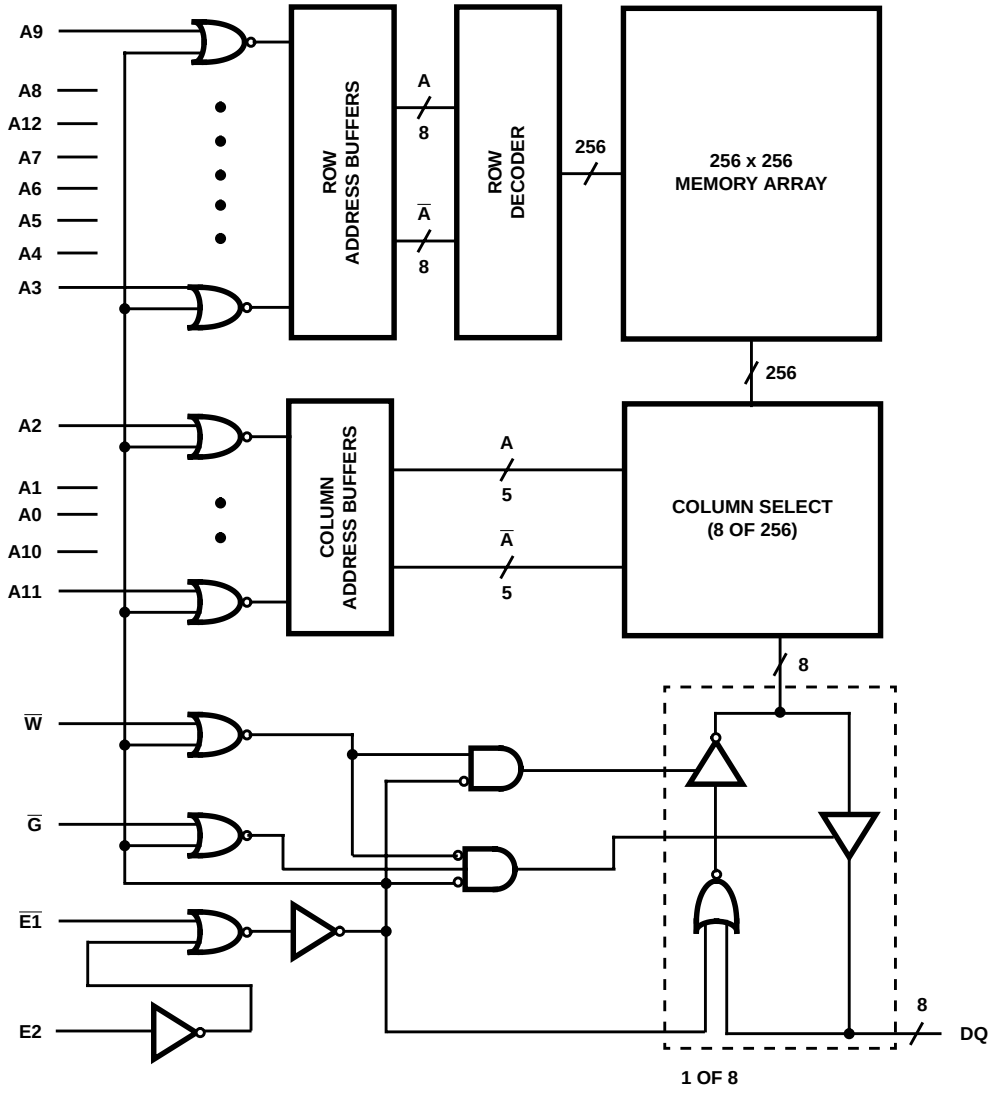
HM-65642 (CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
NC	No Connections
GND	Ground
V_{CC}	Power

File Number **3005.1**

Functional Diagram



TRUTH TABLE

MODE	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	X	GND	X	X
Standby (TTL)	V_{IH}	X	X	X
	X	V_{IL}	X	X
Enable (High Z)	V_{IL}	V_{IH}	V_{IH}	V_{IH}
Write	V_{IL}	V_{IH}	V_{IL}	X
Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage Applied for All Grades . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
CERDIP Package	$45^oC/W$	$8^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 101,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-65642-9 . . . . . -40^oC to $+85^oC$
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . +2.2V to V_{CC} +0.3V

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-65642-9)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	250	µA	E2 = GND, V_{CC} = 5.5V
ICCSB2	Standby Supply Current (TTL)	-	5	mA	E2 = 0.8V or $\overline{E1}$ = 2.2V, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	-	150	µA	E2 = GND, V_{CC} = 2.0V
ICCEN	Enabled Supply Current	-	5	mA	E2 = 2.2V, $\overline{E1}$ = 0.8V, V_{CC} = 5.5V, IIO = 0mA
ICCOP	Operating Supply Current (Note 1)	-	20	mA	f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V, V_{CC} = 5.5V, IIO = 0mA
II	Input Leakage Current	-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	E2 = GND, VIO = V_{CC} or GND, V_{CC} = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
VOH1	Output High Voltage	2.4	-	V	IOH = -1.0mA, V_{CC} = 4.5V
VOH2	Output High Voltage (Note 2)	V_{CC} -0.4	-	V	IOH = -100µA, V_{CC} = 4.5V
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0mA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	12	pF	f = 1MHz, All measurements are referenced to device GND
CIO	Input/Output Capacitance (Note 2)	14	pF	

NOTES:

1. Typical derating 5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-65642-9)

SYMBOL	PARAMETER			LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
READ CYCLE							
(1) TAVAX	Read Cycle Time			150	-	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time			-	150	ns	(Notes 1, 3)
(3) TE1LQV	Chip Enable Access Time		$\overline{E1}$	-	150	ns	(Notes 2, 3)
(4) TE2HQV	Chip Enable Access Time		E2	-	150	ns	(Notes 1, 3)
(5) TGLQV	Output Enable Access Time			-	70	ns	(Notes 1, 3)
(6) TE1LQX	Chip Enable Valid to Output On		$\overline{E1}$	10	-	ns	(Notes 2, 3)
(7) TE2HQX	Chip Enable Valid to Output On		E2	10	-	ns	(Notes 2, 3)
(8) TGLQX	Output Enable Valid to Output On			5	-	ns	(Notes 2, 3)
(9) TE1HQZ	Chip Enable Not Valid to Output Off		$\overline{E1}$	-	50	ns	(Notes 2, 3)
(10) TE2LQZ	Chip Enable Not Valid to Output Off		E2	-	60	ns	(Notes 2, 3)
(11) TGHQZ	Output Enable Not Valid to Output Off			-	50	ns	(Notes 2, 3)
(12) TAXQX	Output Hold From Address Change			10	-	ns	(Notes 2, 3)
WRITE CYCLE							
(13) TAVAX	Write Cycle Time			150	-	ns	(Notes 1, 3)
(14) TWLWH	Write Pulse Width			90	-	ns	(Notes 1, 3)
(15) TE1LE1H	Chip Enable to End of Write		$\overline{E1}$	90	-	ns	(Notes 1, 3)
(16) TE2HE2L	Chip Enable to End of Write		E2	90	-	ns	(Notes 1, 3)
(17) TAVWL	Address Setup Time	Late Write		0	-	ns	(Notes 1, 3)
(18) TAVE1L	Address Setup Time	Early Write	$\overline{E1}$	0	-	ns	(Notes 1, 3)
(19) TAVE2H	Address Setup Time	Early Write	E2	0	-	ns	(Notes 1, 3)
(20) TWHAX	Write Recovery Time	Late Write		10	-	ns	(Notes 1, 3)
(21) TE1HAX	Write Recovery Time	Early Write	$\overline{E1}$	10	-	ns	(Notes 1, 3)
(22) TE2LAX	Write Recovery Time	Early Write	E2	10	-	ns	(Notes 1, 3)
(23) TDVWH	Data Setup Time	Late Write		60	-	ns	(Notes 1, 3)
(24) TDVE1H	Data Setup Time	Early Write	$\overline{E1}$	60	-	-	(Notes 1, 3)
(25) TDVE2L	Data Setup Time	Early Write	E2	60	-	ns	(Notes 1, 3)
(26) TWHDX	Data Hold Time	Late Write		5	-	ns	(Notes 1, 3)
(27) TE1HDX	Data Hold Time	Early Write	$\overline{E1}$	10	-	ns	(Notes 1, 3)
(28) TE2LDX	Data Hold Time	Early Write	E2	10	-	ns	(Notes 1, 3)
(29) TWLQZ	Write Enable Low to Output Off			-	50	ns	(Notes 2, 3)
(30) TWHQX	Write Enable High to Output On			5	-	ns	(Notes 2, 3)

NOTES:

1. Input pulse levels: 0V to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.

Low Voltage Data Retention

Intersil CMOS RAMs are designed with battery backup in mind. Data Retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of V_{CC}.
3. The RAM can begin operating one TAVAX after V_{CC} reaches the minimum operating voltage of 4.5V.

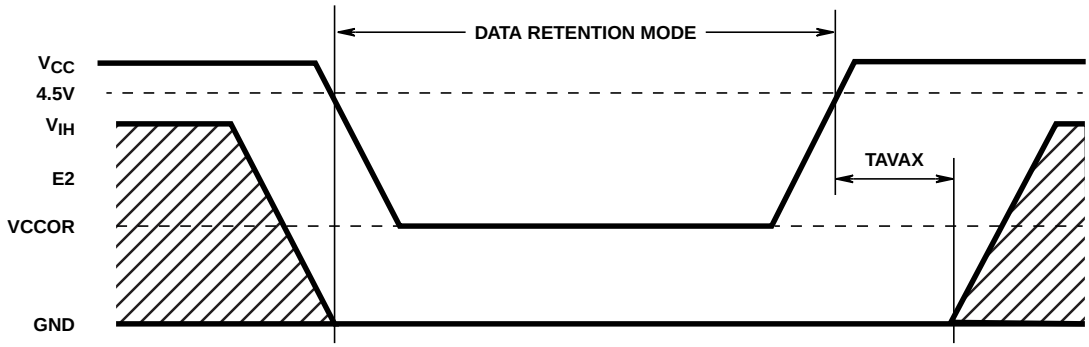


FIGURE 1. DATA RETENTION

Read Cycles

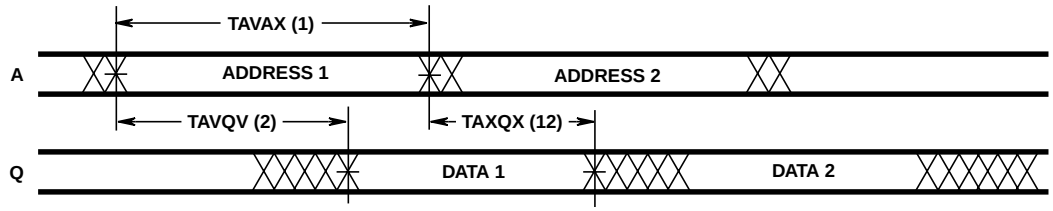


FIGURE 2. READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

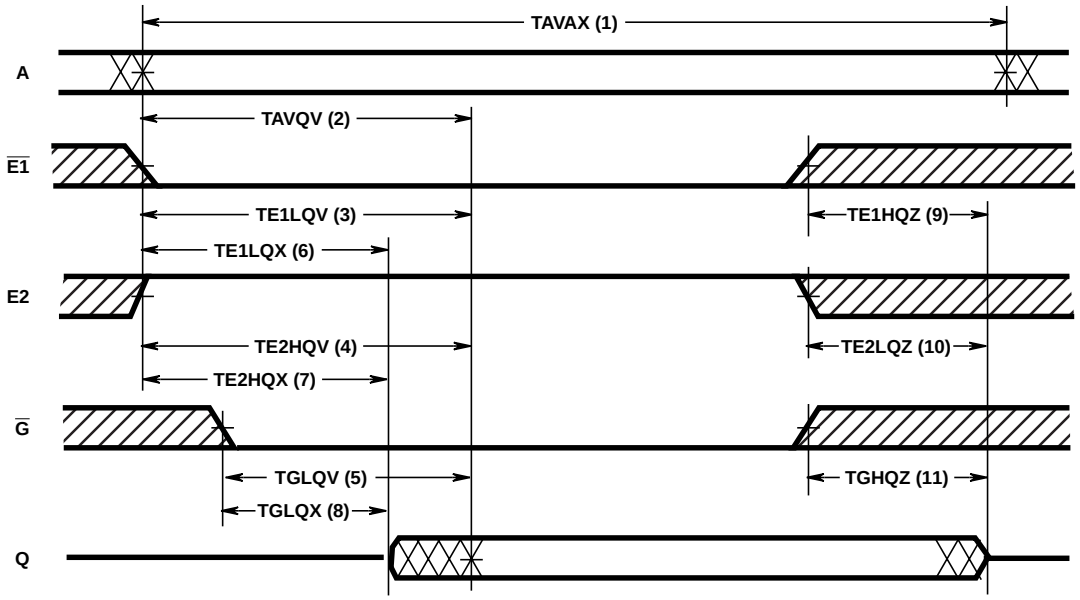


FIGURE 3. READ CYCLE II: $\overline{W}$ HIGH

Write Cycles

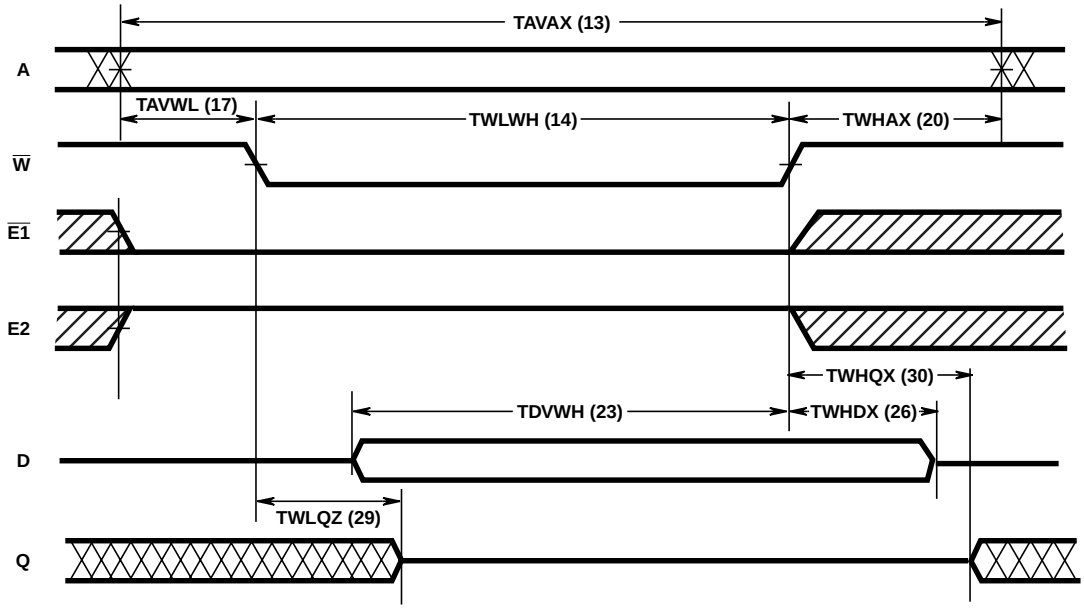


FIGURE 4. WRITE CYCLE I: LATE WRITE

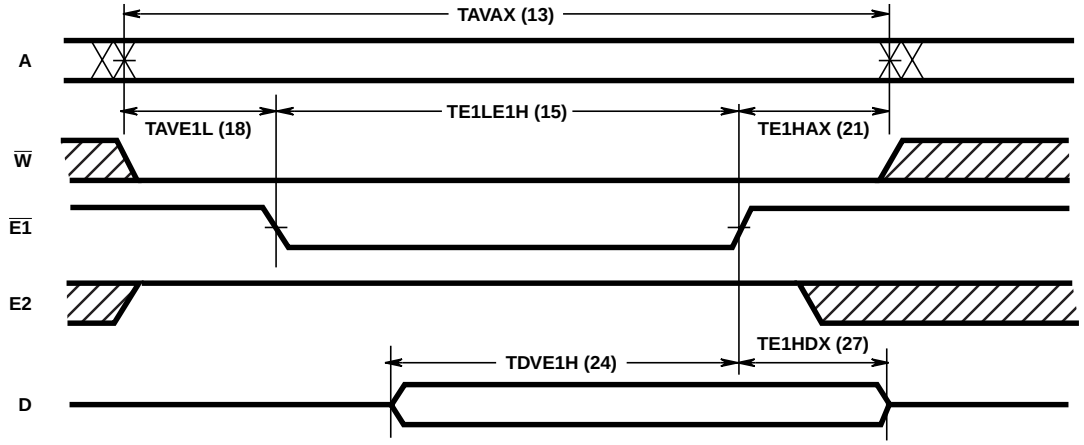


FIGURE 5. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

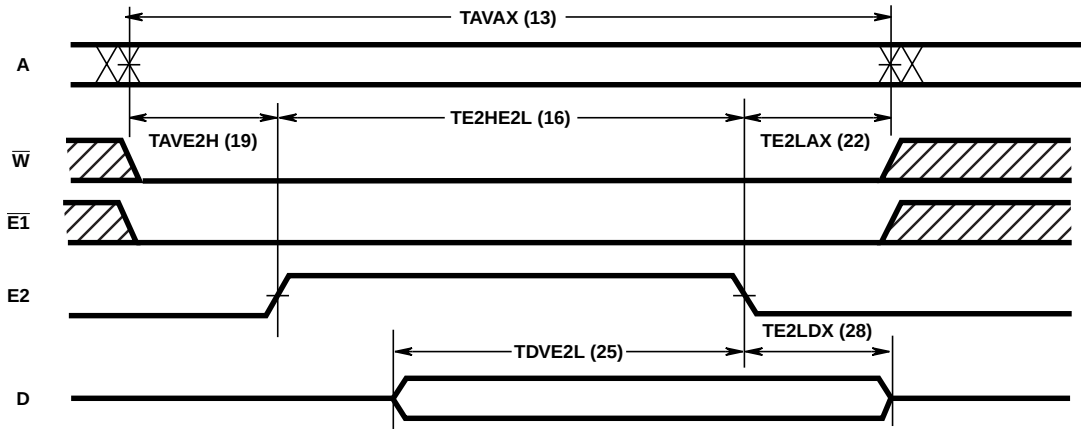


FIGURE 6. WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

Typical Performance Curve

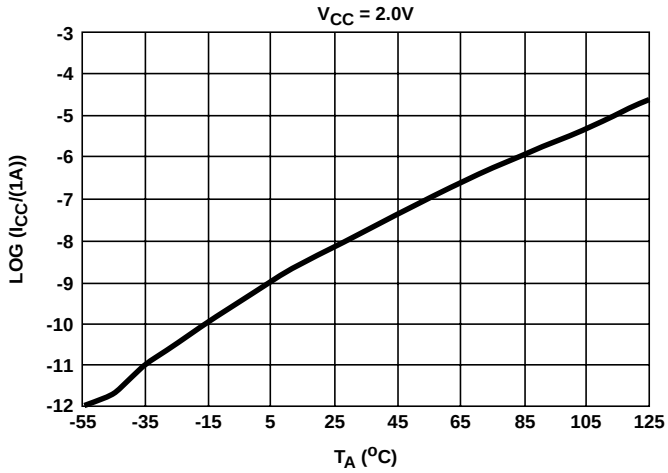


FIGURE 7. TYPICAL ICCDR vs T_A

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029