TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6K14

COLUMN ROW DRIVER LSI FOR DOT MATRIX GRAPHIC LCD

The TOSHIBA T6K14 is a driver for a small or medium scale dot matrix graphic LCD, especially for reflecting color STN LCD.
This LSI incorporate 65 row output, 128 column output and 65 × 128 × 2 bit bit-map display RAM. It has 4 gray-scale function.
The display RAM of this driver is a 2 port RAM so that the access from MPU is as same as general SRAM and has no waiting timing.
It include various power circuit, voltage regulator, voltage divider, Op-amp. contrast control and DC-DC converter (× 2, × 3, × 4, × 5).

Unit : mm

T6K14	LEAD PITCH	
	IN	OUT
(UBW, 5NS)	0.60	0.23

Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

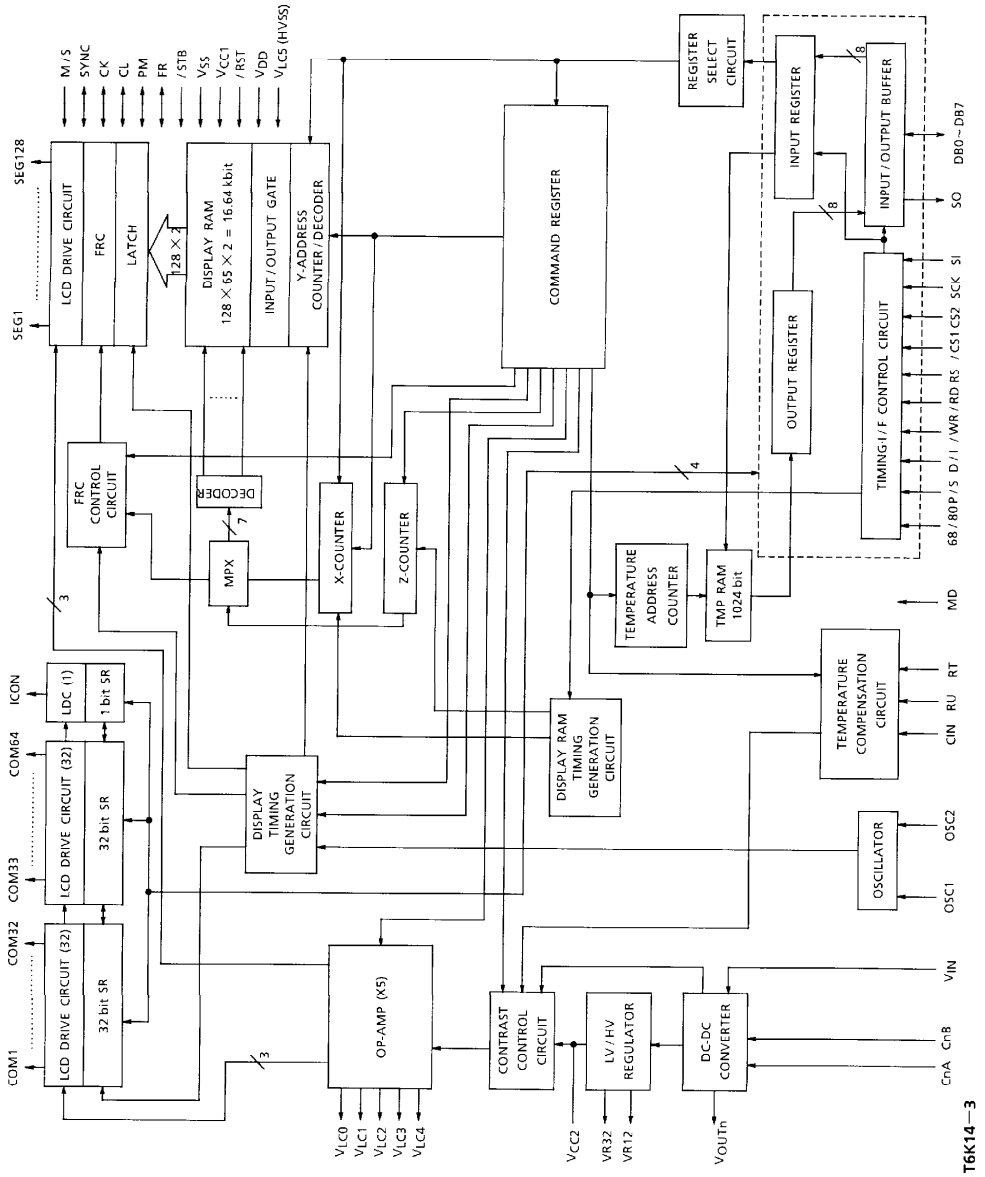
TCP (Tape Carrier Package)

FEATURES

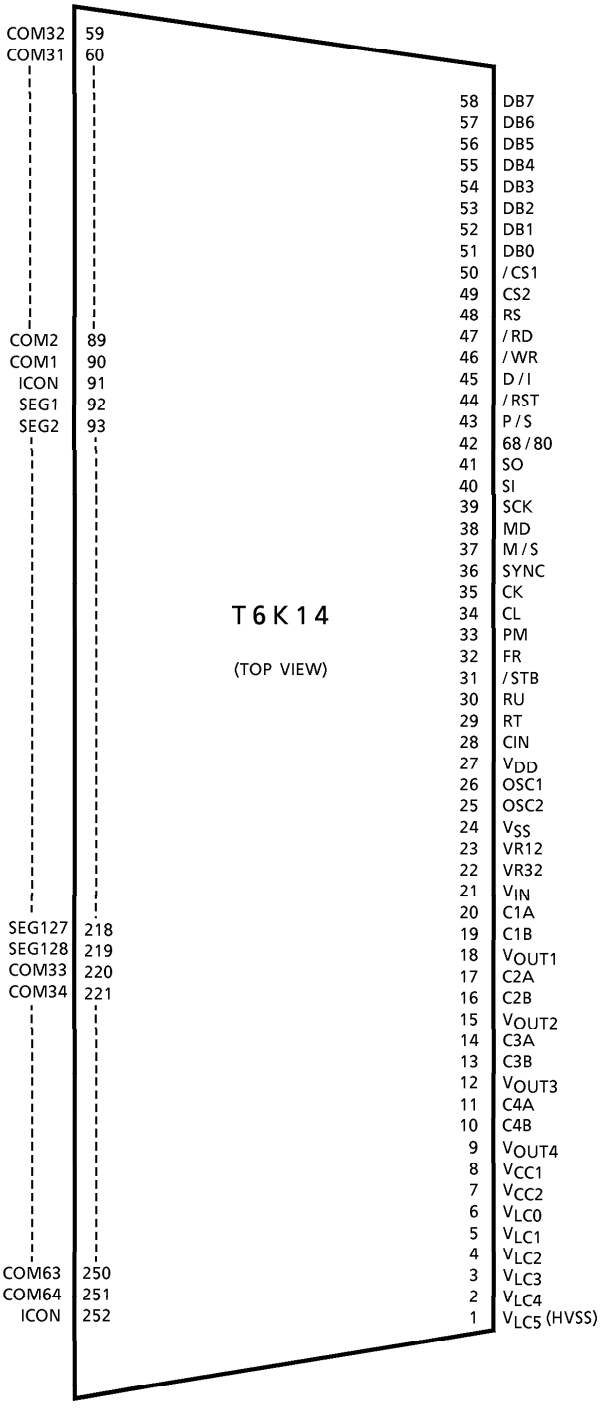
- LCD driver output : 64 row (common) + 128 column (segment) + 128 icons
- Built in display RAM : 65 × 128 × 2 = 16640 bit, 2 port RAM
- Gray scale : 4 gray scale selected
- Word length : 8 bit / word
- Duty cycle : 1 / 2 duty (power save mode)
  1 / 35, 1 / 49, 1 / 57, 1 / 65 duty selectable (normal display mode)

- Power management : Normal mode (Full display)
  Power save mode (Icon display)
  Stand by mode (Clock stop)
- Clock oscillator : CR oscillation
  Low frequency operation – 82 kHz oscillation for FR frequency 70 Hz (1 / 65 duty)
- Power circuit : Voltage regulator, Voltage divider, Voltage follower Op-amp.
  DC-DC converter (× 2, × 3, × 4, × 5), Temperature compensation circuit, Contrast control circuit.
- CPU interface : Interfacing with 68 / 80 series MPU and Serial Interface
- Logic operation voltage : V_{DD} = 2.4~3.3 V, V_{IN} = 2.7~3.3 V
- LCD operation voltage : $V_{CC1, 2}$ = 6.0~16.5 V, if case of used the voltage Regulator, V_{CC2} output voltage at 12.5 V or 11.0 V (Typ.) Ta = 25°C
- CMOS process
- Package : TCP
- Low power consumption: I_{SS} = 200 μA (Typ.)
  Condition : V_{DD} = 2.7 V, V_{IN} = 2.7 V, using the DC-DC converter (× 5), no data access, op-amp on, f_{osc} = 82 kHz (internal clock), no load, 1 / 65 duty, temperature conpensation circuit off.

BLOCK DIAGRAM



PIN CONFIGURATION



(*) : Above drawing describes pin configuration of the LSI Chip, it doesn't define the tape carrier package.

PIN FUNCTION (1)

PIN NAME	I/O	FUNCTION
SEG1~128	O	Column (segment) drive output
COM1~64	O	Row (common) driver output
ICON	O	Row (common) drive output of icon
DB0~7	I/O	Data bus
/CS1	I	Input for chip select signal Data write : Data write enable at the rising edge of /CS1. Data read : Data read out while /CS1 is in "L" level.
CS2	I	Input for chip select signal Data write : Data write enable at the falling edge of CS2. Data read : Data read out while CS2 is in "H" level.
D/I	I	Input for Data/Instruction select signal ● D/I = "H" → Indicates that the data of DB0 to DB7 is the display data. ● D/I = "L" → Indicates that the data of DB0 to DB7 is the instruction data.
/WR	I	Input for write enable signal ● /WR = "L" → State of select
/RD	I	Input for read enable signal ● /RD = "L" → State of select
RS	I	Input for register/mode select signal
P/S	I	Input for parallel interface/serial interface select signal ● P/S = "H" → Parallel interface is selected. SI and SCK must be connected to V_{DD} or V_{SS}. ● P/S = "L" → Serial interface is selected. DB0 to DB7, /WR and /RD must connected to V_{DD} or V_{SS}.
68/80	I	Input for 68 series MPU/80 series MPU select signal ● 68/80 = "H" → 68 series MPU selected ● 68/80 = "L" → 80 series MPU selected
SO	O	Output for serial data
SI	I	Input for serial data
SCK	I	Input for serial clock
/RST	I	Input for reset signal ● /RST = "L" → State of select

PIN FUNCTION (2)

PIN NAME	I/O	FUNCTION
/STB	I	Input for standby signal ● Usually connected to V_{DD} ● /STB = "L" → T6K14 is the state of standby. Column and row drive signal is V_{SS} level, and on-chip oscillator is stop.
OSC1, OSC2	I/O	When using a internal clock oscillator, connect a resistor between OSC1 and OSC2. When using a external clock, input the clock to OSC1.
V_{IN}	—	Power supply for DC-DC converter
CIN	I/O	Input for clock of temperature compensation
RU	—	Connect with standard resistor
RT	—	Connect with thermistor
C1A, C1B	—	Connect with capacitance for × 2 mode
V_{OUT1}	—	DC-DC converter output terminal (×2 level)
C2A, C2B	—	Connect with capacitance for × 3 mode
V_{OUT2}	—	DC-DC converter output terminal (× 3 level)
C3A, C3B	—	Connect with capacitance for × 4 mode
V_{OUT3}	—	DC-DC converter output terminal (× 4 level)
C4A, C4B	—	Connect with capacitance for × 5 mode
V_{OUT4}	—	DC-DC converter output terminal (× 5 level)
VR12	—	LV regulator monitor terminal (Note)
VR32	—	LV regulator monitor terminal (Note)
V_{CC1}	—	Power supply for LCD driver circuit
V_{CC2}	—	Power supply for HV regulator monitor terminal (Note)
V_{LC0}~V_{LC5}	—	Power supply for LCD driver circuit V_{LC5} terminal is connect to V_{SS}. (Note)
V_{SS}, V_{DD}	—	Power supply for logic circuit. Ground : Reference

(Note) : Connect the capacitance between this terminal and V_{SS}.

PIN FUNCTION (3)

PIN NAME	I / O	FUNCTION
MD	I	Mode detect pin for Status Read
M / S	I	Input for master / slave selects ● M / S = "H" → T6K14 is master chip ● M / S = "L" → T6K14 is slave chip
CL	I / O	Input / Output for shift clock pulse ● Master mode (M / S = "H") → output ● Slave mode (M / S = "L") → input
PM	I / O	Input / Output for frame signal ● Master mode (M / S = "H") → output ● Slave mode (M / S = "L") → input
FR	I / O	Input / Output for display synchronous signal ● Master mode (M / S = "H") → output ● Slave mode (M / S = "L") → input
SYNC	I / O	Input / Output for grayscale signal data ● Master mode (M / S = "H") → output ● Slave mode (M / S = "L") → input
CK	I / O	Input / Output for grayscale signal data ● Master mode (M / S = "H") → output ● Slave mode (M / S = "L") → input

PIN FUNCTION (4)

PS	68 / 80	INTERFACE TYPE	/ CS1	CS2	D / I	RS	/ WR	/ RD	SO	SI	SCK	DB0 to DB7
H	L	80 series MPU (/ CS1)	/ CS1	H	A0	A1	/ WR	/ RD	Open	L / H	L / H	DB0 to DB7
		80 series MPU (CS2)	L	CS2	A0	A1	/ WR	/ RD	Open	L / H	L / H	DB0 to DB7
	H	68 series MPU	L	H	A0	A1	R / W	E	Open	L / H	L / H	DB0 to DB7
L	L / H	Serial interface	L	H	L / H	L / H	L / H	L / H	SO	SI	SCK	L / H

FUNCTION OF EACH BLOCK

- Interface logic

  The T6K14 can be operated with 80 series MPUs or 68 series MPUs and Serial Interface.
  Fig.1 shows an example of interface. For ditails, please refer to the example interface part of application circuit.

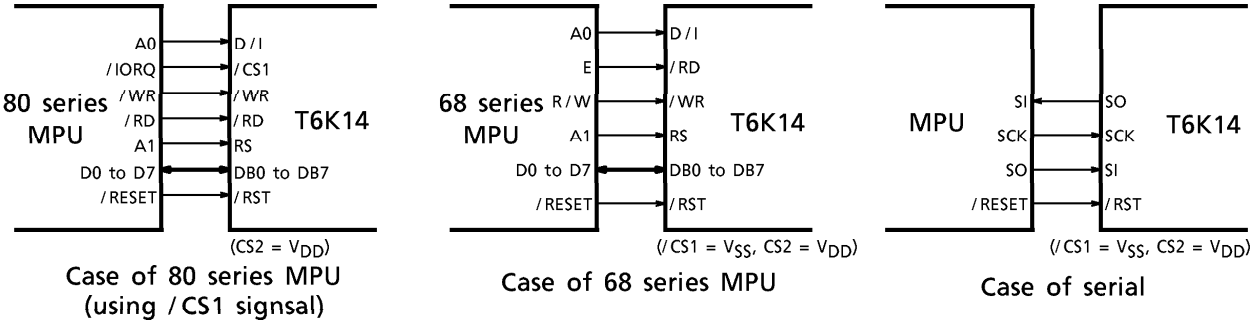


Fig.1

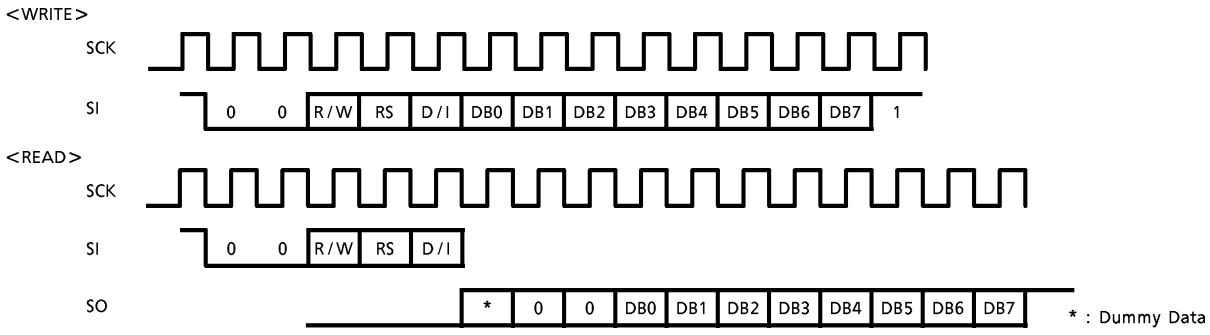


Fig.2

- Input register
  The register stores 8bit data from MPU. D/I signal discriminate between command data and display data.
- X-address counter
  X-address counter is 64-Up/Down counter. It holds the row address for the display RAM. Then it is selected by the command, writing to or reading the data of display RAM causes the X-address to automatically increment or decrement.
- Y (Page) -address counter
  The Y (Page) -address counter is 32-Up/Down counter. It holds the column address for the display RAM. This counter is selected by the command. Writing to or reading the display RAM causes the Y-address to automatically increment or decrement.
- Z-address counter
  The Z-address counter is 64-Up counter that provide the display RAM data for the LCD drive circuit. The data stored in Z-Address Register is send to Z-Address counter as Z start address.
  For instance, when Z start address is 16, the counter increment like this : 16, 17, 18···, 62, 63, 0, 1, 2···14, 15, 16. Therefore, the display start line is 16-line of the display RAM.

- Up / Down register

  The 1bit data stored in this register selects Up or Down mode of X and Y (Page) -address counter.

- Counter select register

  The 1bit data stored in this register selects X-address counter or Y (Page) -address counter.

- Display ON / OFF register

  This 1bit register holds the display ON or OFF state. In the OFF state, the output data from the display RAM is not selected. In the On state, the display data appears according to the display RAM data. The display ON or OFF state does not affect the data of display RAM.

- Z-address register

  This 6bit register holds the data that indicates the display start line.

- Oscillator

  The T6K14 has an on-chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2. When using external clock, input the clock to OSC1 and open OSC2, as shown in Fig.3.

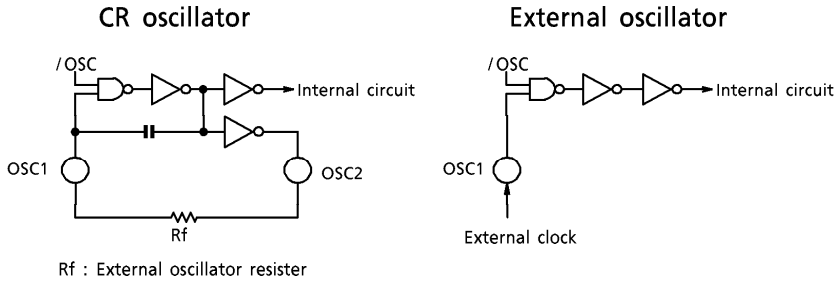


Fig.3

- Timing generation circuit

  The circuit divides the signals from the oscillator and generates display timing signals and operating clock.

- Shift-register

  The T6K14 has two 32bit shift-register and shift register of ICON. These shift-register construct 65 bits shift-register.

- Latch circuit

  This latch circuit latches the data from the display RAM.

- Column driver circuit

  Column driver circuit consists of 128 driver circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the display data transferred from the latch circuit. Details of column driver circuit are shown in Fig.4.

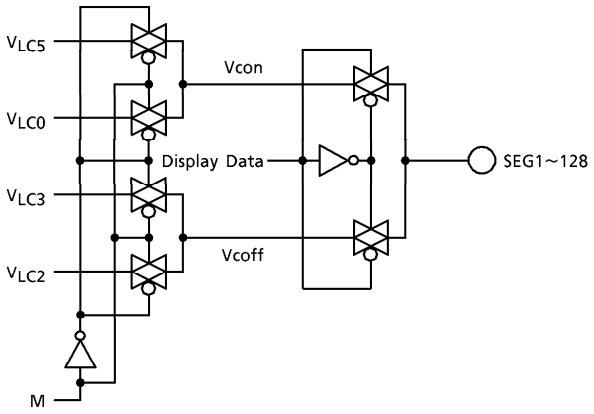


Fig.4

- Row driver circuit

  Row driver circuit consists of 65 drive circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the data from the sift register. Details of row driver circuit are shown in Fig.5.

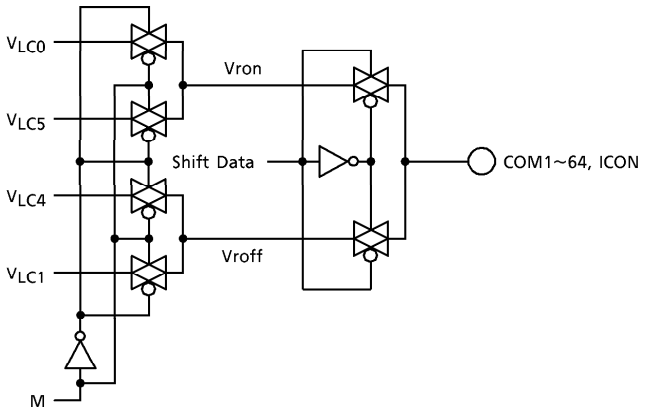


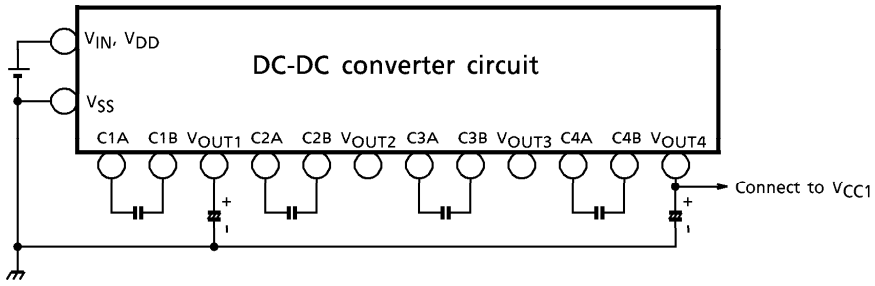
Fig.5

- DC-DC converter

The T6K14 built in DC-DC converter circuit 2 / 3 / 4 / 5 time.
V_{outn} = 0 (V_{SS} level) is at the time of / RST = "L" or / STB = "L".
The capacitor for DC-DC converter and the capacitor for DC-DC level maintenance usually use about 1.0 μF. Since the power supply V_{IN} terminal for DC-DC converter circuit can input voltage usually higher than a digital system power supply V_{DD} terminal, it can generate required LCD voltage in a DC-DC converter. However, since the maximum of LCD operation voltage is 16.5 V (max.) be careful about the relation of the voltage conditions (V_{IN} voltage) and the number of the DC-DC steps which are used in a DC-DC converter so that the DC-DC converted voltage (voltage value outputted from V_{out}) does not exceed 16.5 V.

Note 1 : Power supply voltage ..... 3.3 V ≧ V_{IN} ≧ 2.7 V, V_{IN} ≧ V_{DD}
Note 2 : LCD voltage ..... 16.5 V ≧ V_{IN} × n
(n : number of DC-DC step)

ex) Using the × 5 mode



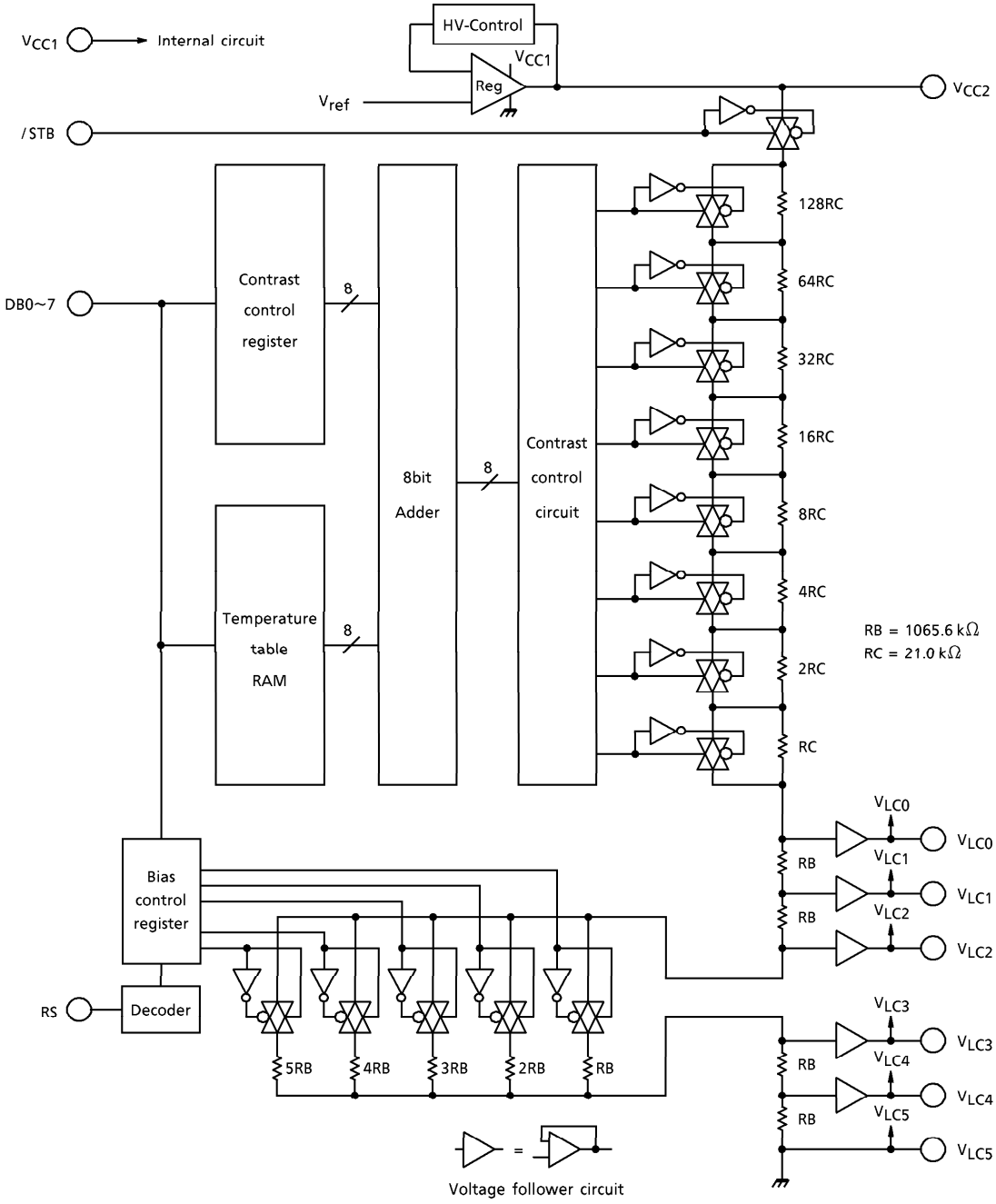
About terminal processing

CONDITION	C1A, C1B	V_{OUT1}	C2A, C2B	V_{OUT2}	C3A, C3B	V_{OUT3}	C4A, C4B	V_{OUT4}
× 2 mode	○	○	Open	Open	Open	Open	Open	Open
× 3 mode	○	○	○	○	Open	Open	Open	Open
× 4 mode	○	○	○	Open	○	○	Open	Open
× 5 mode	○	○	○	Open	○	Open	○	○
None	Open	Open	Open	Open	Open	Open	Open	Open

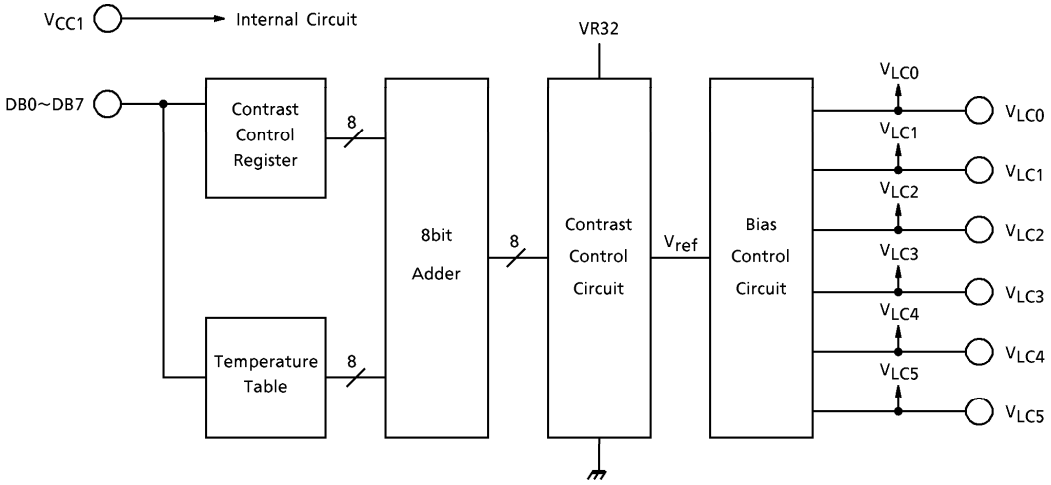
(Note) : ○ = Connect the capacitance.
(Note) : The voltage outputted from DC-DC converter changes with voltage condition, temperature environment, substrate environment, etc.

- Voltage driver resistor, contrast control circuit (Normal mode)

  The T6K14 has on-chip resistors to divide bias voltage with OP-Amp., and a contrast control circuit. The voltage bias is changed by instruction command. And one of four bias is selected.



- Contrast control circuit (Power Save Mode)

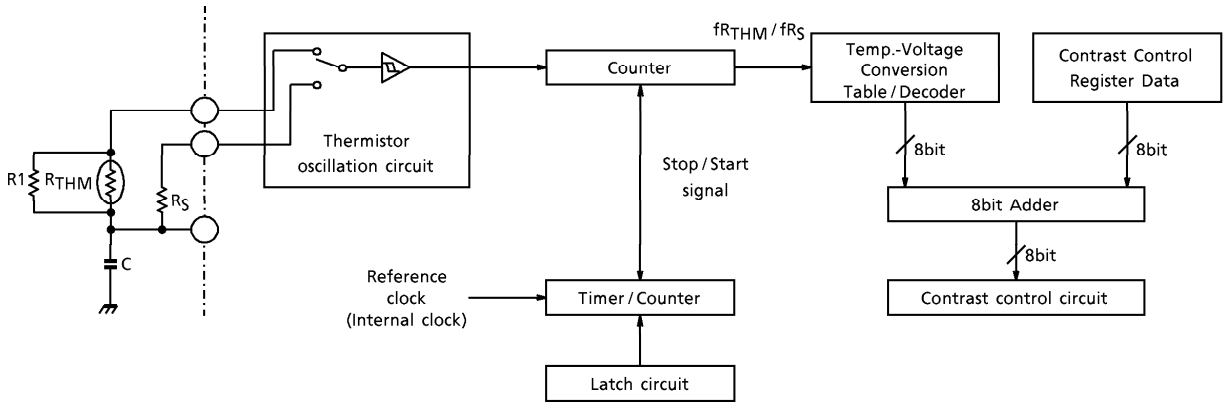


Contrast control output voltage (VLC0) (TYPICAL VALUE)

CONDITION	VR32 [V]	V_{LC0} (MIN.) [V]	V_{LC0} (MAX.) [V]	CONTRAST STEP [mV]	BIAS
Power Save	3.2	2.2	5.0	11.0	1 / 12

- Temperature compensation circuit

  The T6K14 has the temperature compensation circuit.



R1 : 91 kΩ
R_S : 47 kΩ
R_{THM} : 100 kΩ Thermistor
Semitec Type 104HT-1P
C : 1000 pF

While this temperature compensation circuit detects temperature, it controls automatically built-in contrast control. And, original contrast control suitable for all LCD material can be created by writing data in RAM for temperature compensation circuit (TEMP-RAM). Please refer to description of a function about the usage.

COMMAND DEFINITION

COMMAND	REG. No.	D / I	RS	/ WR	/ RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Register set (REG)	—	0	0	0	1	0	0	0	Register (0~31)				
Status read (STRD)	—	0	0	1	0	MD	*	TMP	HVR	N / F	DP	Y / X	U / D
Data mode (DMD)	R0	0	1	0	1	0	0	0	0	0	D / TM	Y / X	U / D
Display mode (DPE)	R1	0	1	0	1	0	CDR	SDR	0	0	0	N / F	DP
Power mode (PWE)	R2	0	1	0	1	×4 / ×5	0	0	0	0	VR	OP	DC
Duty / Bias Select (DTE)	R3	0	1	0	1	Bias (5~9)				0	0	Duty (0~3)	
Oscillation (OSE)	R4	0	1	0	1	0	0	0	0	0	0	0	OSC
X, Y-address (SXYE)	R5	0	1	0	1	1	F / N	X-Address (0~63)					
						0	0	0	Y-Address (0~31)				
Z-address (SZE)	R6	0	1	0	1	0	0	Z-Address (0~63)					
Contrast control (SCE)	R7	0	1	0	1	Contrast Control (0~255)							
TEMP mode (TMPM)	R8	0	1	0	1	0	0	0	0	TMOF	0	time (0~3)	
TEMP-RAM address (TMPA)	R9	0	1	0	1	0	TEMP-RAM address (0~127)						
FRS control mode (FRSC)	R10	0	1	0	1	0	0	FR control (0~63)					
Grayscale (1) (GR1)	R11	0	1	0	1	Grayscale patturn data (1)							
Normal display pattern	R12	0	1	0	1	Normal display data = "00" ··· 16 bit							
Grayscale (2) (GR2)	R13	0	1	0	1	Grayscale patturn data (2)							
Normal display pattern	R14	0	1	0	1	Normal display data = "01" ··· 16 bit							
Grayscale (3) (GR3)	R15	0	1	0	1	Grayscale patturn data (3)							
Normal display pattern	R16	0	1	0	1	Normal display data = "10" ··· 16 bit							
Grayscale (4) (GR4)	R17	0	1	0	1	Grayscale patturn data (4)							
Normal display pattern	R18	0	1	0	1	Normal display data = "11" ··· 16 bit							
Grayscale (5) (GR5) Power save display pattern	R19	0	1	0	1	Grayscale patturn data (5)							
	R20	0	1	0	1	Power save display data = "00" ··· 16 bit							
Grayscale (6) (GR6) Power save display pattern	R21	0	1	0	1	Grayscale patturn data (6)							
	R22	0	1	0	1	Power save display data = "01" ··· 16 bit							
Grayscale (7) (GR7) Power save display pattern	R23	0	1	0	1	Grayscale patturn data (7)							
	R24	0	1	0	1	Power save display data = "10" ··· 16 bit							
Grayscale (8) (GR8) Power save display pattern	R25	0	1	0	1	Grayscale patturn data (8)							
	R26	0	1	0	1	Power save display data = "11" ··· 16 bit							
TEMP-RAM address read	R27	0	1	1	0	*	TEMP-RAM address data (7 bit)						
Test mode	R28~31	0	1	0	1	Please do not using this register							
Data write (DAWR)	—	1	1	0	1	Write data							
Data read (DARD)	—	1	1	1	0	Read data							

- Register set

  Identify register number
  R0 (00H)~R31 (1FH)
  Note : T6K14 is using register between R28 to R31 for test mode. Please do not using this registers.

- R0 : Data mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	0	0	D/TM	Y/X	U/D

  D/TM : Select display RAM address counter / TMP RAM address counter
  D/TM = 1 : Display RAM counter D/TM = 0 : TMP RAM counter

  Y/X : Select X/Y-counter
  Y/X = 1 : Y-counter selected Y/X = 0 : X-counter selected

  U/D : Select counter Up/Down mode
  U/D = 1 : Up mode U/D = 0 : Down mode

- R1 : Display mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	CDR	SDR	0	0	0	N/F	DP

  CDR : Select common data how
  CDR = 1 : COM1 → COM64 → ICON CDR = 0 : COM64 → COM1 → ICON

  SDR : Select segment data direction
  See page 23

  N/F : Select display
  N/F = 1 : Normal display N/F = 0 : Flag display only (Power save mode)

  DP : Display ON/OFF
  DP = 1 : Display ON DP = 0 : Display OFF

- R2 : Power management

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	X4/X5	0	0	0	0	VR	OP	DC

X4/X5 :

X4/X5 = 0 : LCD voltage regulator output voltage is 12.5 V typ. (at Ta = 25°C)

X4/X5 = 1 : LCD voltage regulator output voltage is 11.0 V typ. (at Ta = 25°C)

VR : LCD voltage regulator (HVR)

VR = 1 : Voltage regulator ON VR = 0 : Voltage regulator OFF

OP : Op-Amp

OP = 1 : Op-Amp ON OP = 0 : Op-Amp OFF

DC : DC-DC converter

DC = 1 : DC-DC converter ON DC = 0 : DC-DC converter OFF

(Note) : Refer to the description of a function for the combination of a power supply setup.

- R3 : Bias/Duty select

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Bias				0	0	Duty	

Bias select :

DB7	DB6	DB5	DB4	
1	0	0	1	1/9 bias
1	0	0	0	1/8 bias
0	1	1	1	1/7 bias
0	1	1	0	1/6 bias
0	1	0	1	1/5 bias

Duty select :

DB1	DB0	
1	1	1/65 duty
1	0	1/57 duty
0	1	1/49 duty
0	0	1/35 duty

- R4 : Oscillation control

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	0	0	0	0	OSC

OSC : Oscillation ON/OFF

OSC = 1 : Oscillator ON OSC = 0 : Oscillator OFF

- R5 : X-address, Y-address set

(1) X-address set

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	1	F/N	X-Address (0~63)					

F/N = 0 : Set display RAM address from 0 to 63
F/N = 1 : Set flag RAM (The data from DB0 to DB5 is ignored)

(2) Y-address set

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	Y-Address (0~31)				

- R6 : Z-address set

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	Z-Address (0~63)					

The command set the starting line of display RAM.
Since correspondence of RAM for a display and Z-address set changes when using duty setup except 1/65 duty, please be careful.
Please refer to description of a function for details.

- R7 : Contrast control

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Contrast Control (0~255)							

This command set contrast.
It becomes the maximum contrast when data is 255, and it becomes the minimum contrast when data is 0.
When a temperature compensation circuit is used, data for a contrast control circuit are changed to the sum of R7 register 8-bit data and TEMP-RAM 8-bit data. Therefore, the contrast is controlled.

- R8 : TMP mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	0	TMOF	0	TIME	

TMOP : Temperature compensation ON/OFF
TMOF = 1 : ON TMOF = 0 : OFF (Note 1)

DB1	DB0	
1	1	4 sec cycle
1	0	2 sec cycle
0	1	1 sec cycle
0	0	No measurement

(Note 1) : Data on the output bus of the temperature table RAM are fixed on "L" data.
Therefore, data on the contrast control register are inputted to contrast control circuit.

- R9 : TEMP-RAM address

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	TEMP-RAM address (0~127)						

This command set temperature compensation address.
In case of using this command, counter up mode only.

- R10 : FRS control

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	FR control (0~63)					

This command sets the number of the row lines for polarity change.
The setting of FRS corresponds to the row line number, see following table.

FRS	FRAME
0	In case 1/x duty is selected by R3, FR signal inverts on every x line. (Note)
n	FR signal inverts on every (n + 1) line.

(Note) : In case FRS = 0 ;
FR signal inverts synchronously with the earlier edge of COM1.
In case FRS ≠ 0 (1~63) ;
FR signal inverts synchronously with the edge of COMm. (m = 1 to 64, or ICON)
"m" shows a COM line right after the instruction practice.

- R11~R26 : Grayscale data

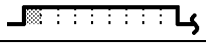
This register have the PWM (Pulse Width Modulation) and FRC (Frame Rate Control) control data. PWM chooses one of 10 kinds and assigns data of PWM to four frames. Therefore, it will choose from 40 kinds of levels in all.

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	1st FR data				0th FR data			
					3rd FR data				2nd FR data			

This register is constituted from "0th FR data" by 4 bits of "3rd FR data", and inputs PWM data into four FR data. That is, it becomes data of one color (one grayscale level) by 4 frames.

DISPLAY MODE	DISPLAY RAM DATA		REGISTER No.	GRAYSCALE DATA
Normal Display Mode	0	0	R11, 12	4 bit × 4
	0	1	R13, 14	4 bit × 4
	1	0	R15, 16	4 bit × 4
	1	1	R17, 18	4 bit × 4
Power Save Mode	0	0	R19, 20	4 bit × 4
	0	1	R21, 22	4 bit × 4
	1	0	R23, 24	4 bit × 4
	1	1	R25, 26	4 bit × 4

- Data of PWM (Pulse Width Modulation)

FR DATA	HEX	PWM (ON WIDTH)	NOTE
0000	0	0 (0/9)	
0001	1	1/9	
0010	2	2/9	
0011	3	3/9	
0100	4	4/9	
0101	5	5/9	
0110	6	6/9	
0111	7	7/9	
1000	8	8/9	
1001	9	1 (9/9)	
1010 ∫ 1111	A ∫ F	0 (0/9)	(Note)

(*) : The phase of PWM turn over by the even/odd of the output pin.

(Note) : This area is selected to off level (0/9 level)

- R27 : TEMP-RAM address read

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	1	0	*	d	d	d	d	d	d	d

This register store the data of temperature compensation circuit counting values. (Read out only). This read out data corresponds by temperature and 1 to 1.

- R28~31 : Test mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Test mode							

Please don't access this register.

- Status read

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	MD	*	TMP	HVR	N/F	DP	Y/X	V/D

MD : When input the V_{DD} level from MD terminal, MD (DB7) = 1.
When input the V_{SS} level from MD terminal, MD (DB7) = 0.

TMP : When TMP = 1, the temperature compensation circuit is ON.
When TMP = 0, the temperature compensation circuit is OFF.

HVR : When HVR = 1, HV-Regulator mode is X4.
When HVR = 0, HV-Regulator mode is X5.

N/F : When N/F = 1, Display mode is Normal display mode.
When N/F = 0, Display mode is FLAG display only mode. (Power save mode)

DP : When DP = 1, Display is ON.
When DP = 0, Display is OFF.

Y/X : When Y/X = 1, Y-counter is selected.
When Y/X = 0, X-counter is selected.

U/D : When U/D = 1, X and Y counters are in up mode.
When U/D = 0, X and Y counters are in down mode.

- Write / read display data (DAWR / DARD)

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Code	1	1	0	1	d	d	d	d	d	d	d	d	DAWR
	1	1	1	0	d	d	d	d	d	d	d	d	DARD

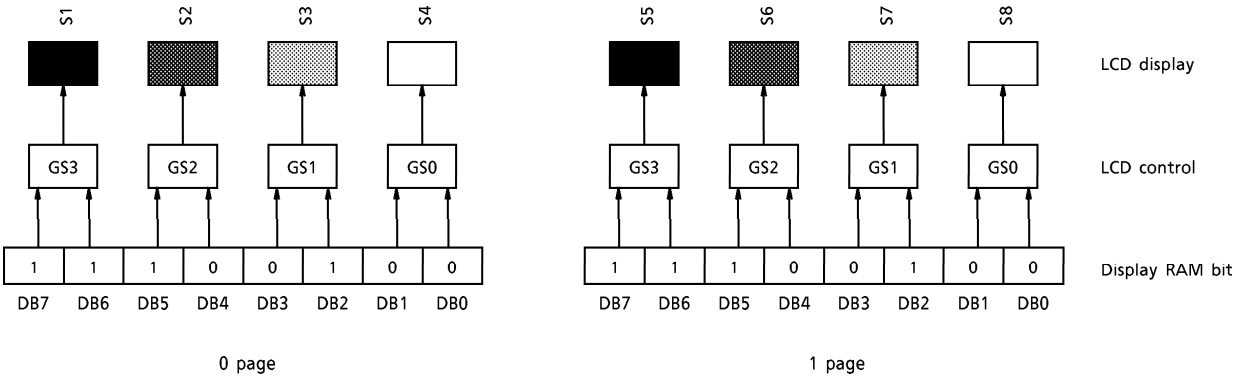
DAWR : Display data write
DARD : Display data read

The command DAWR writes display data in the address specified before hand.
Moreover, the command DARD reads display data stored in the specified address.

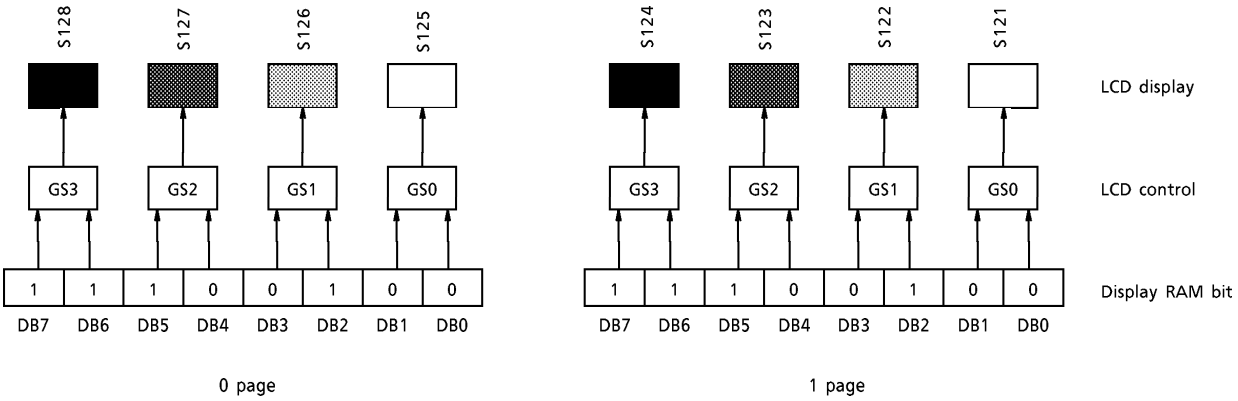
FUNCTION DESCRIPTION

- Display data bit

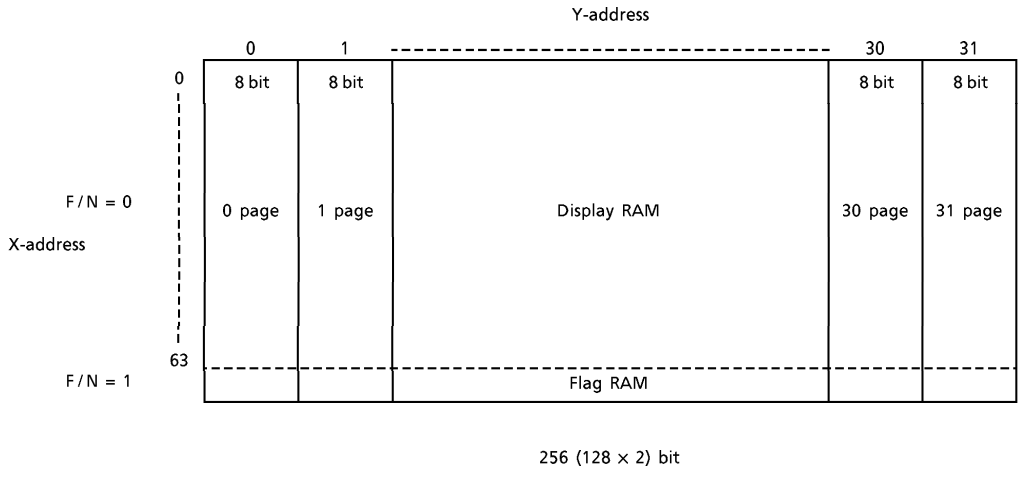
SDR = 1



SDR = 0



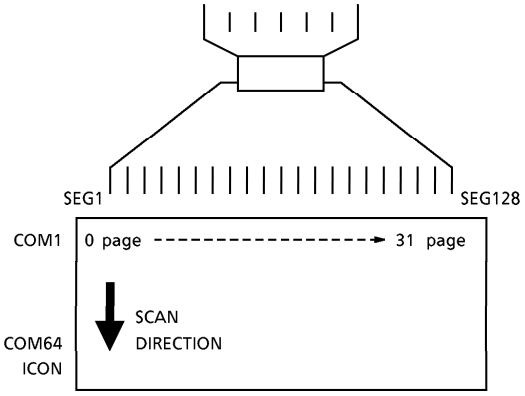
- Display mode



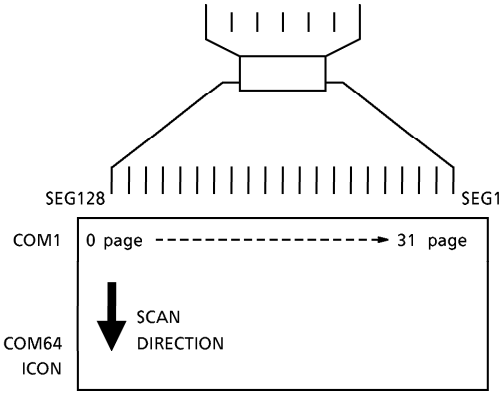
256 (128 × 2) bit

- RAM map and CDR, SDR relation

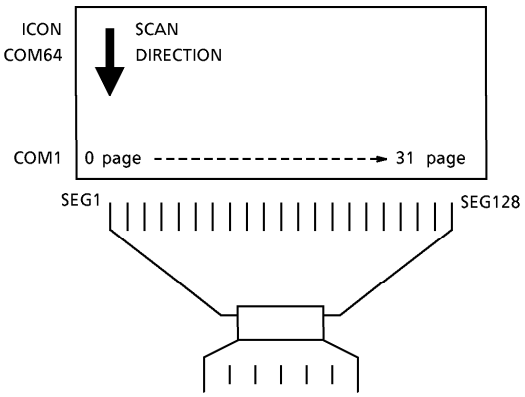
(1) CDR = 1, SDR = 1



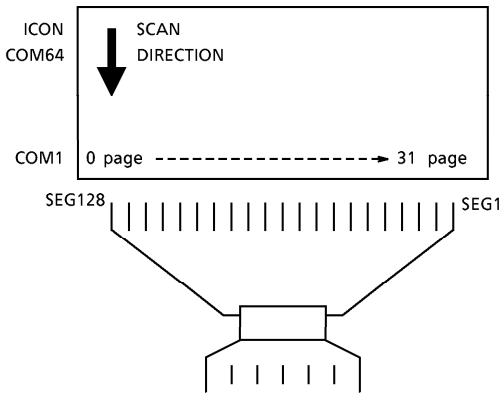
(2) CDR = 1, SDR = 0



(3) CDR = 0, SDR = 1



(4) CDR = 0, SDR = 0



- Reset function

  When /RST = "L", reset function is executed and following instruction (resister) are executed.

COMMAND	REG No.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Data mode	R0	*	*	*	*	*	1	1	1
Display mode	R1	*	1	1	*	*	*	1	0
Power mode	R2	1	*	*	*	*	0	0	0
Duty / Bias	R3	1	0	0	1	*	*	1	1
Oscillation	R4	*	*	*	*	*	*	*	1
X, Y-address	R5	0	0	0	0	0	0	0	0
Z-address	R6	*	*	0	0	0	0	0	0
Contrast control	R7	0	0	0	0	0	0	0	0
TEMP mode	R8	*	*	*	*	0	*	0	0
TEMP-RAM address	R9	*	0	0	0	0	0	0	0
FRS control mode	R10	*	*	0	0	0	0	0	0
Gray scale	R11~R27	0	0	0	0	0	0	0	0

- Standby function

  When /STB = "L", the T6K14 is in standby state. The internal oscillation is stopped, power consumption is reduced, and power supply for LCD (V_{LC0}~V_{LC5}) become V_{SS}.

● Expansion function

The T6K14 has expansion function. When using this function, the T6K14 (2 chip) can drive 256 × 64 + icon dots LCD panel (maximum) or 128 × 128 + icon dots LCD panel (Maximum).
Next table shows the selectable function by using M / S pins.

M / S	
H	L
● One chip mode Disable expansion mode ● Two chips mode (Master chip) Timing signal and power voltage supply to Slave chip.	● Two chips mode (Slave chip) Timing signal and power voltage are supplied from Master chip.

Fig.6 and Fig.7 illustrate the application example of disable expansion mode and enable expansion mode.
In enable expansion mode (Tow chip mode)
As shown in Fig.7-1, Fig.7-2 Master chip supplies LCD drive signals and power voltage to slave chip. (The oscillator, the timing circuits, Op-Amp, and Contrast control circuit are disable.)

(1) Disable expansion mode

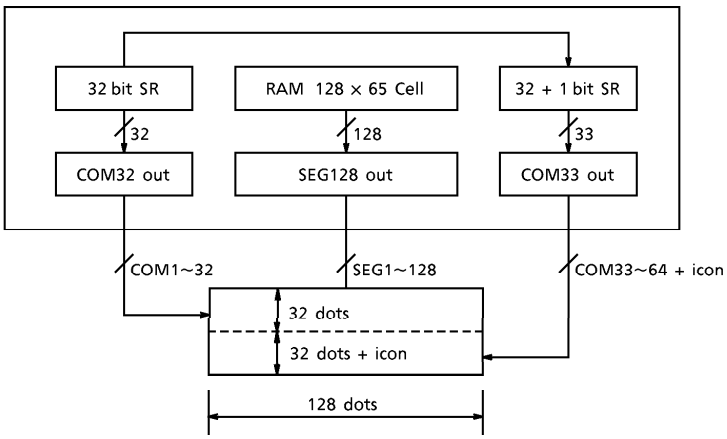


Fig.6

(2) Enable expansion mode

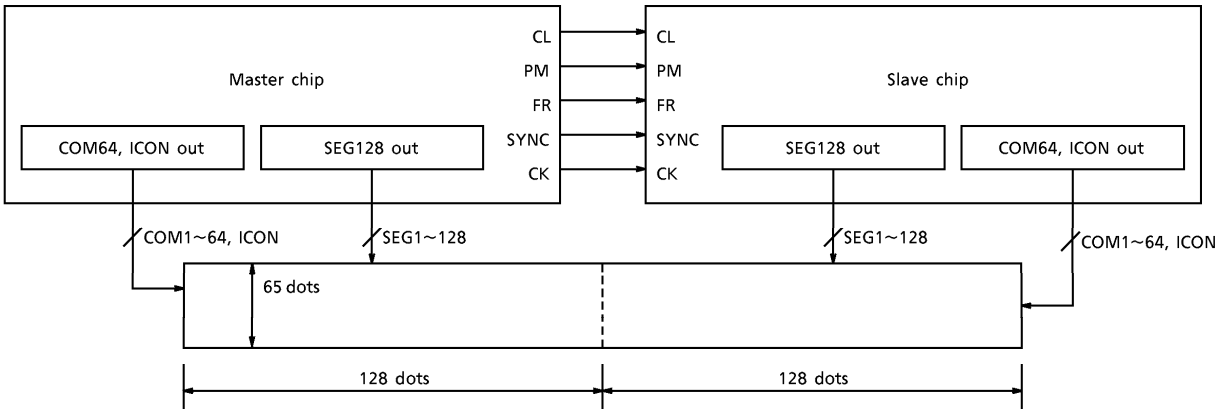


Fig.7-1

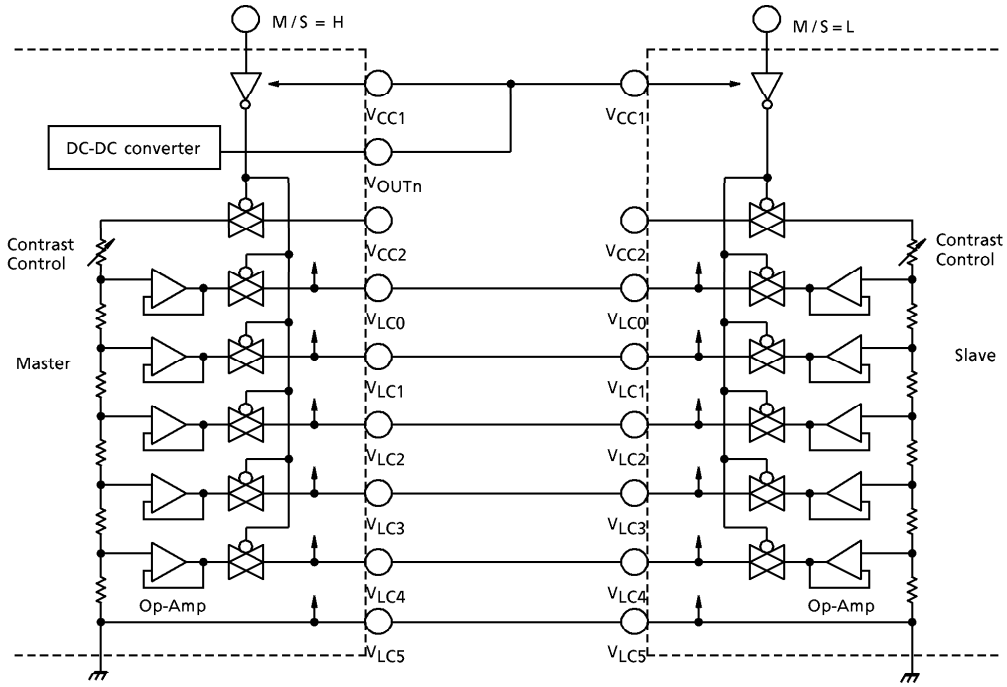


Fig.7-2

● X-address counter and Y (Page) -address counter

Fig.8-1 shows a sample of operating procedure for the X-address counter.
After reset is executed, X-address becomes X-address = 0, then select X-counter / Up mode. Next set the X-address to 62 by commanding SXYE (R13).
After data has been written to or read, the X-address is automatically incremented by one.
After X-counter / Down mode has been selected and data has been written to or read, the X-address is automatically decremented by one.
When the X-counter is selected, Y-counter does not count up or down.
And flag-counter does not count up or down too.

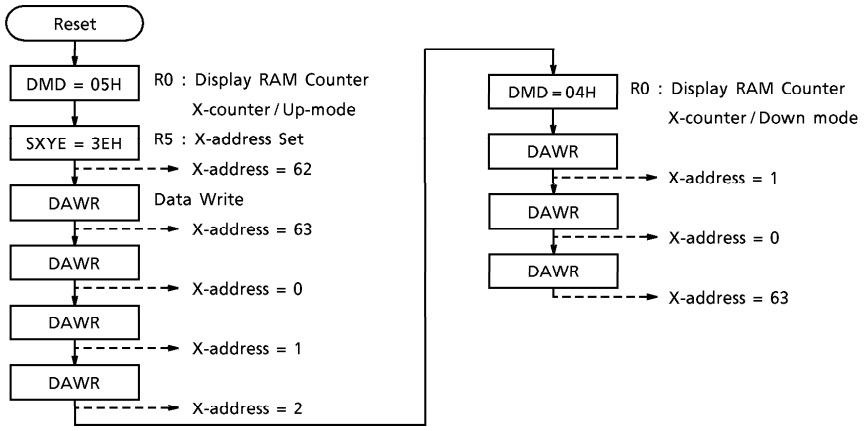


Fig.8-1

Fig.8-2 shows a sample operating procedure for the Y-address counter.
After reset is executed, Y (Page) -address becomes Y-address = 0, then select Y (Page) -counter / Up-mode. After data has been written to or read, the Y (Page) -address counter is automatically incremented by one.
After Y (Page) -counter / Down mode has been selected and data has been written to or read, the Y (Page) -address is automatically decremented by one.
When the Y (Page) -counter is selected, X-counter doesn't count up or down.

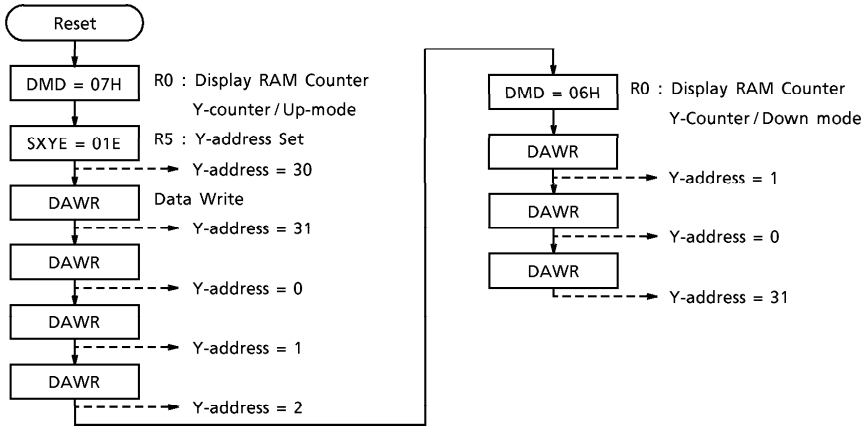
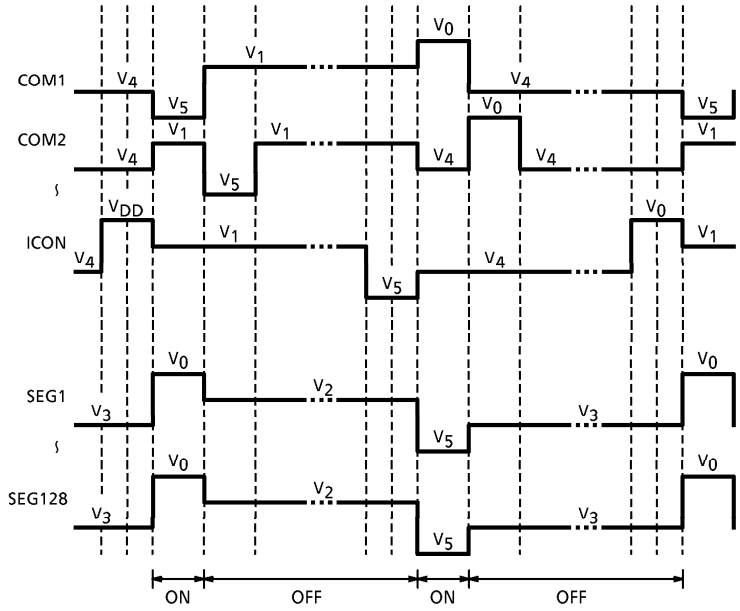


Fig.8-2

- **LCD DRIVER WAVEFORM** (Case of normal mode)



LCD driver timing chart (1/65 duty)

MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD}, V_{IN} (Note 1)	−0.3~7.0	V
Supply Voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{CC1}, V_{CC2}	V_{SS} + 18.0~V_{SS} − 0.3	V
Input Voltage	V_{inp} (Note 1, 2)	−0.3~V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~125	°C

(Note 1) : Referred to V_{SS} = 0 V
(Note 2) : Applied data bus terminals and Input terminals expect V_{CC1}, V_{CC2}, V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (1)

(Test condition : If not specified, V_{SS} = 0 V, V_{DD} = 2.4~3.3 V, V_{IN} = 2.7~3.3 V, V_{LC0} = 0 V, Ta = 25°C)

ITEM		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Operating Supply (1)		V_{DD}	—	—	2.4	—	3.3	V	V_{DD}
Operating Supply (2)		V_{IN}	—	—	2.7	—	3.3	V	V_{IN}
Operating Supply (3)		V_{LC0} $V_{CC1, 2}$	—	—	6.0 – V_{SS}	—	16.5 – V_{SS}	V	V_{LC0}, V_{CC1}, V_{CC2}
Input Level	"H" Level	V_{IH}	—	—	0.8V_{DD}	—	V_{DD}	V	DB0~DB7, D/I, /WR, /RD, /CS1, CS2, /RST, /STB, RS, SI, SCK, P/S, 68/80, CL, PM, FR, SYNC, CK
	"L" Level	V_{IL}	—	—	0	—	0.2V_{DD}	V	
Output Level	"H" Level	V_{OH}	—	I_{OH} = –400 μA	V_{DD} – 0.2	—	V_{DD}	V	DB0~DB7, SO, CL, PM, FR, SYNC, CK
	"L" Level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Column Driver On Resistance	Normal Mode	Rcol1	—	(Note 1)	—	—	7.5	kΩ	SEG1~SEG128
	Power Save Mode	Rcol2	—	(Note 2)	—	—	15.0	kΩ	SEG1~SEG128
Row Driver On Resistance	Normal Mode	Rrow1	—	(Note 1)	—	—	1.5	kΩ	COM1~COM64, ICON
	Power Save Mode	Rrow2	—	(Note 2)	—	—	5.0	kΩ	COM1~COM64, ICON
Input Leakage		I_{IL}	—	V_{inp} = V_{DD} ~GND	– 1	—	1	μA	DB0~DB7, D/I, /WR, /RD, /CS1, CS2, /RST, /STB, RS, SI, SCK, P/S, 68/80, CL, PM, FR, SYNC, CK
Operating Freq		f_{OSC}	—	(Note 6)	—	82	—	kHz	OSC1
External Clock Freq		f_{ex}	—	(Note 6)	—	82	—	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{SS1}	—	(Note 3)	—	200	350	μA	V_{SS}
Current Consumption (2)		I_{SS2}	—	(Note 4)	—	500	700	μA	V_{SS}
Current Consumption (3)		I_{SSSTB}	—	(Note 5)	– 1	—	1	μA	V_{SS}

(Note 1) : V_{SS} + V_{LC0} = 11.0 V, Load current = ± 100 μA, 1/9 bias
(Note 2) : V_{SS} + V_{LC0} = 3.0 V, Load current = ± 100 μA, 1/12 bias
(Note 3) : V_{DD} = 2.7 V, $V_{CC1, 2}$ = V_{OUT4} (X5 mode), No data access, Internal clock (f_{OSC} = 82 kHz), LCD out pin No Load, 1/9 bias, 1/65 duty, OP-Amp. on, regulator on
(Note 4) : V_{DD} = 3.0 V, $V_{CC1, 2}$ = V_{OUT4} (X5 mode), Data access cycle $f\overline{CE}$ = 1 MHz, Internal clock (OSC = 82 kHz), LCD out pin No Load, 1/9 bias, 1/65 duty, OP-Amp. on, regurator on
(Note 5) : V_{DD} = 3.3 V, $V_{CC1, 2}$ – V_{SS} = 16.0 V, /STB = L
(Note 6) : In case of 1/65 duty and f_{FR} = 70 Hz

DC CHARACTERISTICS (2)
(Test condition : If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, V_{LC0} = 0 V, Ta = 25°C)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Output Voltage (X2 Mode)	VO1	(1)	(Note 1)	4.60	5.10	—	V	V_{OUT1}
Output Voltage (X3 Mode)	VO2	(2)	(Note 2)	6.80	7.60	—	V	V_{OUT2}
Output Voltage (X4 Mode)	VO3	(3)	(Note 3)	9.10	10.20	—	V	V_{OUT3}
Output Voltage (X5 Mode)	VO4	(4)	(Note 4)	11.40	12.70	—	V	V_{OUT4}

(Note 1) : V_{IN} = 2.7 V, ILoad = 200 μA, $V_{CC1, 2}$ = 5.40 V (external power supply)
CnA – CnB = 1.0 μF, $V_{OUT1} - V_{SS}$ = 1.0 μF, OSC = 82 kHz, Ta = 25°C
(Note 2) : V_{IN} = 2.7 V, ILoad = 200 μA, $V_{CC1, 2}$ = 8.10 V (external power supply)
CnA – CnB = 1.0 μF, $V_{OUT1} - V_{SS}$ = 1.0 μF, OSC = 82 kHz, Ta = 25°C
(Note 3) : V_{IN} = 2.7 V, I_{Load} = 200 μA, $V_{CC1, 2}$ = 10.80 V (external power supply)
CnA – CnB = 1.0 μF, $V_{OUT1} - V_{SS}$ = 1.0 μF, OSC = 82 kHz, Ta = 25°C
(Note 4) : V_{IN} = 2.7 V, I_{Load} = 200 μA, $V_{CC1, 2}$ = 13.50 V (external power supply)
CnA – CnB = 1.0 μF, $V_{OUT1} - V_{SS}$ = 1.0 μF, OSC = 82 kHz, Ta = 25°C

DC CHARACTERISTICS (3) This spec table is not fixed.
(Test condition : If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, V_{LC0} = 0 V)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN	TYP.	MAX	UNIT	APPLICABLE TERMINAL
Regulator Reference High Voltage (1)	VHR	—	(Note 5) X4 / X5 = 0, Ta = 25°C	12.3	12.5	12.7	V	V_{CC2}
		—	(Note 5) X4 / X5 = 1, Ta = 25°C	10.8	11.0	11.2	V	V_{CC2}
Regulator Reference High Voltage (2)	VHRC	—	(Note 5) Ta = – 20°C	0.999 × VHR	1.012 × VHR	1.025 × VHR	V	V_{CC2}
Regulator Reference High Voltage (3)	VHRH	—	(Note 5) Ta = 60°C	0.982 × VHR	0.994 × VHR	1.006 × VHR	V	V_{CC2}

(Note 5) : $V_{CC1} \geqq$ 12.8 V at Ta = – 20~60°C

Note : Temperature dependence of V_{ref12} and VHR should be defined after process variation evaluation finish.

DC CHARACTERISTICS (4)
(Test condition : If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, V_{LC0} = 0 V)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Op-Amp Output Voltage Offset (1)	V_{opoff}	—	(Note 1)	– 100	—	100	mV	V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}
Op-Amp Output Voltage Offset (2)	V_{opoffs}	—	(Note 2)	TBD	—	TBD	mV	V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}

(Note 1) : V_{DD} = 2.7~3.3 V, V_{SS} = 0 V, 1/9 bias, 1/65 duty
V_{CC1} = 13.0 V, V_{CC2} = 12.5 V, Contrast control = max
Op-Amp ON, DC-DC OFF, regulator OFF, LCD outpin No Load

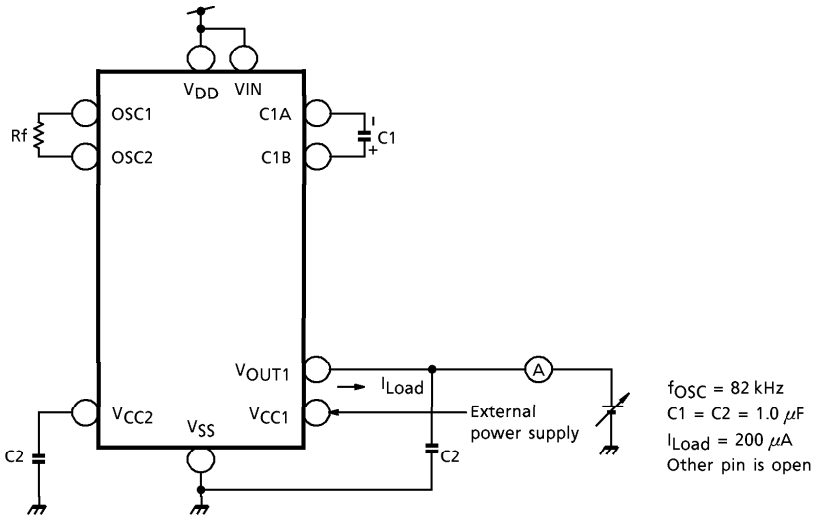
Case of V_{LC0} : $12.5 - V_{LC0} = V_{opoff}$
V_{LC1} : $(V_{LC0} \div 8/9) - V_{LC1} = V_{opoff}$
V_{LC2} : $(V_{LC0} \div 7/9) - V_{LC2} = V_{opoff}$
V_{LC3} : $(V_{LC0} \div 2/9) - V_{LC3} = V_{opoff}$
V_{LC4} : $(V_{LC0} \div 1/9) - V_{LC4} = V_{opoff}$

(Note 2) : V_{DD} = 2.7~3.3 V, V_{SS} = 0 V, 1/9 bias, 1/65 duty
V_{CC1} = 13.0 V, V_{CC2} = 12.5 V, Contrast control = max
Op-Amp ON, DC-DC OFF, regulator OFF, LCD outpin No Load

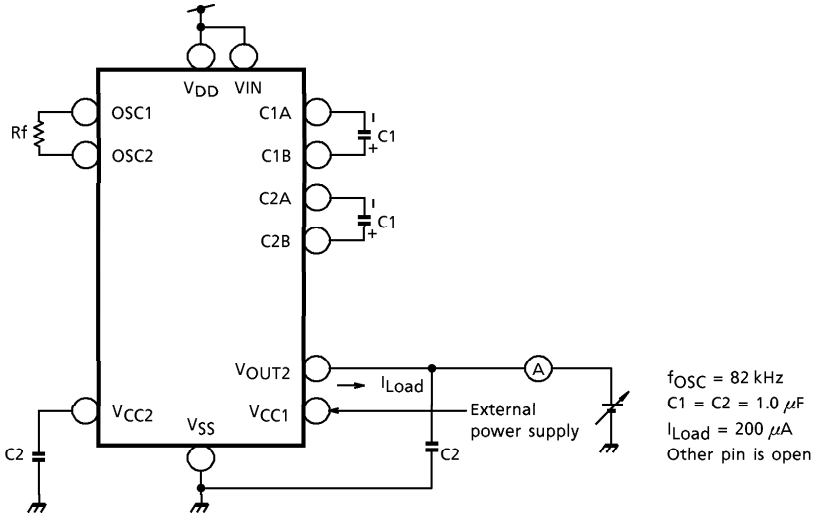
$$V_{opoffs} = ((V_{LC1} - V_{LC2}) - (V_{LC0} - V_{LC1})) + ((V_{LC3} - V_{LC4}) - (V_{LC4} - V_{LC5}))$$

TEST CIRCUIT

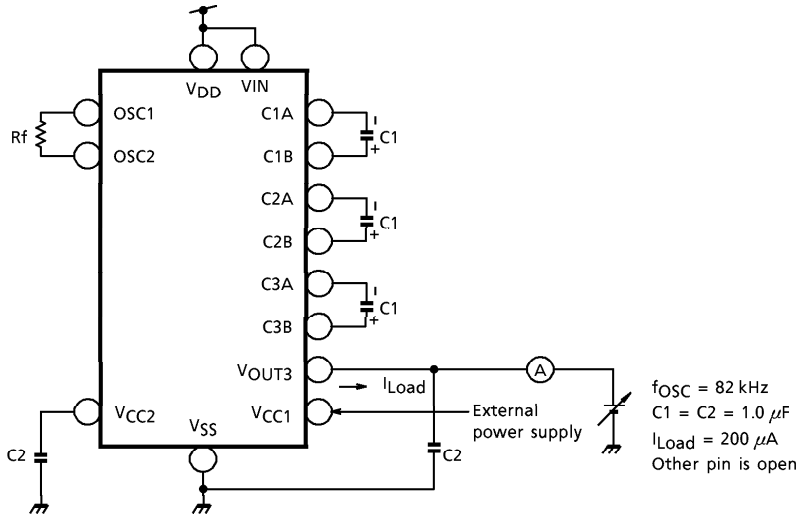
(1) DC-DC converter X2 mode



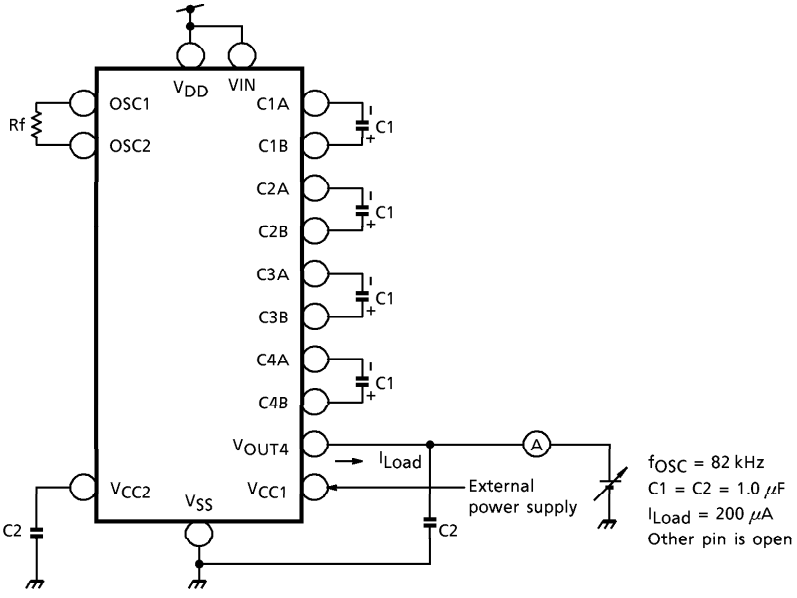
(2) DC-DC converter X3 mode



(3) DC-DC converter X4 mode

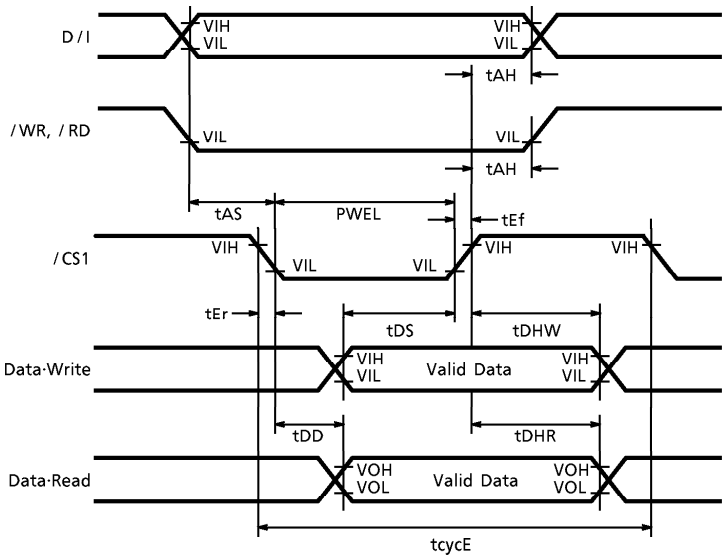


(4) DC-DC converter X5 mode



AC CHARACTERISTICS

- Switching characteristics (80 series MPU 8 bit interface)

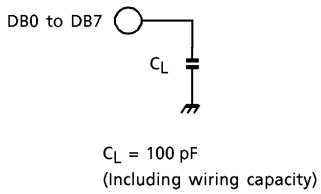


TEST CONDITION
(If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEL	410		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	20		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	100		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		300	ns
Data Hold Time	tDHR (Note)	20		ns

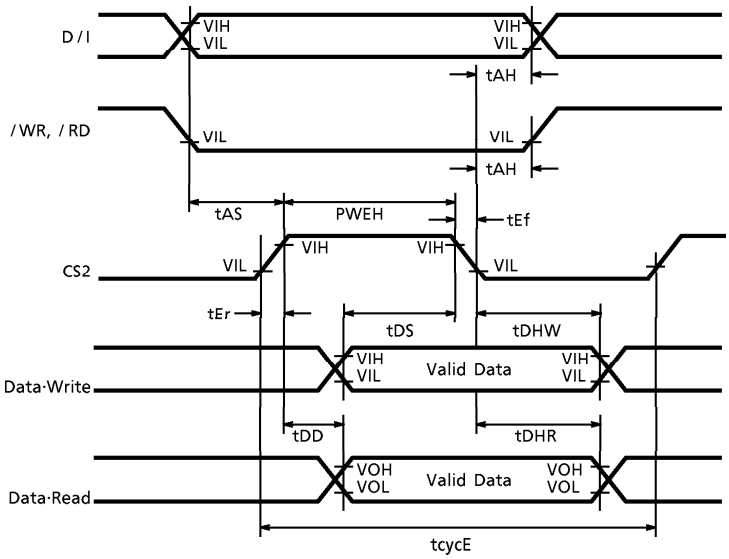
(Note) : Connect to Load circuit.

LOAD CIRCUIT



AC CHARACTERISTICS

- Switching characteristics (80 series MPU 8 bit interface)

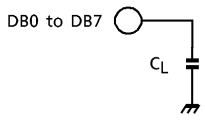


TEST CONDITION
(If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNITS
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEH	410		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	20		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	100		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		300	ns
Data Hold Time	tDHR (Note)	20		ns

(Note) : Connect to Load circuit.

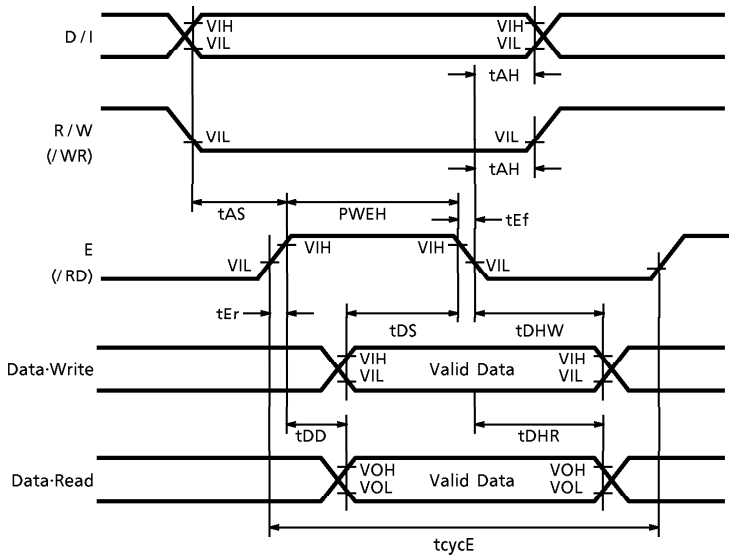
LOAD CIRCUIT



C_L = 100 pF
(Including wiring capacity)

AC CHARACTERISTICS

- Switching characteristics (68 series MPU 8 bit interface)

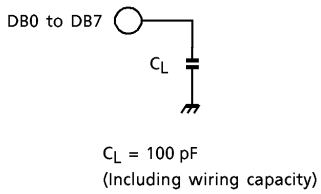


TEST CONDITION
(If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, Ta = 25°C)

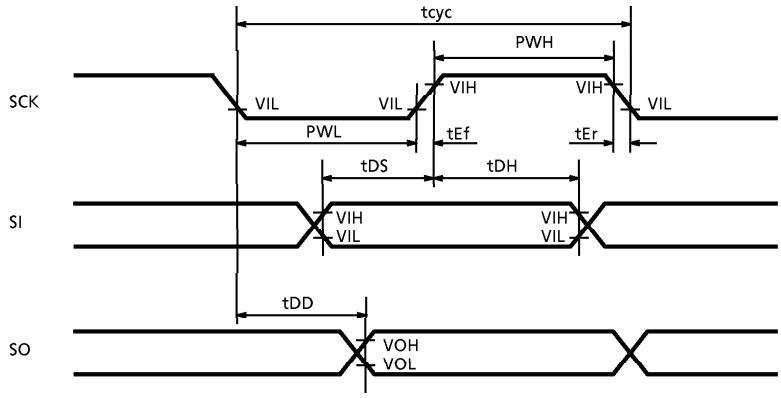
ITEM	SYMBOL	MIN.	MAX.	UNITS
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEH	410		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	20		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	100		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		300	ns
Data Hold Time	tDHR (Note)	20		ns

(Note) : Connect to Load circuit.

LOAD CIRCUIT



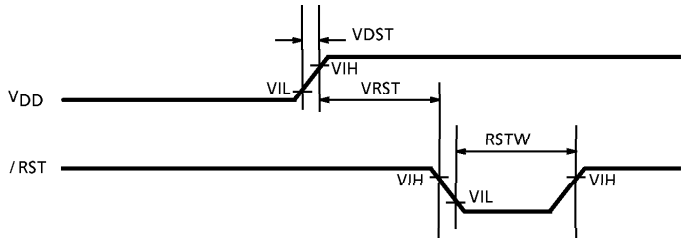
- Switching characteristics (serial interface)



TEST CONDITION
(If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
Clock Cycle Time	tcycC	2000		ns
Clock Pulse Width	PWCL, PWCH	900		ns
Clock Rise / Fall Time	tCr, tCf		25	ns
Data Set-up Time	tDS	300		ns
Data Hold Time	tDH	100		ns
Data Delay Time	tDD		200	ns

- Switching characteristics (4)



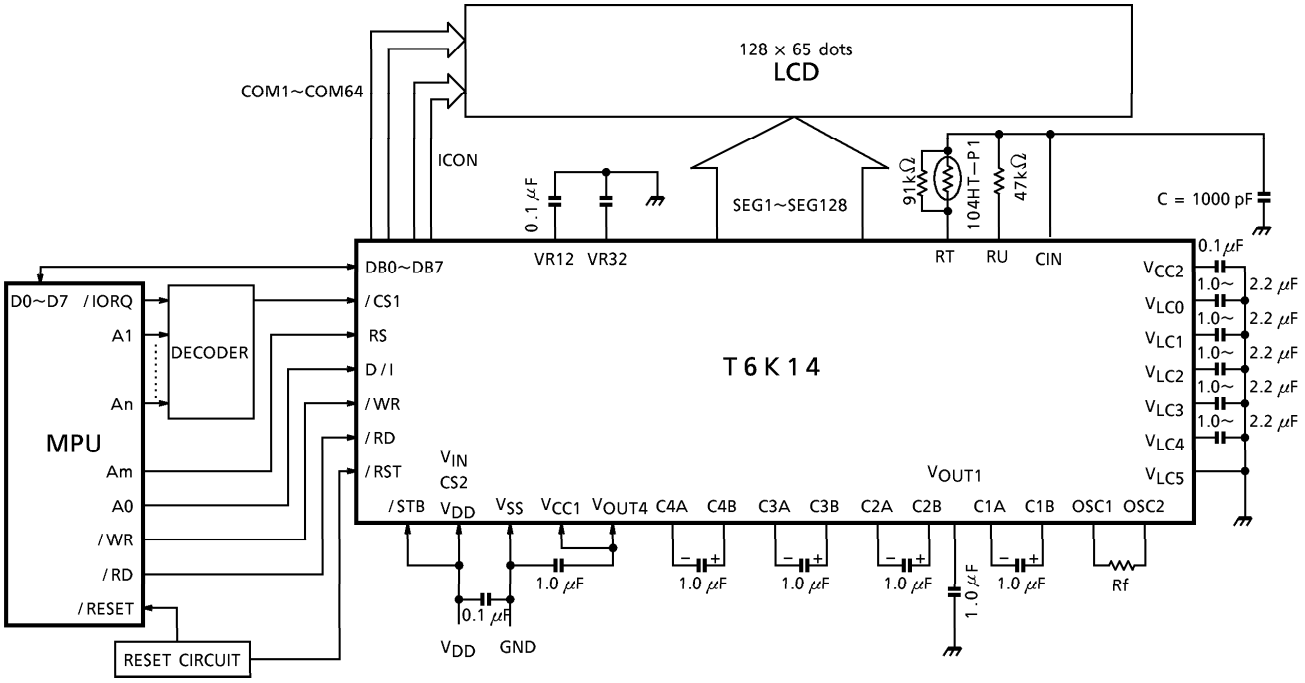
TEST CONDITION
(If not specified, V_{SS} = 0 V, V_{DD} = 2.7~3.3 V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
V_{DD} Rise Time	VDST		1	ms
Reset Hold Time	VRST	1		μs
Reset Pulse Width	RSTW	1		μs

APPLICATION CIRCUIT (1)

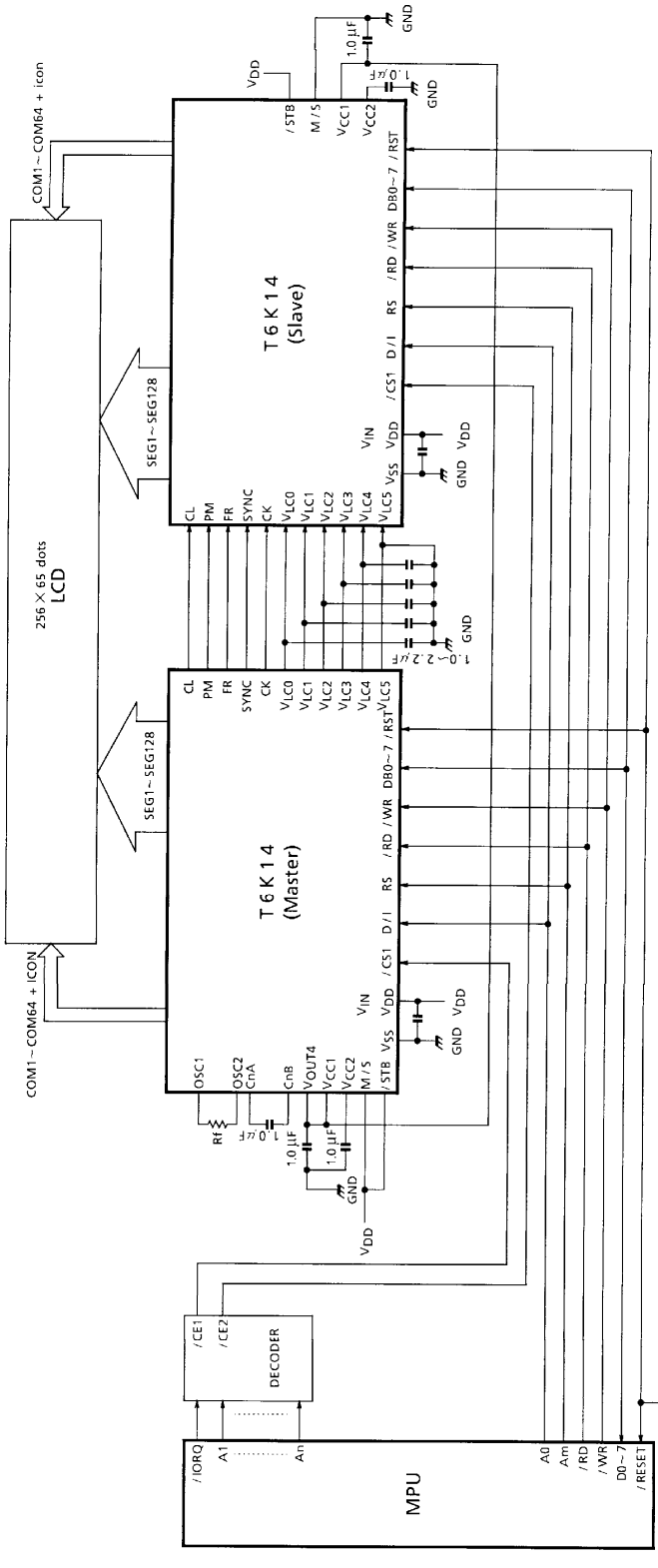
T6K14 One chip mode

- Using CR oscillation
- LCD drive bias 1 / 9
- Using DC-DC converter (X5 mode)
- Using 80 series MPU
- Using temperature compensation



APPLICATION CIRCUIT (2)
T6K14 Two chip mode

- Using CR oscillation
- LCD drive bias 1 / 9
- Using DC-DC converter (X5 mode)
- Using 80 series MPU



T6K14—40