# 8-bit Proprietary Microcontrollers

**CMOS**

# F²MC-8L MB89210 Series

# MB89215/F217/P215/PV210

## ■ DESCRIPTION

The MB89210 series is a one-chip microcontroller that features a compact instruction set and contains a range of peripheral functions including timers, a serial interface, A/D converters and external interrupts.

## ■ FEATURES

- F²MC-8L CPU core
- Maximum memory spaces            : 64 Kbytes
- Minimum instruction execution time : 0.32 µs to 5.12 µs (at 12.5 MHz)
- Interrupt processing time         : 2.88 µs to 46.08 µs (at 12.5 MHz)
- I/O port                          : Max 22
- 21-bit time base timer
- 8-bit PWM timer
- 8-/16-bit capture timer/counter : 2 ch
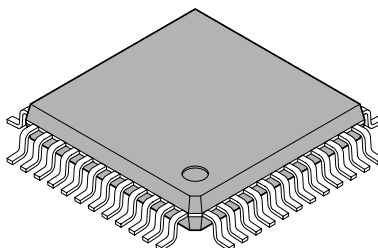- Watchdog timer
- 12-bit PPG timer

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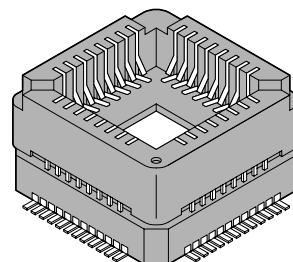
## ■ PACKAGE

| 30-pin Plastic SSOP | 48-pin Plastic QFP | 48-pin Ceramic MQFP |
|---|---|---|
| (FPT-30P-M02) | (FPT-48P-M13) | (MQP-48C-P02) |
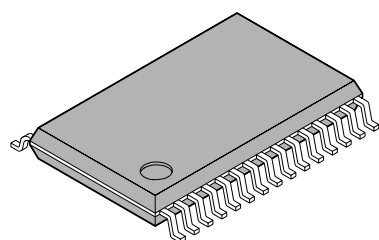
FUJITSU

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- 10-bit A/D converter : 8 ch
- LIN-UART
- 8-bit serial I/O
- External Interrupt : 3 ch
- External or CR (built-in) oscillation clock, switchable
- Low power consumption modes (stop modes, sleep modes)
- Package : SSOP-30,QFP-48, MQFP-48
- CMOS technology

## ■ PRODUCT LINEUP

| Part number<br>Parameter | MB89215 | MB89F217 | MB89P215 | MB89PV210 |
|---|---|---|---|---|
| Type | For mass products (Mask ROM product) | Flash products (Flash ROM product) | One-time product (for small-scale production) | Piggy back/ Evaluation product (for development) |
| ROM capacity | 16 Kbyte (Built-in ROM) | 32 Kbyte (Built-in Flash memory) | 16 Kbyte (Built-in PROM) | 32 Kbyte (External EPROM) |
| RAM capacity | 512 byte | 1 Kbyte | 512 byte | 2 Kbyte |
| CPU functions | Number of basic instructions : 136<br>Instruction bit length : 8 bits<br>Instruction length : 1 to 3 bytes<br>Data bit length : 1, 8, and 16 bits<br>Minimum instruction execution time : 0.32 µs to 5.12 µs (at 12.5 MHz)<br>Interruption processing time : 2.88 µs to 46.08 µs (at 12.5 MHz) | | | |

| | | |
|---|---|---|
| Peripheral functions | Ports | General purpose I/O port × 21 (also usable as resources) General purpose input port × 1 |
| | 21-bit time base timer | 21 bits<br>Interrupt cycle : at 10 MHz (0.82 ms,3.3 ms,26.2 ms,419.4 ms) |
| | Watchdog timer | Reset generation cycle : at 10 MHz (Min 419.4 ms) |
| | 8-bit PWM timer | 8-bit interval timer operation (supports square wave output, operating clock period : 0.4 µs to 25.6 µs)<br>8-bit resolution PWM operation (conversion period : 102.4 µs to 26.84 µs ) |
| | 8/16-bit capture timer counter | 8-bit capture timer/counter × 1 channel + 8-bit timer<br>or 16-bit capture timer/counter × 1 channel<br>Capable of event count operation and square wave output using external clock input with 8-bit timer 0 or 16-bit counter |
| | LIN-UART | Full duplex, Synchronous/asynchronous transfer (with start/stop bit), Capable of setting over 30,000 different baud rates using a 15-bit reload counter<br>Support for the LIN protocol, slave nodes, and LIN synch break/sync field detection |
| | 8-bit serial I/O | 8-bit length, Selectable LSB first or MSB first<br>Transfer clock (0.8 µs external, 0.8 µs, 3.2 µs, 12.8 µs internal) |
| | 12-bit PPG timer | Output requency : Selectable pulth width and cycle (Cycle : 1.6 µs to 419.3 ms ) |
| | External interrupt circuit | 3-channel (interrupt vector, request flag, requesr output acceptance)<br>Edge selectable (selectable rising, falling or both edge)<br>Can be use for recovery from stop or sleep mode (edge detection also available in stop mode). |
| | A/D converter | 10-bit accurasy × 8-channel<br>A/D conversion function (conversion time : 15.2 µs/10 MHz)<br>Continuous activation by an 8-/16-bit timer/counter output or time base timer output capable. |

| | | | | |
|---|---|---|---|---|
| Standby mode | Sleep mode and Stop mode | | | |
| Operating voltage * | 3.5 V to 5.5 V | 3.5 V to 5.5 V | 3.5 V to 5.5 V | 3.5 V to 5.5 V |
| CR(built-in) oscillator | Yes | Yes | Yes | No |

* : The minimum operating voltage varies with the operating frequency, the function and the connected ICE.

Note : Unless otherwise stated, clock periods and conversion times are for 10 MHz operation with the internal clock operating at maximum speed.

## ■ PACKAGES AND CORRESPONDING PRODUCTS

| Package | MB89215 | MB89F217 | MB89P215 | MB89PV210 |
|---|---|---|---|---|
| FPT-30P-M02 | O | × | O | × *1 |
| FPT-48P-M13 | O | O | × | × *2 |
| MQP-48C-P02 | × | × | × | O |
| Power supply pins | Vcc,Vss × 2 | Vcc, Vss × 3, AVcc, AVss | Vcc,Vss × 2 | Vcc, Vss × 2, AVcc, AVss |

O : Yes      × : No

*1 : Adapter for 48-pin to 30-pin conversion (manufactured by Sunhayato Corp.)
     Part number : 48QF-30SOP-8L
     Inquiry : Sunhayato Corp.     TEL     : (81)-3-3984-7791
                                   FAX     : (81)-3-3971-0535
                                   E-mail  : adapter@sunhayato.co.jp

*2 : Adapter for 48-pin (EVA)  to 48-pin  (MASK/FLASH) conversion.
     Part number : Under development.

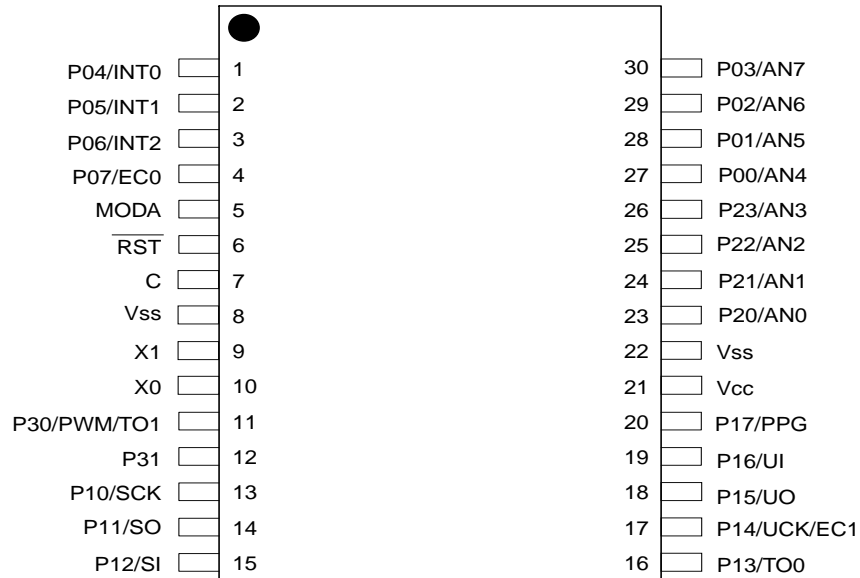## ■ DIFFERENCES AMONG PRODUCTS

### 1.   Memory space

When this product is used in a piggy-back or other evaluation configuration, it is necessary to carefully confirm the differences between the model being used and the product it is evaluating.

### 2.   Current Consumption

• On the MB89PV210, the additional current consumed by the EPROM is added at the connecting socket on the back side.
• When operating at low speed, the current consumption in the one-time PROM or EPROM models is greater than on the mask ROM models. However, current consumption in sleep or stop modes is identical. However, in sleep/stop mode the current consumption is the same.
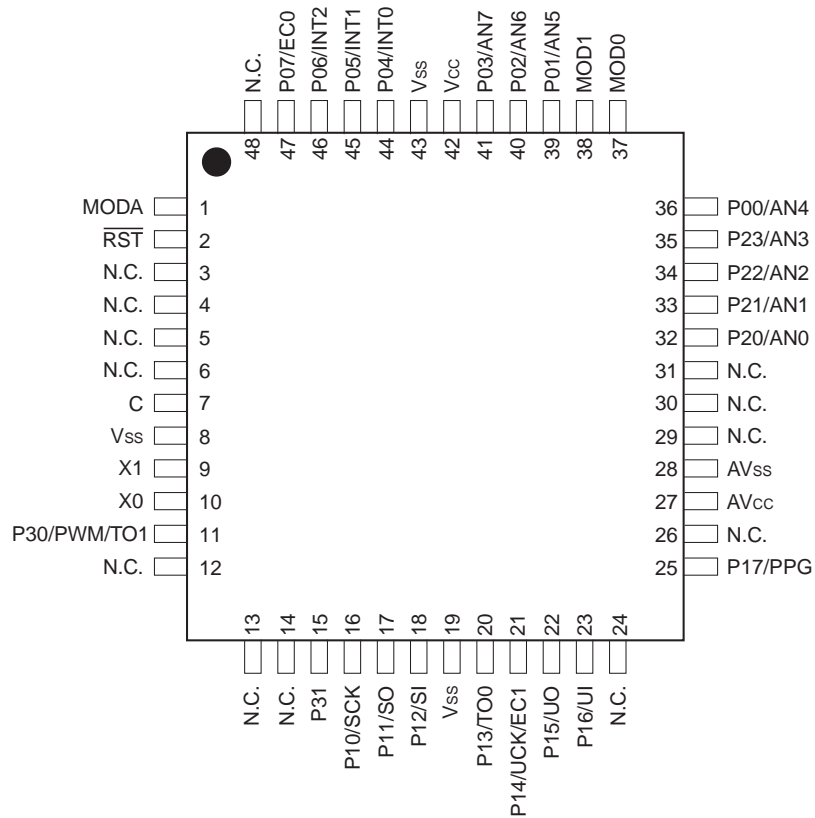
## ■ PIN ASSIGNMENT

(TOP VIEW)

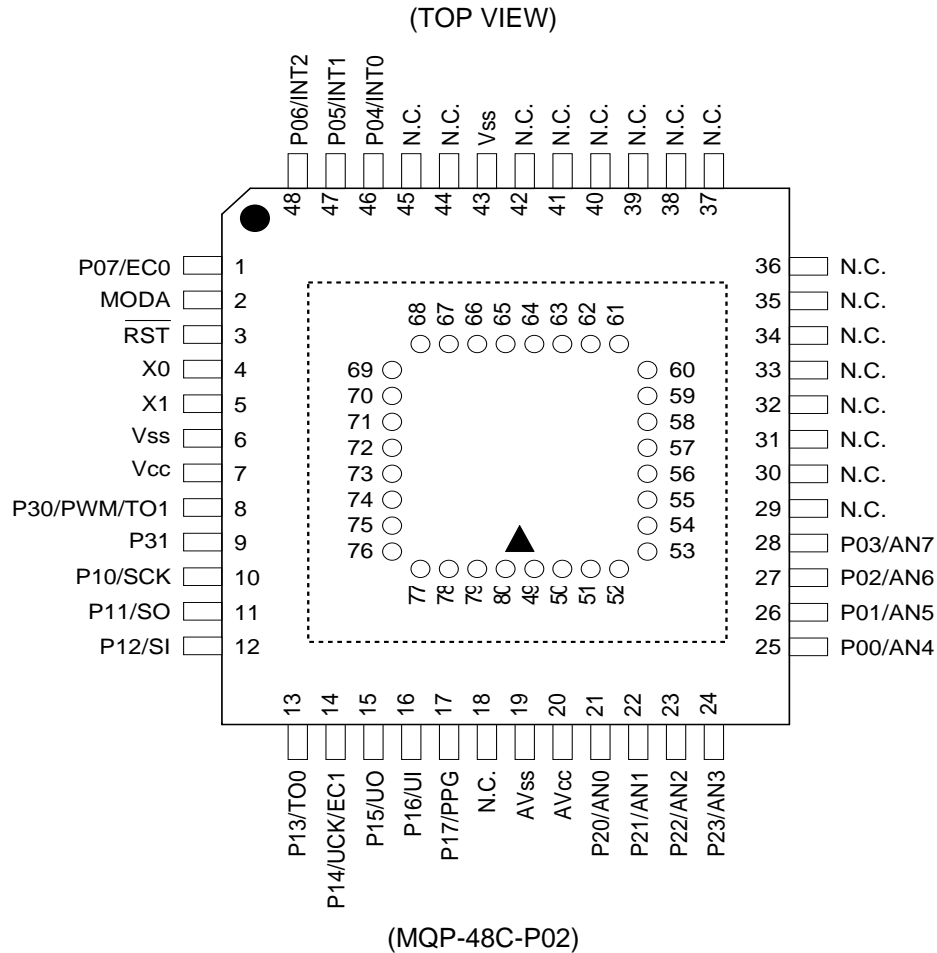| Pin | | |
|---|---|---|
| P04/INT0 | 1 | 30 | P03/AN7 |
| P05/INT1 | 2 | 29 | P02/AN6 |
| P06/INT2 | 3 | 28 | P01/AN5 |
| P07/EC0 | 4 | 27 | P00/AN4 |
| MODA | 5 | 26 | P23/AN3 |
| RST | 6 | 25 | P22/AN2 |
| C | 7 | 24 | P21/AN1 |
| Vss | 8 | 23 | P20/AN0 |
| X1 | 9 | 22 | Vss |
| X0 | 10 | 21 | Vcc |
| P30/PWM/TO1 | 11 | 20 | P17/PPG |
| P31 | 12 | 19 | P16/UI |
| P10/SCK | 13 | 18 | P15/UO |
| P11/SO | 14 | 17 | P14/UCK/EC1 |
| P12/SI | 15 | 16 | P13/TO0 |

(FPT-30P-M02)

(TOP VIEW)

Top pins (48–37): N.C., P07/EC0, P06/INT2, P05/INT1, P04/INT0, Vss, Vcc, P03/AN7, P02/AN6, P01/AN5, MOD1, MOD0

Left (1–12): MODA, RST, N.C., N.C., N.C., N.C., C, Vss, X1, X0, P30/PWM/TO1, N.C.

Right (36–25): P00/AN4, P23/AN3, P22/AN2, P21/AN1, P20/AN0, N.C., N.C., N.C., AVss, AVcc, N.C., P17/PPG

Bottom (13–24): N.C., N.C., P31, P10/SCK, P11/SO, P12/SI, Vss, P13/TO0, P14/UCK/EC1, P15/UO, P16/UI, N.C.

(FPT-48P-M13)

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*(Continued)*

(TOP VIEW)

P06/INT2  P05/INT1  P04/INT0  N.C.  N.C.  Vss  N.C.  N.C.  N.C.  N.C.  N.C.  N.C.
48  47  46  45  44  43  42  41  40  39  38  37

| Left pins | | Right pins | |
|---|---|---|---|
| P07/EC0 | 1 | 36 | N.C. |
| MODA | 2 | 35 | N.C. |
| RST | 3 | 34 | N.C. |
| X0 | 4 | 33 | N.C. |
| X1 | 5 | 32 | N.C. |
| Vss | 6 | 31 | N.C. |
| Vcc | 7 | 30 | N.C. |
| P30/PWM/TO1 | 8 | 29 | N.C. |
| P31 | 9 | 28 | P03/AN7 |
| P10/SCK | 10 | 27 | P02/AN6 |
| P11/SO | 11 | 26 | P01/AN5 |
| P12/SI | 12 | 25 | P00/AN4 |

Inner pins: 68 67 66 65 64 63 62 61 / 69 70 71 72 73 74 75 76 / 60 59 58 57 56 55 54 53 / 77 78 79 80 49 50 51 52

13  14  15  16  17  18  19  20  21  22  23  24

P13/TO0  P14/UCK/EC1  P15/UO  P16/UI  P17/PPG  N.C.  AVss  AVcc  P20/AN0  P21/AN1  P22/AN2  P23/AN3

(MQP-48C-P02)

| Pin no. | Pin | Pin no. | Pin | Pin no. | Pin | Pin no. | Pin |
|---|---|---|---|---|---|---|---|
| 49 | Vpp | 57 | N.C. | 65 | O4 | 73 | OE |
| 50 | A12 | 58 | A2 | 66 | O5 | 74 | N.C. |
| 51 | A7 | 59 | A1 | 67 | O6 | 75 | A11 |
| 52 | A6 | 60 | A0 | 68 | O7 | 76 | A9 |
| 53 | A5 | 61 | O1 | 69 | O8 | 77 | A8 |
| 54 | A4 | 62 | O2 | 70 | CE | 78 | A13 |
| 55 | A3 | 63 | O3 | 71 | A10 | 79 | A14 |
| 56 | N.C. | 64 | Vss | 72 | N.C. | 80 | Vcc |

N.C. : Internal connection only. Not for use.

## ■ PIN DESCRIPTIONS

| Pin no. | | | Pin name | Circuit type | Function |
|---|---|---|---|---|---|
| SSOP[1] | QFP[2] | MQFP[3] | | | |
| 10 | 10 | 4 | X0 | A | Connecting pins to crystal oscillator or other oscillator. |
| 9 | 9 | 5 | X1 | | When using ecternal clock, input to X0 and X1 is left open. |
| — | 37 | — | MOD0 | C/D$_1$[4] | Input pins for memory access mode setting. Connect directly to V$_{SS}$. |
| — | 38 | — | MOD1 | | Input pins for memory access mode setting. Connect directly to V$_{SS}$. |
| 5 | 1 | 2 | MODA | C/D$_2$[5] | Input pins for memory access mode setting. Connect directly to V$_{SS}$. |
| 6 | 2 | 3 | $\overline{\text{RST}}$ | E | Reset I/O pin. This pin has pull-up resistance with N-ch open drain or hysteresis input. At an internal reset request, an "L" signal is output. An "L" level input initializes the internal circuits. |
| 27 to 30 | 36, 39 to 41 | 25 to 28 | P00/AN4 to P03/AN7 | G | General purpose I/O port. Hysteresis input. These pins also functions as the analog input of A/D converter. |
| 1 to 3 | 44 to 46 | 46 to 48 | P04/INT0 to P06/INT2 | F | General purpose I/O port. These pins also functions as the external interrupt input. Hysteresis input. |
| 4 | 47 | 1 | P07/EC0 | | General purpose I/O port. This pin also functions as external clock of 8-/16-bit capture timer/counter 0 or capture input pin. Hysteresis input. |
| 13 | 16 | 10 | P10/SCK | | General purpose I/O port. This pin also functions as clock input/output pin of serial I/O. Hysteresis input. |
| 14 | 17 | 11 | P11/SO | | General purpose I/O port. This pin also functions as the data output pin of serial I/O. Hysteresis input. |
| 15 | 18 | 12 | P12/SI | | General purpose I/O port. This pin also functions as the data input pin of serial I/O. Hysteresis input. |
| 16 | 20 | 13 | P13/TO0 | | General purpose I/O port. This pin also functions as the output pin of 8-/16-bit capture timer/counter 0. Hysteresis input. |
| 17 | 21 | 14 | P14/UCK/ EC1 | | General purpose I/O port. This pin also functions as the clock input/output pin of LIN-UART and the external clock of 8-/16-bit capture timer/counter 1 or capture input pin. Hysteresis input. |
| 18 | 22 | 15 | P15/UO | | General purpose I/O port. This pin also functions as the data output pin of LIN-UART. Hysteresis input |

*(Continued)*

*(Continued)*

| Pin no. | | | Pin name | Circuit type | Function |
|---|---|---|---|---|---|
| SSOP*1 | QFP*2 | MQFP*3 | | | |
| 19 | 23 | 16 | P16/UI | H | General purpose I/O port.<br>This pin also functions as the data input pin of LIN-UART.<br>General port input is hysteresis and resource input is CMOS. |
| 20 | 25 | 17 | P17/PPG | F | General purpose I/O port.<br>This pin also functions as 12-bit PPG timer output.<br>Hysteresis input. |
| 23 to 26 | 32 to 35 | 21 to 24 | P20/AN0 to P23/AN3 | G | General purpose I/O port.<br>Shared for A/D converter analog input pin.<br>Hysteresis input. |
| 11 | 11 | 8 | P30/PWM/TO1 | F | General purpose I/O port.<br>This pin also functions as the output pin of 8-bit PWM and 8-/16-bit capture timer/counter 1.<br>Hysteresis input. |
| 12 | 15 | 9 | P31 | B | General purpose I/O port of CMOS type. |
| 21 | 42 | 7 | V$_{CC}$ | — | Power supply pin. |
| 8,22 | 8, 19, 43 | 6,43 | V$_{SS}$ | — | Power supply pin (GND). Use the both pins at the same voltage level. |
| — | 27 | 20 | AV$_{CC}$ | — | A/D converter power supply pin.<br>Apply potential under V$_{CC}$ to this pin. |
| — | 28 | 19 | AV$_{SS}$ | — | A/D converter power supply pin (GND).<br>Use at the same voltage level as the V$_{SS}$ supply. |
| 7 | 7 | — | C | — | This is the power supply stabilization capacitor pin for MB89F217 and MB89P215.<br>Connect an external capacitor of 0.1 $\mu$F.<br>MB89215 is not internally connected. It is unnecessary to connect a capacitor. |
| — | 3 to 6, 12 to 14, 24, 26, 29 to 31, 48 | 18, 29 to 42, 44,45 | N.C. | — | Internal connect pin.<br>Be sure this pin is left open. |

*1 : FPT-30P-M02

*2 : FPT-48P-M13

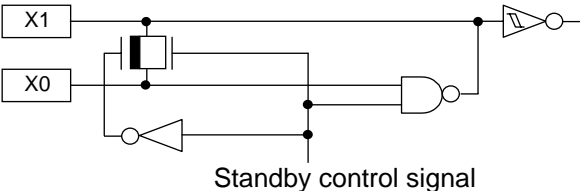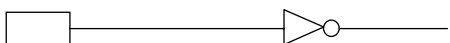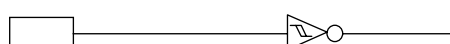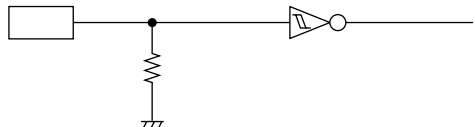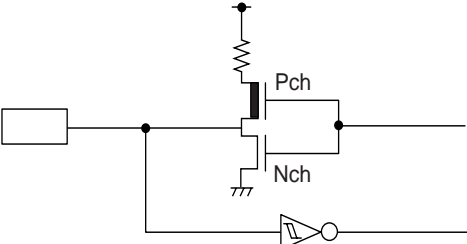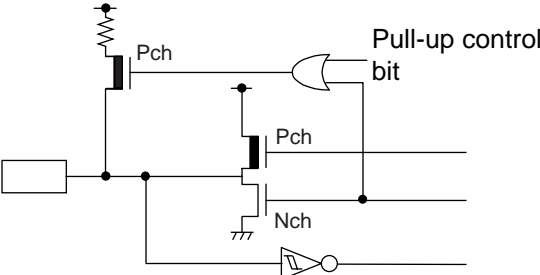*3 : MQP-48C-P02

*4 : MB89F217 is C.

*5 : MB89F217 and MB89P215 are C.

## ■ EXTERNAL EPROM PIN DESCRIPTION (MB89PV210 only)

| Pin no. | Pin name | I/O | Function |
|---|---|---|---|
| 49 | Vpp | O | "H" level output pin. |
| 50<br>51<br>52<br>53<br>54<br>55<br>58<br>59<br>60 | A12<br>A7<br>A6<br>A5<br>A4<br>A3<br>A2<br>A1<br>A0 | O | Address output pin. |
| 61<br>62<br>63 | O1<br>O2<br>O3 | I | Data input pin. |
| 64 | $V_{SS}$ | O | Power supply pin (GND). |
| 65<br>66<br>67<br>68<br>69 | O4<br>O5<br>O6<br>O7<br>O8 | I | Data input pin. |
| 70 | CE | O | Chip acceptance pin for ROM.<br>Output "H" at standby. |
| 71 | A10 | O | Address output pin. |
| 73 | OE | O | Output acceptance pin for ROM.<br>Output "L" usually. |
| 75<br>76<br>77<br>78<br>79 | A11<br>A9<br>A8<br>A13<br>A14 | O | Address output pin. |
| 80 | $V_{CC}$ | O | Power supply pin for EPROM. |
| 56<br>57<br>72<br>74 | N.C. | — | Internal connect pin.<br>Must be left open. |

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|---------|
| A | X1 X0 Standby control signal | • Oscillator feedback resistance : approx. 1 MΩ |
| B | | • CMOS input |
| C | | • Hysteresis input |
| D$_1$ | | • Open |
| D$_2$ | | • With pull-down resistance : approx. 50 kΩ(5V)<br>• Hysteresis input |
| E | Pch Nch | • Output pull-up resistance (Pch) approx. 50 kΩ (5V)<br>• Hysteresis input |
| F | Pch Pull-up control bit Pch Nch | • CMOS output<br>• Hysteresis input<br>• Selectable by pull-up resistor register |

*(Continued)*

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*(Continued)*

| Type | Circuit | Remarks |
|------|---------|---------|
| G | Pch<br>Pch<br>Nch<br>Pull-up control bit<br>Analog input<br>A/D acceptance | • CMOS output<br>• Hysteresis input<br>• Analog input<br>• Selectable by pull-up resistor register |
| H | Pch<br>Pch<br>Nch<br>Pull-up control bit | • CMOS output<br>• Hysteresis input<br>• CMOS input<br>• Selectable by pull-up resistor register |

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input or output pins other than the medium-and high-voltage pins or if voltage higher than the rating is applied between $V_{CC}$ and $V_{SS}$.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog input from exceeding the digital power supply ($V_{CC}$) when the analog system power supply is turned on and off.

To supply power, turn on the digital power supply ($V_{CC}$) and then the analog power supply ($AV_{CC}$).

### 2. Treatment of Unused Input Pins

Leaving unused input teminals open may lead to permanent damage due to malfunction and latchup; pull up or pull down the terminals through the resistors of 2 kΩ or more.

Make the unused I/O terminal in a state of output and leave it open and if it is in an input state, handle it with the same procedure as the input terminals.

### 3. Treatment of N.C. Pins

Any pins marked "NC" (not connected) must be left open.

### 4. Power Supply Voltage Fluctuations

Although Vcc power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important.As stabilization guidelines, it is recommended to control power so that $V_{CC}$ ripple fluctuations (P-P value) will be less than 10% of the standard $V_{CC}$ value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms.

### 5. Treatment of power supply pin

All $V_{SS}$ power suppluy pin must be use at the same voltage level.

Connect to be $AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$ even if the A/D converters are not in use in MB89PV210.

### 6. Notes on Using External Clock

When an external clock is used, oscillation stabilization time is required for even power-on reset and release from stop mode.

### 7. Notes on using the CR (internal) oscillator

To use the CR (internal) oscillator as the operating clock for the MB89215, MB89F217 or MB89P215, adjust the timer value and baud rate setting.

### 8. Program Execution in RAM

When the MB89PV210 is used with an emulation pod other than the MB2144-508, no program can be executed in RAM.

### 9. Operation check for evaluating the LIN-UART

When the MB89215, MB89F217 or MB89P215 uses the CR (internal) oscillator as the clock for the LIN-UART, the evaluation program (MB89PV210 [customized for external oscillation]) requires an operation check within a range of oscillation frequencies from 8.5 MHz to 11.5 MHz.

## 10. Handling reset pin

Reset pin must be inputted external reset.

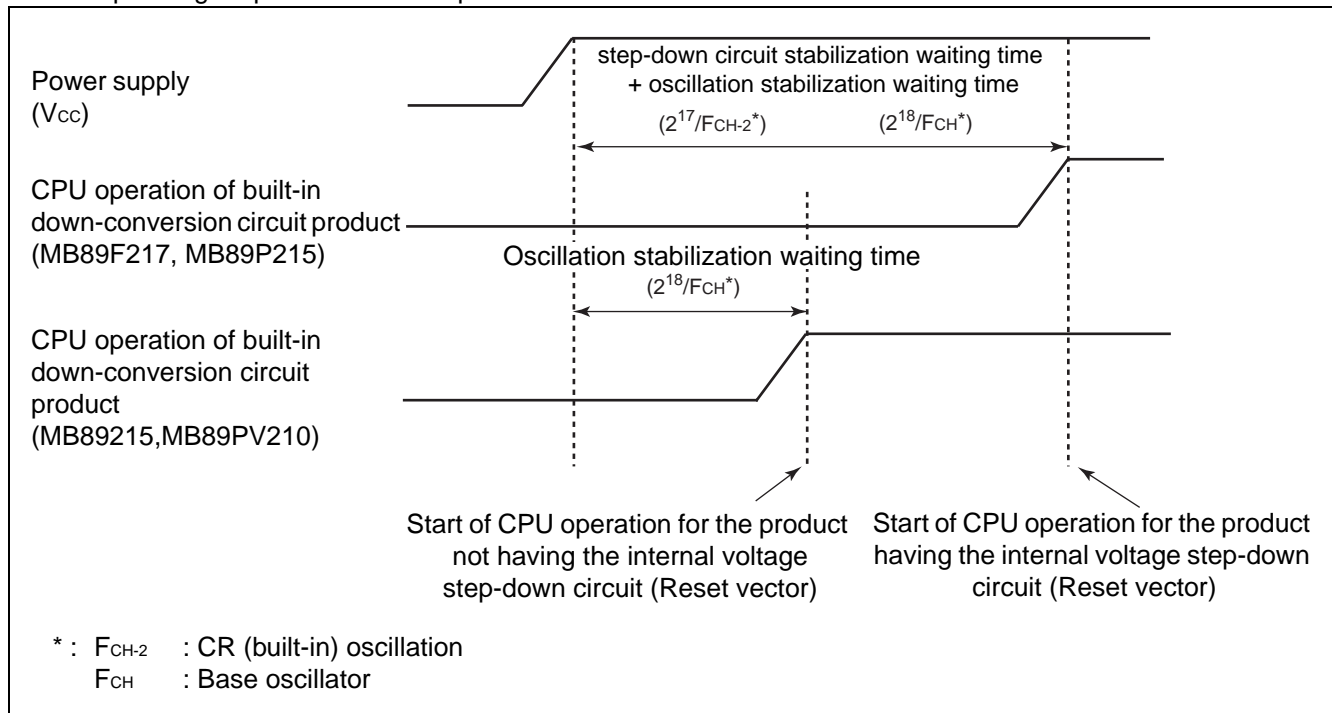## 11. Up/down conversion circuit stabilization waiting time

MB89210 series contains the following products and the operating characteristics vary with whether they contain the internal stepdown circuit.

| Product name | Operating voltage * | Down conversion |
|---|---|---|
| MB89215 | 3.5 V to 5.5 V | not built-in |
| MB89F217 | 3.5 V to 5.5 V | built-in |
| MB89P215 | 3.5 V to 5.5 V | built-in |
| MB89PV210 | 3.5 V to 5.5 V | not built-in |

* : The minimum operating voltage varies with the operating frequency, the function and the connected ICE.

The same built-in resources are used for the above product types; operating sequences after the power-on reset are different depending on whether they have the internal voltages step-down circuit.

The operating sequences after the power-on reset with the different models will be described below.



Power supply
($V_{CC}$)

step-down circuit stabilization waiting time
+ oscillation stabilization waiting time

($2^{17}/F_{CH-2}$*)        ($2^{18}/F_{CH}$*)

CPU operation of built-in
down-conversion circuit product
(MB89F217, MB89P215)

Oscillation stabilization waiting time
($2^{18}/F_{CH}$*)

CPU operation of built-in
down-conversion circuit
product
(MB89215,MB89PV210)

Start of CPU operation for the product
not having the internal voltage
step-down circuit (Reset vector)

Start of CPU operation for the product
having the internal voltage step-down
circuit (Reset vector)

* :  $F_{CH-2}$   : CR (built-in) oscillation
     $F_{CH}$     : Base oscillator

As described above, CPU starts at delayed time with the product having the internal voltage step-down circuit compared with the product not having the internal voltage step-down circuit. This is because the time should be allowed for the stabilization time for voltage step-down circuit for normal operation.

Note : As the period of the oscillation is unstable immediately after oscillation starts, the listed oscillation stabilization delay times are guides only.

## 12. Treatment of analog input

The analog input also serves as a general-purpose input/output port.  The A/D enable register is initialized at a reset.  When the intermediate-level signal is input in port input mode (ADEN:ADEx = 0), an input leakage current flows to the gate.  Set the corresponding pin to an analog input.

## ■ PROGRAMMING AND ERASING FLASH MEMORY ON THE MB89F217

### 1. Flash Memory

The flash memory is located between 8000$_H$ and FFFF$_H$ in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

### 2. Flash Memory Features
• 32 K byte × 8-bit configuration :  (16 K + 8 K + 8 K sectors)
• Automatic programming algorithm (Embedded algorithm* : Equivalent to MBM29LV200)
• Includes an erase pause and restart function
• Data polling and toggle bit for detection of program/erase completion
• Detection of program/erase completion via CPU interrupt
• Compatible with JEDEC-standard commands
• Sector Erasing (sectors can be combined in any combination)
• No. of program/erase cycles : 10,000 (Min)

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

### 3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

### 4. Flash Memory Register

• Control status register (FMCS)

| | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |
|---|---|---|---|---|---|---|---|---|---|
| Address 007A$_H$ | INTE | RDYINT | WE | RDY | Reserved | Reserved | – | Reserved | Initial value 0 0 0 X 0 0 - 0$_B$ |
| | R/W | R/W | R/W | R | R/W | R/W | – | R/W | |

### 5. Sector Configuration

The table below shows the sector configuration of flash memory and lists the address of each sector for both during CPU access a flash memory programming.
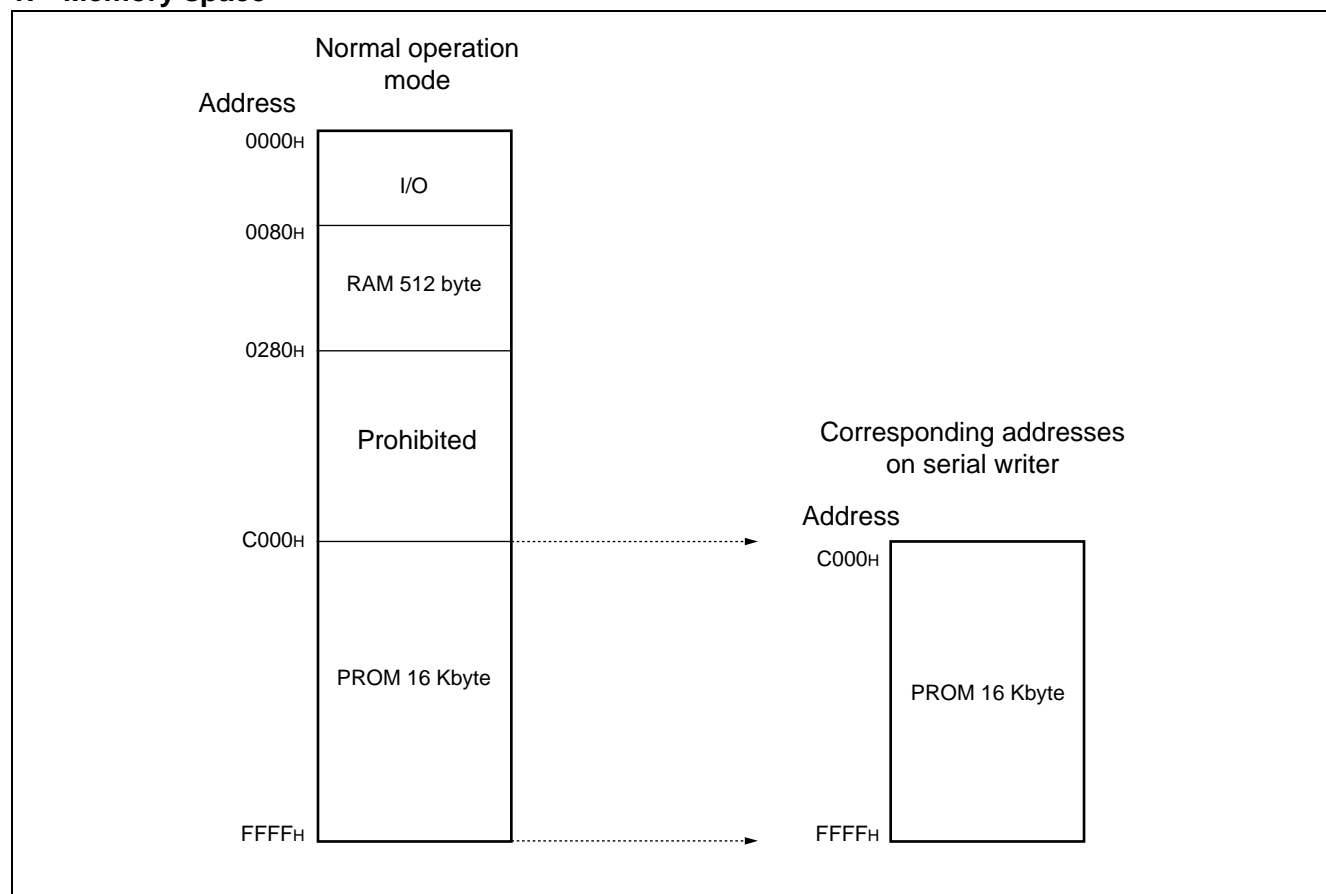
• Sector configuration of flash memory

| FLASH Memory | CPU Address | Programming Address* |
|---|---|---|
| 16 K bytes | FFFF$_H$ to C000$_H$ | 1FFFF$_H$ to 1C000$_H$ |
| 8 K bytes | BFFF$_H$ to A000$_H$ | 1BFFF$_H$ to 1A000$_H$ |
| 8 K bytes | 9FFF$_H$ to 8000$_H$ | 19FFF$_H$ to 18000$_H$ |

* : The programmer address is the address to be used instead of the CPU address when programming data from a parallel flash memory programmer. Use the programmer address on programming or erasing using a general-purpose parallel programmer.

## ■ PROGRAMMING TO OTPROM ON THE MB89P215

### 1.   Memory space

```
                    Normal operation
                         mode
      Address
    0000H  ┌──────────────┐
           │      I/O      │
    0080H  ├──────────────┤
           │              │
           │ RAM 512 byte │
    0280H  ├──────────────┤
           │              │              Corresponding addresses
           │              │                 on serial writer
           │  Prohibited  │
           │              │                 Address
    C000H  ├──────────────┤ ·········▸   C000H  ┌──────────────┐
           │              │                      │              │
           │              │                      │              │
           │              │                      │              │
           │ PROM 16 Kbyte│                      │ PROM 16 Kbyte│
           │              │                      │              │
           │              │                      │              │
           │              │                      │              │
    FFFFH  └──────────────┘ ·········▸   FFFFH  └──────────────┘
```

### 2.   Programming to the OTPROM

To program to the OTPROM using an EPROM programmer AF220/AF210/AF120/AF110 (manufacturer : Yokoga-wa Digital Computer Corp.).

Inquiry : Yokogawa Digital Computer Corp. : TEL(81)-42-333-6224

Note : Programming to the OTPROM with MB89P215 is serial programming mode only.

### 3.   Programming Adaptor for OTPROM

To program to the OTPROM using an EPROM programmer  AF220/AF210/AF120/AF110, use the programming adapter (manufacturer : Sunhayato Corp.) listed below.

Adaptor socket : ROM3-FPT30M02-8L3

Inquiry : Sunhayato Corp. :     TEL     : (81)-3-3984-7791
                                FAX     : (81)-3-3971-0535
                                E-mail  : adapter@sunhayato.co.jp

### 4.   Programming yields

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature.

For this reason, a programming yield of 100% cannot be assured at all times.

## ■ EPROM WRITING TO PIGGY-BACK/EVALUATION CHIPS

### 1.  EPROM model

MBM27C256A-20TVM

### 2.  Writer adapter

For writing to EPROM using a ROM writer, use one of the writer adapters shown below (manufactured by Sunhayato) .

| Package | Adapter socket model |
|---------|---------------------|
| LCC-32 | ROM-32LC-28DP-S |

Inquiries should be addressed to Sunhayato Corp.  :  TEL    : (81)-3-3984-7791
FAX    : (81)-3-3971-0535
E-mail : adapter@sunhayato.co.jp

### 3.  Memory space

Shown below the memory space in each mode.
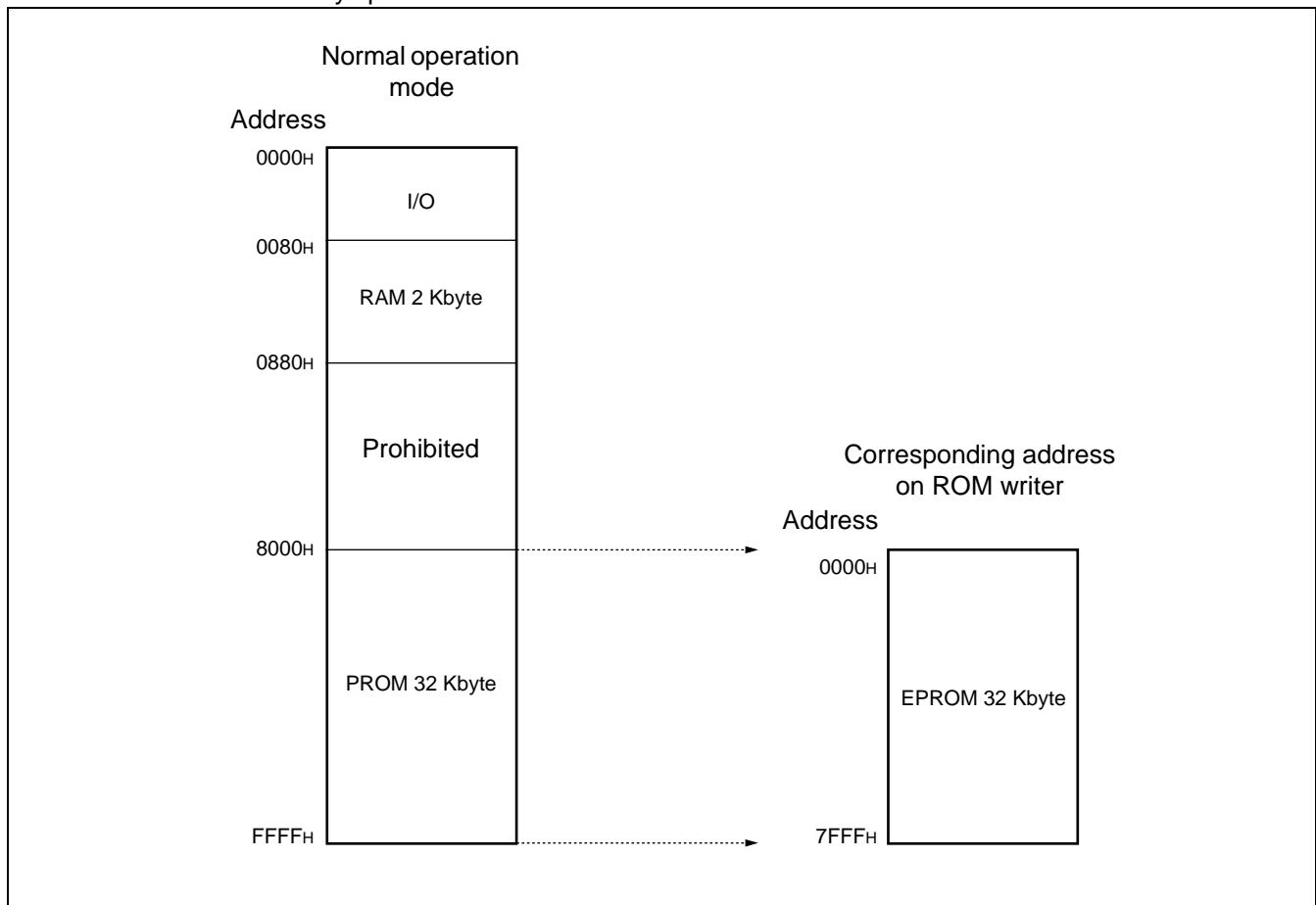


### 4.  Writing to EPROM

(1) Set up the EPROM writer for the MBM27C256A.

(2) Load program data on to the EPROM programmer at $0000_H$ to $7FFF_H$.

(3) Program $0000_H$ to $7FFF_H$ with the EPROM programmer.

■ **BLOCK DIAGRAM**
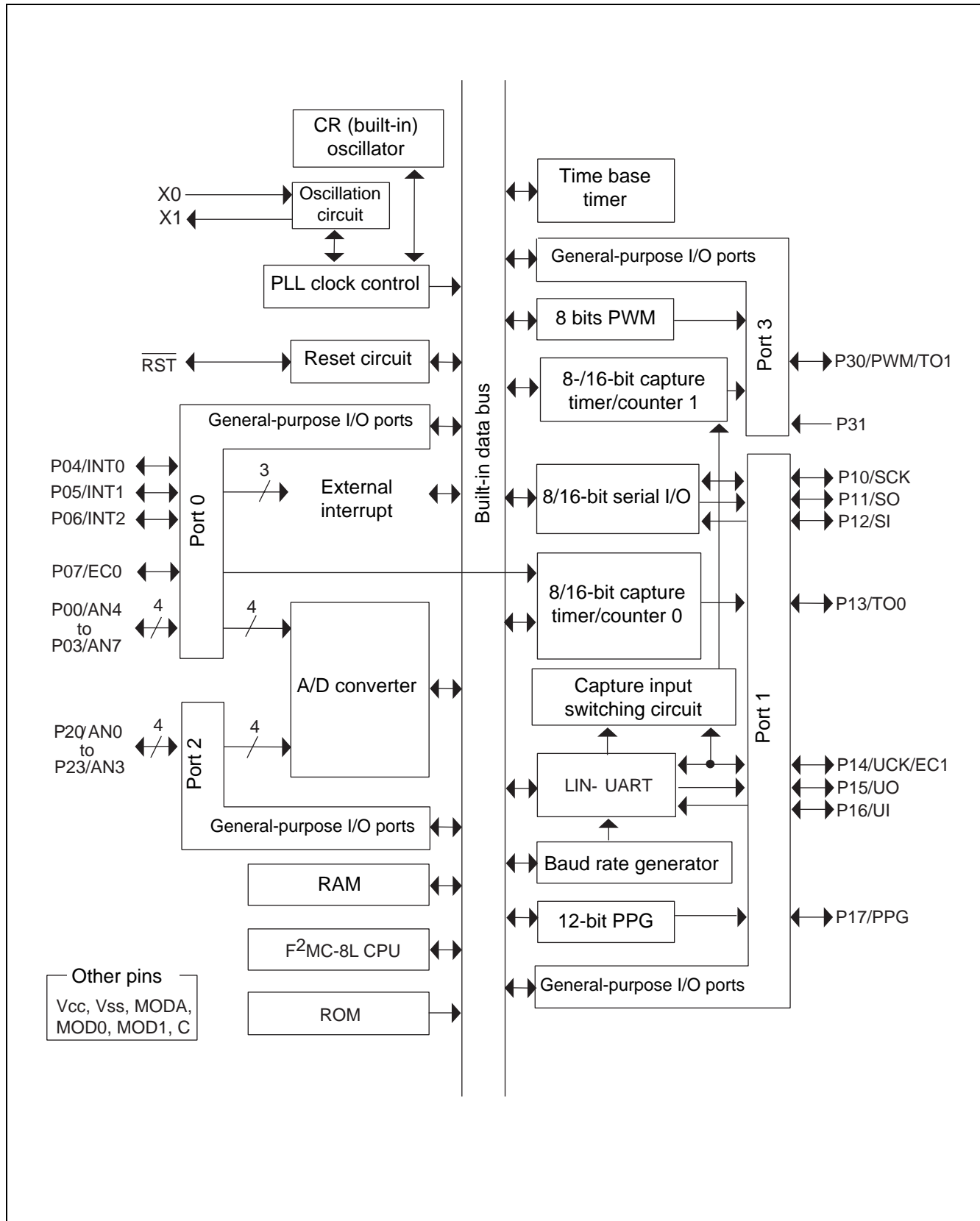
## ■ CPU CORE

### 1. Memory space

The MB89210 series has 64 KB of memory space, containing all I/O, data areas, and program areas. The I/O area is located at the lowest addresses, with the data area placed immediately above. The data area can be partitioned into register areas, stack areas, or direct access areas depending on the application. The program area is located at the opposite end of memory, closest to the highest addresses, and the highest part of this area is assigned to the tables of interrupt and reset vectors and vector call instructions. The following diagram shows the structure of memory space in the MB89210 series.
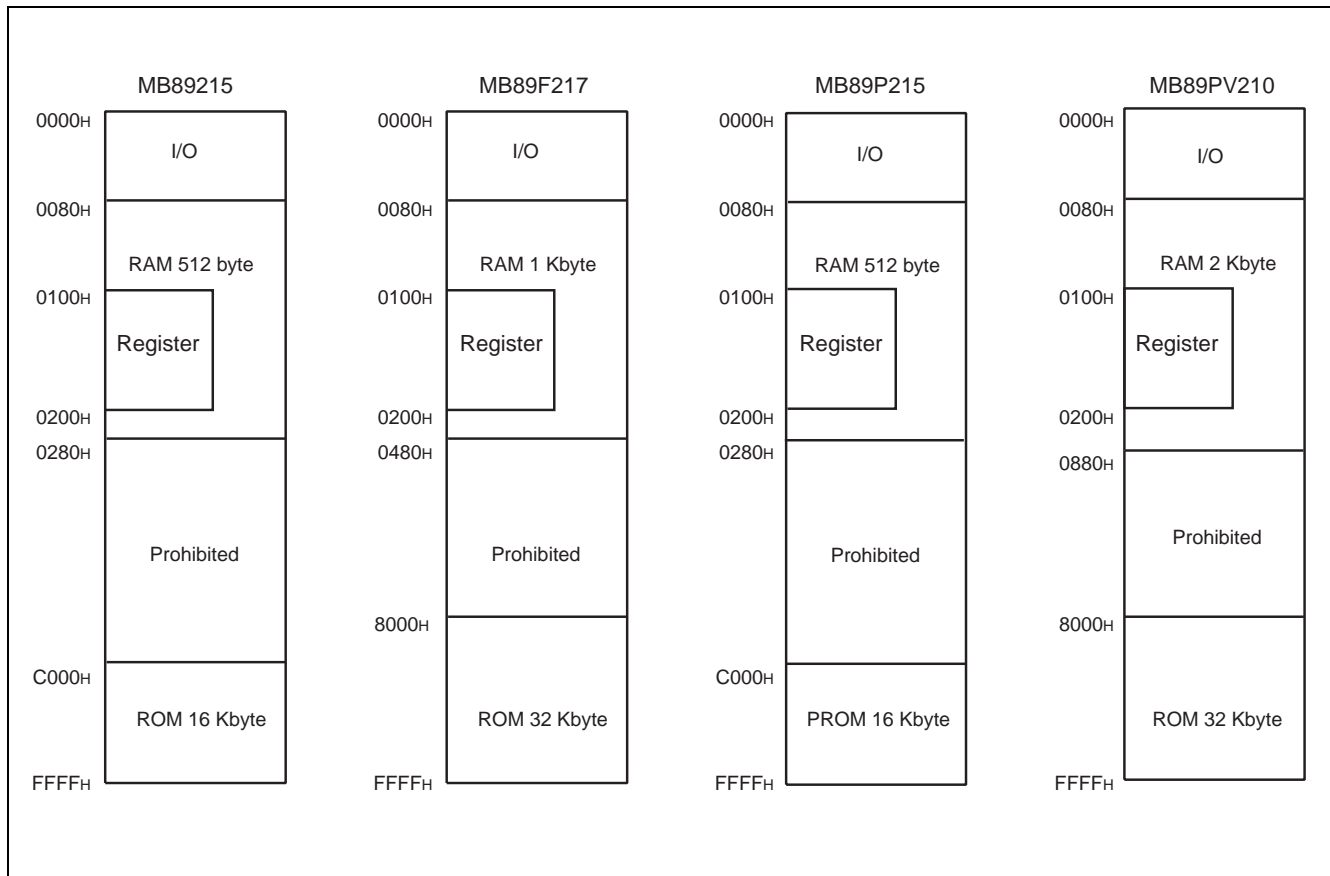
## 2. Register

The MB89210 series has two types of registers; the registers dedicated to specific purposes in the CPU and the general-purpose registers. The dedicated registers are as follows:

Program counter (PC)      : 16-bit length, shows the locations where instructions are stored.
Accumulator (A)       : 16-bit length, a temporary memory register for calculation operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
Temporary accumulator (T)  : 16-bit length, performs calculations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
Index register (IX)      : 16-bit length, a register for index modification.
Extra pointer (EP)      : 16-bit length, apointer indicating memory addresses.
Stack pointer (SP)      : 16-bit length, indicates stack areas.
Program status (PS)     : 16-bit length, contains register pointer and condition code.

```
        16 bits
  ┌──────────────┐                                        Initial value
  │      PC      │   : Program counter                      FFFD_H
  └──────────────┘
  ┌──────────────┐
  │      A       │   : Accumulator                        Indeterminate
  └──────────────┘
  ┌──────────────┐
  │      T       │   : Temporary accumulator              Indeterminate
  └──────────────┘
  ┌──────────────┐
  │      IX      │   : Index register                     Indeterminate
  └──────────────┘
  ┌──────────────┐
  │      EP      │   : Extra pointer                      Indeterminate
  └──────────────┘
  ┌──────────────┐
  │      SP      │   : Stack pointer                      Indeterminate
  └──────────────┘
  ┌──────┬───────┐
  │  RP  │  CCR  │   : Program status                     I-flag = 0, IL1, 0 = 11
  └──────┴───────┘                                        Initial values for other bits are
       PS                                                 indeterminate.
```
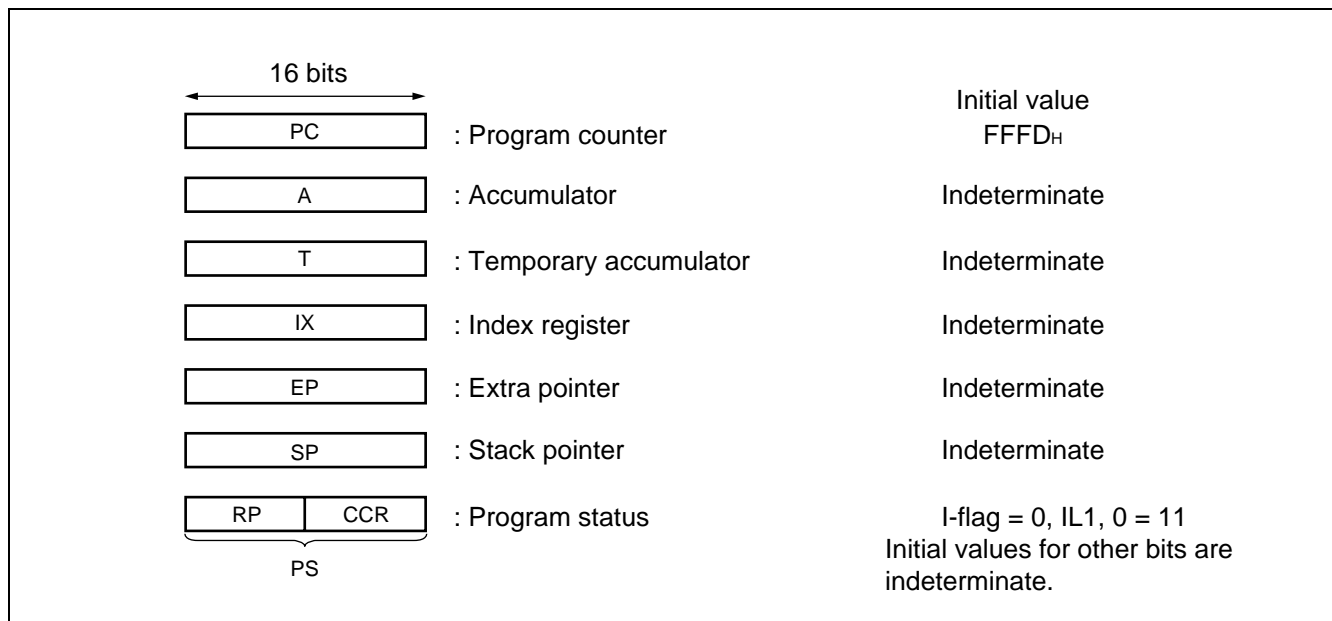
The PS register can further be divided into the register bank pointer in the higher 8 bits (RP) and the condition code register in the lower 8 bits (CCR). (See the diagram below.)

| | RP | | | | | | | | CCR | | | | | | | | CCR initial value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |
| PS | R4 | R3 | R2 | R1 | R0 | – | – | – | H | I | IL1 | IL0 | N | Z | V | C | X011XXXX$_B$ |

H-flag

I-flag

Interrupt level bit

N-flag

0-flag

V-flag

C-flag
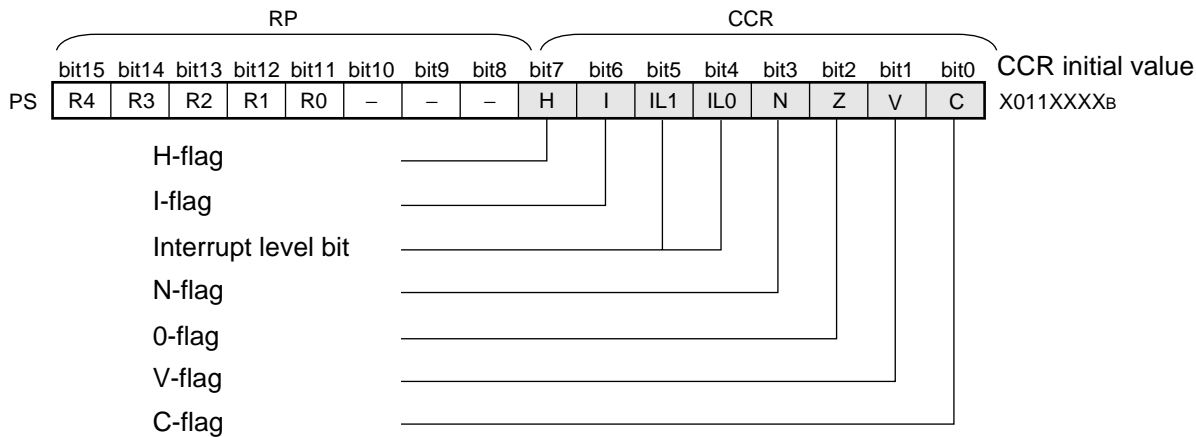
X : Undefined

The RP points to the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule shown next.

Rule for Conversion of Actual Addresses in the General-purpose Register Area

RP higher bits    OP code lower bits

"0"  "0"  "0"  "0"  "0"  "0"  "0"  "1"  | R4  R3  R2  R1  R0 : b2  b1  b0 |

Generated address  | A15  A14  A13  A12  A11  A10  A9  A8  A7  A6  A5  A4  A3  A2  A1  A0 |
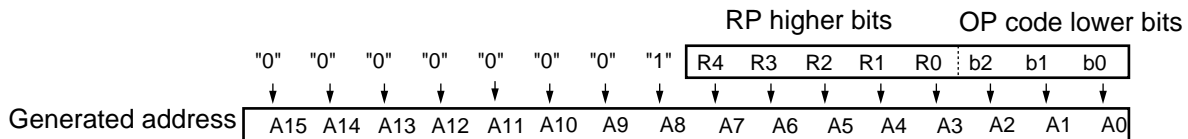
The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at the time of an interrupt.

H flag : Set to 1 if calculations result in carry operations from bit 3 to bit 4 or borrow operations from bit 4 to bit 3, otherwise set to 0.
The flag is for decimal adjustment instructions; do not use for other than additions and subtractions.

I flag : This flag is set to 1 if interrupts are enabled, and 0 if interrupts are prohibited. The default value at reset is 0.

IL1, 0 : Indicates the level of the interrupt currently enabled.
An interrupt is processed only if its level is higher than the value this bit indicates.

| IL1 | IL0 | Interrupt level | High-low |
|-----|-----|-----------------|----------|
| 0 | 0 | 1 | Higher |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | Lower = no interruption |

N flag : Set to 1 if the highest bit is 1 after a calculation, otherwise cleared to 0.
Z flag : Set to 1 if a calculation result is 0, otherwise cleared to 0.
V flag : Set to 1 if a 2's complement overflow results during a calculation, otherwise cleared to 0.
C flag : Set to 1 if a calculation results in a carry or borrow operation from bit 7, otherwise cleared to 0.
This is also the shift-out value in a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit length, data storage registers

The general-purpose registers are 8 bits in length and located in the register banks in the memory. One bank contains eight registers and the MB89210 series allow a total of 16 banks to be used at maximum.

The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration

This address = 0100H + 8 x (RP)

| R0 |
| R1 |
| R2 |
| R3 |
| R4 |
| R5 |
| R6 |
| R7 |

16 banks

Memory area
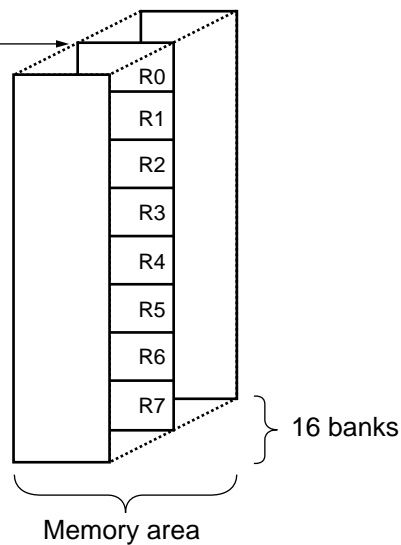
## ■ I/O MAP

| Address | Register name | Register description | Read/write | Initial value |
|---|---|---|---|---|
| 0000H | PDR0 | Port 0 data register | R/W | XXXXXXXX |
| 0001H | DDR0 | Port 0 direction register | R/W | 0 0 0 0 0 0 0 0 |
| 0002H to 0006H | | Access prohibited | | |
| 0007H | SYCC | System clock control register | R/W | 1 – – 1 1 1 0 0 |
| 0008H | STBC | Standby control register | R/W | 0 0 0 1 0 – – – |
| 0009H | WDTC | Watchdog timer control register | W | 0 – – –XXXX |
| 000AH | TBTC | Time base timer control register | R/W | 0 0 – – – 0 0 0 |
| 000BH | | Access prohibited | | |
| 000CH | PDR1 | Port 1 data register | R/W | XXXXXXXX |
| 000DH | DDR1 | Port 1 direction register | R/W | 0 0 0 0 0 0 0 0 |
| 000EH | RSFR | Reset flag register | R | XXXX – – – – |
| 000FH | PDR2 | Port 2 data register | R/W | – – – – XXXX |
| 0010H | DDR2 | Port 2 direction register | R/W | – – – – 0 0 0 0 |
| 0011H | | Access prohibited | | |
| 0012H | PDR3 | Port 3 data register | R/W | – – – – – – XX |
| 0013H | DDR3 | Port 3 direction register | R/W | – – – – – – – 0 |
| 0014H | RCR21 | 12-bit PPG control register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 0015H | RCR22 | 12-bit PPG control register 2 | R/W | – – 0 0 0 0 0 0 |
| 0016H | RCR23 | 12-bit PPG control register 3 | R/W | 0 – 0 0 0 0 0 0 |
| 0017H | RCR24 | 12-bit PPG control register 4 | R/W | – – 0 0 0 0 0 0 |
| 0018H | | Access prohibited | | |
| 0019H | TCCR0 | Capture control register 0 | R/W | 0 0 0 0 0 0 0 0 |
| 001AH | TCR10 | Timer 1 control register 0 | R/W | 0 0 0 – 0 0 0 0 |
| 001BH | TCR00 | Timer 0 control register 0 | R/W | 0 0 0 0 0 0 0 0 |
| 001CH | TDR10 | Timer 1 Data 0 | R/W | XXXXXXXX |
| 001DH | TDR00 | Timer 0 Data 0 | R/W | XXXXXXXX |
| 001EH | TCPH0 | Capture data register H 0 | R | XXXXXXXX |
| 001FH | TCPL0 | Capture data register L 0 | R | XXXXXXXX |
| 0020H | TCR20 | Timer output control 0 | R/W | – – – – – – 0 0 |
| 0021H | | Access prohibited | | |
| 0022H | CNTR | PWM control register | R/W | 0 – 0 0 0 0 0 0 |
| 0023H | COMR | PWM Compare register | W | XXXXXXXX |
| 0024H | EIC1 | External interrupt control register 1 (edge) | R/W | 0 0 0 0 0 0 0 0 |
| 0025H | EIC2 | External interrupt control register 2 (edge) | R/W | 0 0 0 0 0 0 0 0 |

*(Continued)*

| Address | Register name | Register description | Read/write | Initial value |
|---|---|---|---|---|
| 0026H | | Access prohibited | | |
| 0027H | | | | |
| 0028H | SCR | Serial control register | R/W | 0 0 0 0 0 0 0 0 |
| 0029H | USMR | LIN-UART serial mode register | R/W | 0 0 0 0 0 0 0 0 |
| 002AH | SSR | Serial status register | R/W | 0 0 0 0 1 0 0 0 |
| 002BH | RDR | Recieving data register | R | 0 0 0 0 0 0 0 0 |
| | TDR | Sending data register | W | 1 1 1 1 1 1 1 1 |
| 002CH | ESCR | Extended status control register | R/W | 0 0 0 0 0 X 0 0 |
| 002DH | ECCR | Extended communication control register | R/W | 0 0 0 0 0 − 1 1 |
| 002EH | BGRH | Baud rate generator register H | R/W | − 0 0 0 0 0 0 0 |
| 002FH | BGRL | Baud rate generator register L | R/W | 0 0 0 0 0 0 0 0 |
| 0030H | ADC1 | A/D control register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 0031H | ADC2 | A/D control register 2 | R/W | 0 0 0 0 0 0 0 1 |
| 0032H | ADDH | A/D data register H | R/W | 0 0 0 0 0 0 XX |
| 0033H | ADDL | A/D data register L | R/W | XXXXXXXX |
| 0034H | ADEN | A/D enable register | R/W | 0 0 0 0 0 0 0 0 |
| 0035H to 0038H | | Access prohibited | | |
| 0039H | SMR | Serial mode register | R/W | 0 0 0 0 0 0 0 0 |
| 003AH | SDR | Serial Data register | R/W | XXXXXXXX |
| 003BH to 0040H | | Access prohibited | | |
| 0041H | TCCR1 | Capture control register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 0042H | TCR11 | Timer 1 control register 1 | R/W | 0 0 0 − 0 0 0 0 |
| 0043H | TCR01 | Timer 0 control register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 0044H | TDR11 | Timer 1 Data register 1 | R/W | XXXXXXXX |
| 0045H | TDR01 | Timer 0 Data register 1 | R/W | XXXXXXXX |
| 0046H | TCPH1 | Capture status register H1 | R | XXXXXXXX |
| 0047H | TCPL1 | Capture status register L1 | R | XXXXXXXX |
| 0048H | TCR21 | Timer output control register 1 | R/W | − − − − − − 0 0 |
| 0049H | TCSL | Capture input select register | R/W | − − − − − − − 0 |
| 004AH to 005FH | | Access prohibited | | |
| 0060H | XCRS* | External/CR(built-in)oscillation clock control register | R/W | 0 0 − 0 0 0 1 0 |
| 0061H to 006FH | | Access prohibited | | |

*(Continued)*

*(Continued)*

| Address | Register name | Register description | Read/write | Initial value |
|---|---|---|---|---|
| 0070$_H$ | PUL0 | Port 0 pull-up setting register | R/W | 0 0 0 0 0 0 0 0 |
| 0071$_H$ | PUL1 | Port 1 pull-up setting register | R/W | 0 0 0 0 0 0 0 0 |
| 0072$_H$ | PUL2 | Port 2 pull-up setting register | R/W | – – – – 0 0 0 0 |
| 0073$_H$ | PUL3 | Port 3 pull-up setting register | R/W | – – – – – – – 0 |
| 0074$_H$ to 0079$_H$ | | Access prohibited | | |
| 007A$_H$ | FMCS | Flash memory control status register | R/W | 0 0 0 0 0 0 – 0 |
| 007B$_H$ | ILR1 | Interrupt level setting register 1 | W | 1 1 1 1 1 1 1 1 |
| 007C$_H$ | ILR2 | Interrupt level setting register 2 | W | 1 1 1 1 1 1 1 1 |
| 007D$_H$ | ILR3 | Interrupt level setting register 3 | W | 1 1 1 1 1 1 1 1 |
| 007E$_H$ | ILR4 | Interrupt level setting register 3 | W | 1 1 1 1 1 1 1 1 |
| 007F$_H$ | | Access prohibited | | |

* : Only for MB89215, MB89F217, MB89P215

Description of write/read symbols :

    R/W : Read/write enabled
    R : Read only
    W : Write only

Description of initial values

    0 : This bit initialized to "0".
    1 : This bit initialized to "1".
    X : The initial value of this bit is undefined.
    - : This bit is not defined.

Note : If a bit manipulation instruction accesses the serial mode register (SMR), a write-only register, or a register containing a write-only bit, the bit focused on by the instruction is set to a prescribed value but a malfunction occurs when the other bits contains a write-only bit.  Do not use bit manipulation instructions to access such registers.

# MB89210 Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating Min | Rating Max | Unit | Remarks |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | |
| Input voltage | $V_I$ | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | *2 |
| Output voltage | $V_O$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | |
| Maximum clamp current | $I_{CLAMP}$ | $- 0.4$ | $+ 0.4$ | mA | *1 |
| Maximum clamp total current | $\Sigma|I_{CLAMP}|$ | — | 10 | mA | *1 |
| "L" level output current | $I_{OL}$ | — | 10 | mA | |
| "L" level average current | $I_{OLAV}$ | — | 4 | mA | Average value (operating current $\times$ operating duty) |
| "L" level total output current | $\Sigma I_{OL}$ | — | 50 | mA | |
| "H" level output current | $I_{OH}$ | — | $- 10$ | mA | |
| "H" level average current | $I_{OHAV}$ | — | $- 4$ | mA | Average value (operating current $\times$ operating duty) |
| "H" level total output current | $\Sigma I_{OH}$ | — | $- 50$ | mA | |
| Power consumption | Pd | — | 200 | mW | MB89215, MB89P215 |
| | | — | 300 | mW | MB89F217 |
| Storage temperature | Tstg | $- 55$ | $+ 150$ | °C | |

*1 : • Applicable to pins : P00 to P07, P10 to P17, P20 to P23, P30 to P31
 • Use within recommended operating conditions.
 • Use at DC voltage (current) .
 • The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
 • The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 • Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
 • Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
 • Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
 • Care must be taken not to leave the +B input pin open.
 • Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.

*(Continued)*

*(Continued)*
- Sample recommended circuits :

- Input/Output Equivalent circuits

Protective diode

Limiting
resistance

+B input (0 V to 16 V)

$V_{CC}$

P-ch

N-ch

R
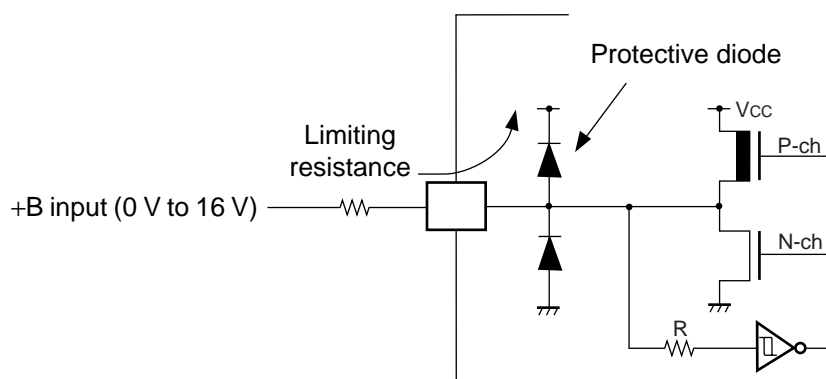
*2 : If the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

WARNING:   Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2.  Recommended Operating Conditions

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | 3.5 | 5.5 | V | Normal Operation Assurance Range |
| | | 3.0 | 5.5 | V | RAM status in stop mode |
| Input "H" voltage | $V_{IH}$ | 0.7 $V_{CC}$ | $V_{CC}$ + 0.3 | V | P31,UI |
| | $V_{IHS}$ | 0.8 $V_{CC}$ | $V_{CC}$ + 0.3 | V | MODA, MOD0, MOD1, $\overline{RST}$, P00 to P07, P10 to P17, P20 to P23, P30, INT0 to INT2, EC0, EC1, SCK, SI, UCK |
| Input "L" voltage | $V_{IL}$ | $V_{SS}$ – 0.3 | 0.3 $V_{CC}$ | V | P31,UI |
| | $V_{ILS}$ | $V_{SS}$ – 0.3 | 0.2 $V_{CC}$ | V | MODA, MOD0, MOD1, $\overline{RST}$, P00 to P07, P10 to P17, P20 to P23, P30, INT0 to INT2, EC0, EC1, SCK, SI, UCK |
| Operating temperature | Ta | – 40 | + 105 | °C | |
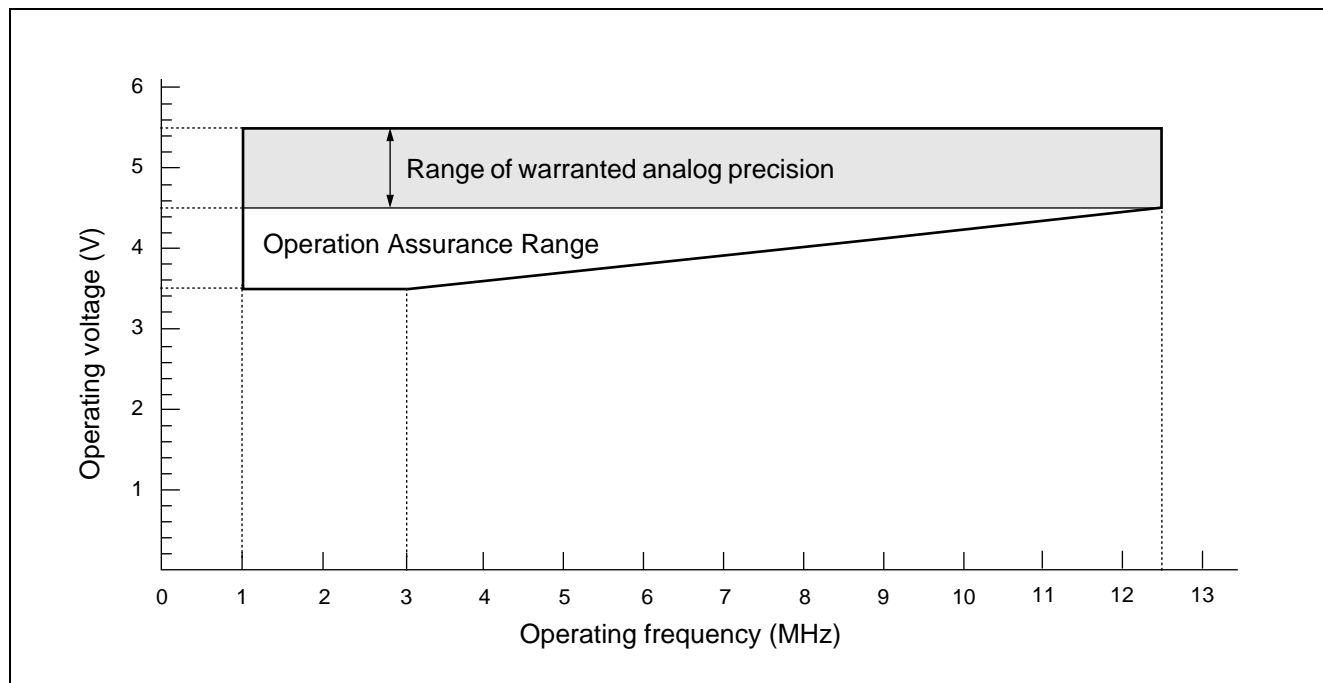


WARNING:  The recommended operating conditions are required in order to ensure the normal operation of  the semiconductor device.  All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

$(V_{CC} = 5.0 \text{ V} \pm 10\%, V_{SS} = 0.0 \text{ V}, F_{CH} = 10 \text{ MHz (external clock)}, Ta = -40 \text{ °C to } +105 \text{ °C})$

| Parameter | Symbol | Pin name | Condition | Value Min | Value Typ | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| "H" level input voltage | $V_{IH}$ | P31,UI | — | $0.7 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| | $V_{IHS}$ | MODA, MOD0, MOD1, $\overline{RST}$, P00 to P07, P10 to P17,P20 to P23, P30, INT0 to INT2, EC0, EC1, SCK, SI, UCK | — | $0.8 V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| "L" level input voltage | $V_{IL}$ | P31,UI | — | $V_{SS} - 0.3$ | — | $0.3 V_{CC}$ | V | |
| | $V_{ILS}$ | MODA, MOD0, MOD1, $\overline{RST}$, P00 to P07, P10 to P17,P20 to P23, P30, INT0 to INT2, EC0, EC1, SCK, SI, UCK | — | $V_{SS}-0.3$ | — | $0.2 V_{CC}$ | V | |
| "H" level output voltage | $V_{OH}$ | P00 to P07, P10 to P17, P20 to P23, P30 | $Vcc = 4.5$ V, $I_{OH} = -4.0$ mA | $V_{CC} - 0.5$ | — | — | V | |
| "L" level output voltage | $V_{OL}$ | P00 to P07, P10 to P17, P20 to P23, P30, $\overline{RST}$ | $Vcc = 4.5$ V, $I_{OL} = 4.0$ mA | — | — | 0.4 | V | |
| Input leak current | $I_{LI}$ | P00 to P07, P10 to P17, P20 to P23, P30, P31, MODA, MOD0, MOD1 | $0.45 \text{ V} < V_I < V_{CC}$ | — | — | $\pm 5$ | $\mu$A | Without pull-up resistance specified |
| Pullup resistance | $R_{PULL}$ | P00 to P07,P10 to P17, P20 to P23, P30, $\overline{RST}$ | $V_I = 0.0$ V | 25 | 50 | 100 | k$\Omega$ | |
| Power supply current | $I_{CC}$ | $V_{CC}$ — At normal operating (External clock, Max gear speed) | When A/D convereter stops | — | 8 | 12 | mA | MB89215 |
| | | | | — | 6 | 10 | mA | MB89F217 |
| | | | | — | 6 | 9 | mA | MB89P215 |
| | | | When A/D convereter starts | — | 10 | 15 | mA | MB89215 |
| | | | | — | 8 | 13 | mA | MB89F217 |
| | | | | — | 8 | 12 | mA | MB89P215 |
| | $I_{CCS}$ | at sleep mode (External clock, Max gear speed) | When A/D convereter stops | — | 4 | 6 | mA | MB89215 |
| | | | | — | 3 | 5 | mA | MB89F217, MB89P215 |
| | $I_{CCH}$ | At stop mode Ta = +25 °C (External clock) | When A/D convereter stops | — | — | 1 | $\mu$A | MB89215 |
| | | | | — | — | 10 | $\mu$A | MB89F217, MB89P215 |
| Input capacitance | $C_{IN}$ | Other than $V_{CC}$ and $V_{SS}$ | — | — | 5 | 15 | pF | MB89F217, MB89P215 |

## 4. AC Characteristics

### (1) Reset Timing

(Vss = 0.0 V, Ta = −40 °C to +105 °C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $\overline{RST}$ "L" level pulse width | $t_{ZLZH}$ | — | 48 $t_{HCYL}$* | — | ns | |

* : $t_{HCYL}$ : Oscillation clock one cycle time
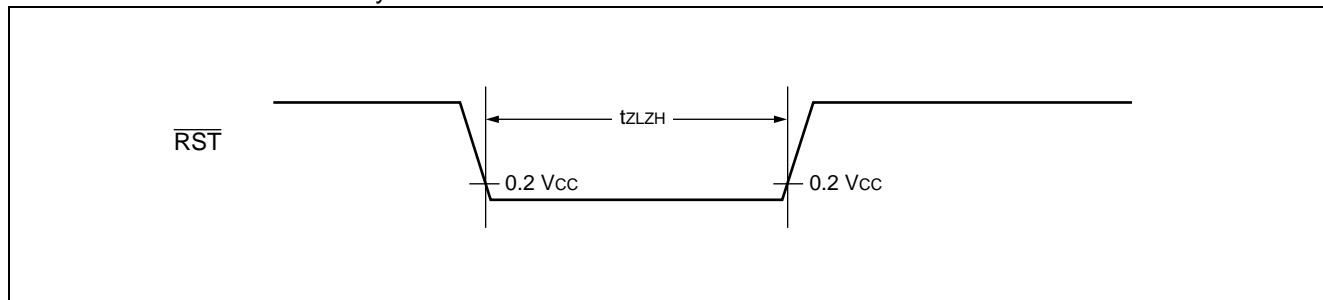


### (2) Power-on reset

(Vss = 0.0 V, Ta = −40 °C to +105 °C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power on time | $t_R$ | — | — | 50 | ms | |
| Power shutoff time | $t_{OFF}$ | — | 1 | — | ms | For repeated operation |
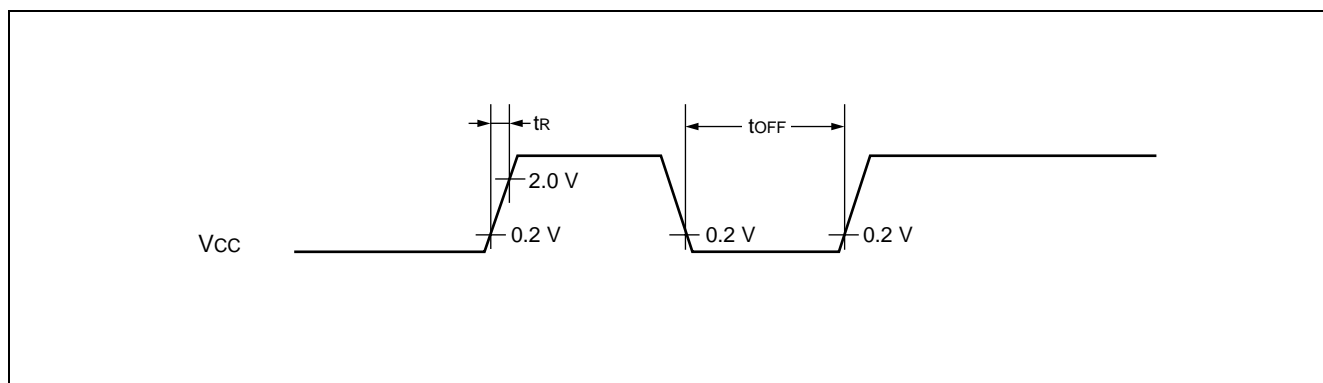


Note : The supply voltage must be set to minimum value required for operation within the prescribed default oscillation setting time.

### (3) Clock Timing

(Vss = 0.0 V, Ta = −40 °C to +105 °C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Clock frequency | $F_{CH-1}$ | Crystal or ceramic oscillation | 1 | 12.5 | MHz | |
| Clock cycle time | $t_{XCYL}$ | | 80 | 1000 | ns | |
| Input clock pulse width | $t_{WH}$ $t_{WL}$ | | 20 | — | ns | |
| Input clock rise, fall time | $t_{CR}$ $t_{CF}$ | | — | 10 | ns | |
| Oscillation frequency | $F_{CH-2}$ | CR(built-in) oscillator | 8.5 | 11.5 | MHz | |

• X0 and X1 Timing and application Conditions
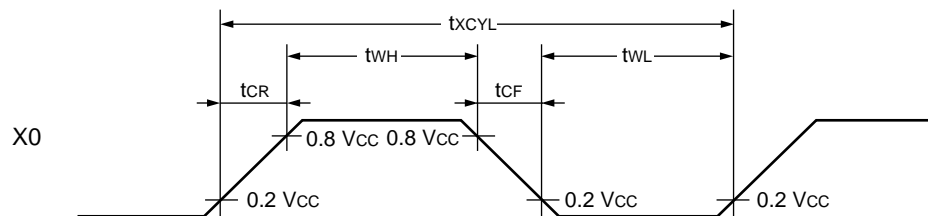


• Clock application Conditions

Using crystal oscillator
or
ceramic oscillator
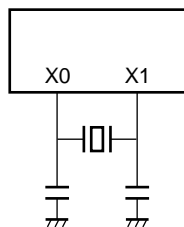
Using external clock
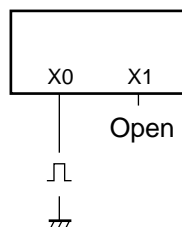
Using CR (built-in)
oscillator
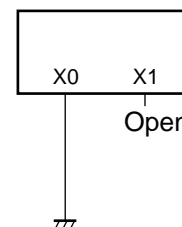


### (4) Instruction Cycle

(Vss = 0.0 V, Ta = −40 °C to +105 °C)

| Parameter | Symbol | Value | Unit | Remarks |
|---|---|---|---|---|
| Instruction cycle (instruction execution time) | $t_{INST}$ | 4/$F_{CH}$, 8/$F_{CH}$, 16/$F_{CH}$, 64/$F_{CH}$ | μs | When operating at $F_{CH}$ = 10 MHz $t_{INST}$ = 0.4 μs (4/$F_{CH}$) |

$F_{CH}$ : Oscillation frequency (Operating clock frequency after switching between external and CR (internal) oscillator clocks)

**(5) Recommended Resonator Manufactures**

• Sample application of ceramic resonator
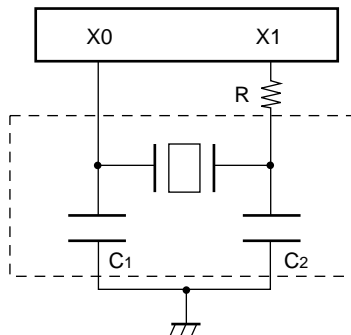


| Resonator manufacture | Resonator | Frequency (MHz) | $C_1$ | $C_2$ | R |
|---|---|---|---|---|---|
| Murata Mfg. Co., Ltd. | CSTLS4M00G56-B0 | 4.00 | built-in | built-in | 680 $\Omega$ |
| | CSTCR4M00G55-R0 | 4.00 | built-in | built-in | 680 $\Omega$ |
| | CSTLS8M00G53-B0 | 8.00 | built-in | built-in | — |
| | CSTCC8M00G53-R0 | 8.00 | built-in | built-in | — |
| | CSTLS10M0G53-B0 | 10.00 | built-in | built-in | — |
| | CSTCC10M00G53-R0 | 10.00 | built-in | built-in | — |

Inquiry :  • Murata Electronics North America Inc  : TEL +1-404-436-1300
          • Murata Europe Management GmbH     : TEL +49-911-66870
          • Murata Electronics Singapore (p/e)      : TEL +65-758-4233

**(6) Peripheral Input Timing**

$(V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ Ta = -40\ °C\ to\ +105\ °C)$

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Peripheral input "H" pulse width | $t_{ILIH}$ | INT0 to INT2, EC0, EC1 | $2\ t_{INST}$* | — | μs | |
| Peripheral input "L" pulse width | $t_{IHIL}$ | | $2\ t_{INST}$* | — | μs | |

*: For $t_{INST}$ see " (4) Instruction Cycle".
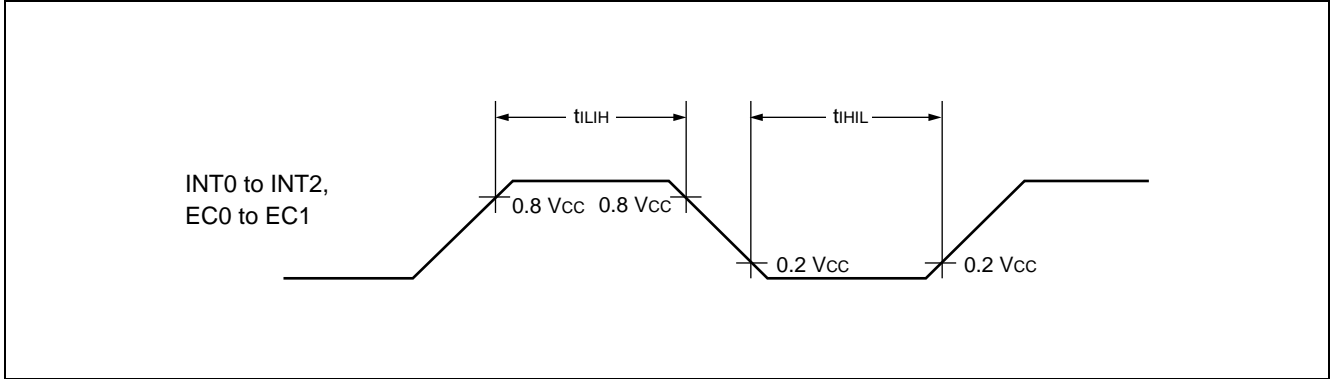
**(7) Serial I/O Timing**

(Vcc = 5.0 V ± 10%, Vss = 0.0 V, Ta = −40 °C to +105 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | **Min** | **Max** | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK | Internal clock operation | 2 $t_{INST}$* | — | μs | |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK, SO | | − 200 | 200 | ns | |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SCK, SI | | 0.5 $t_{INST}$* | — | μs | |
| SCK ↑ → Valid SI hold time | $t_{SHIX}$ | SCK, SI | | 0.5 $t_{INST}$* | — | μs | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK | External clock operation | $t_{INST}$* | — | μs | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK | | $t_{INST}$* | — | μs | |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK, SO | | 0 | 200 | ns | |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SCK, SI | | 0.5 $t_{INST}$* | — | μs | |
| SCK ↑ → Valid SI hold time | $t_{SHIX}$ | SCK, SI | | 0.5 $t_{INST}$* | — | μs | |

*: For $t_{INST}$ see " (4) Instruction Cycle".

- Internal shift clock mode
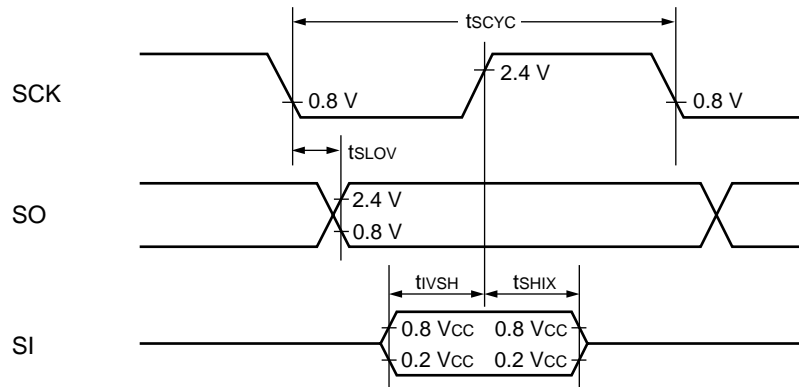
- External shift clock mode
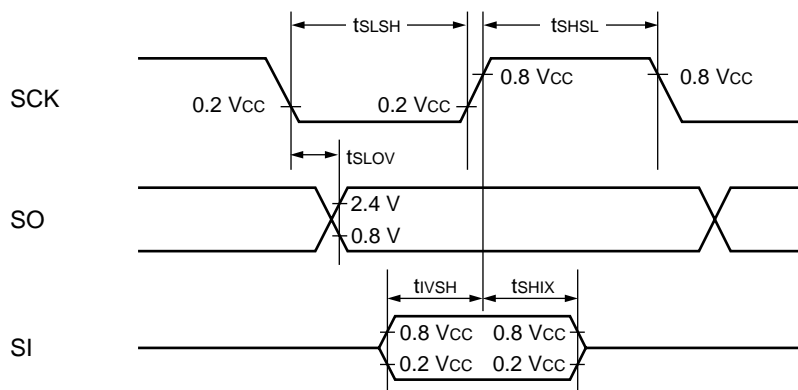
## (8) LIN-UART timing

$(V_{CC} = 5.0\ V \pm 10\%,\ V_{SS} = 0.0\ V,\ Ta = -40\ ^\circ C\ to +105\ ^\circ C)$

| Parameter | Symbol | Pin name | Condition | Value Min | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Serial clock cycle time | $t_{SCYC}$ | UCK | Internal clock operation | 2 $t_{INST}$* | — | μs | |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK, UO | | − 200 | 200 | ns | |
| Valid UI → UCK ↑ | $t_{IVSH}$ | UCK, UI | | 0.5 $t_{INST}$* | — | μs | |
| UCK ↑ → Valid UI hold time | $t_{SHIX}$ | UCK, UI | | 0 | — | μs | |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK, UO | | − 200 | 200 | ns | SCDE = 1 |
| UCK (delay) ↓ → UO time | $t_{SCLK}$ | UCK (delay), UO | | − 0.5 $t_{INST}$* | — | μs | SCDE = 1 |
| UCK ↓ → UCK (delay) ↓ | $t_{SDEL}$ | UCK, UCK (delay) | | 0.5 $t_{INST}$* | — | μs | SCDE = 1 |
| Serial clock "H" pulse width | $t_{SHSL}$ | UCK | External clock operation | 1.5 $t_{INST}$* | — | μs | |
| Serial clock "L" pulse width | $t_{SLSH}$ | UCK | | 1.5 $t_{INST}$* | — | μs | |
| UCK ↓ → UO time | $t_{SLOV}$ | UCK, UO | | $t_{INST}$* | — | μs | |
| Valid UI → UCK ↑ | $t_{IVSH}$ | UCK, UI | | 0 | — | μs | |
| UCK ↑ → Valid UI hold time | $t_{SHIX}$ | UCK, UI | | 0.5 $t_{INST}$* | — | μs | |

*: For $t_{INST}$ see " (4) Instruction Cycle".

• Internal shift clock mode
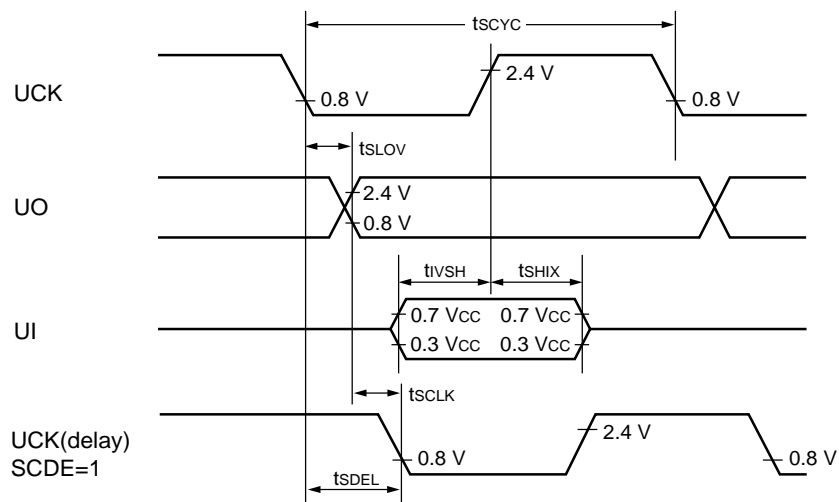


• External shift clock mode
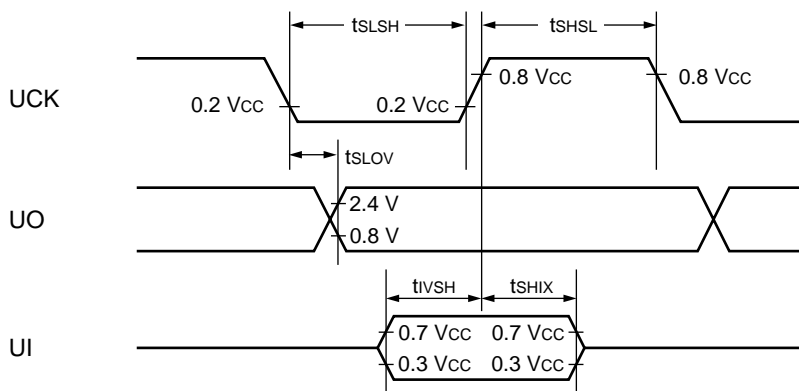
## 5. A/D Converter
### (1) A/D converter electrical characteristics

($V_{CC}$ = 5.0 V + 10%, $V_{SS}$ = 0.0 V, Ta = −40 °C to +105 °C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | bit | |
| Total error | | − 5.0 | — | + 5.0 | LSB | |
| Linearity error | | − 3.0 | — | + 3.0 | LSB | |
| Differential linear error | | − 2.5 | — | + 2.5 | LSB | |
| Zero transition voltage | $V_{OT}$ | $V_{SS}$ − 3.5 LSB | $V_{SS}$ + 0.5 LSB | $V_{SS}$ + 4.5 LSB | V | |
| Full-scale transition voltage | $V_{FST}$ | $V_{CC}$ − 6.5 LSB | $V_{CC}$ − 1.5 LSB | $V_{CC}$ + 2.0 LSB | V | |
| A/D mode conversion time | — | — | — | 38 $t_{INST}$* | μs | |
| Analog input current | $I_{AIN}$ | — | — | 10 | μA | |
| Analog input voltage range | — | 0 | — | $V_{CC}$ | V | |

* : For $t_{INST}$ see " (4) Instruction Cycle" in "4. AC Characteristics".

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## (2) Definition of A/D Converter Terms

* Resolution

  The level of analog variation that can be distinguished by the A/D converter.

  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

* Linear error (Unit : LSB)

  The deviation between the value along a straight line connecting the zero transition point("00 0000 0000"$\leftarrow\rightarrow$"00 0000 0001") of a device and the full-scale transition point ("11 1111 1111"$\leftarrow\rightarrow$"11 1111 1110"), compared with the actual conversion values obtained.

* Differential linear error (Unit : LSB)

  Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

* Total error (Unit : LSB)

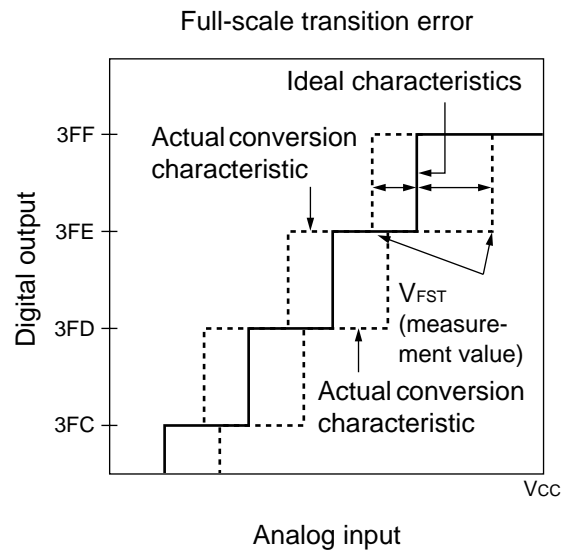  The difference between theoretical conversion value and actual conversion value.
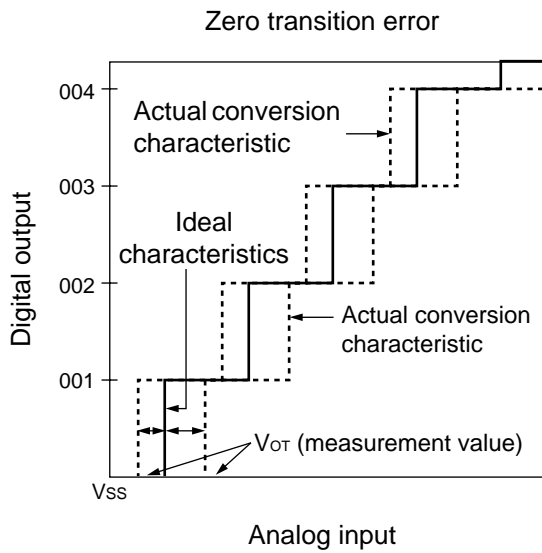


Ideal I/O characteristics    Total error
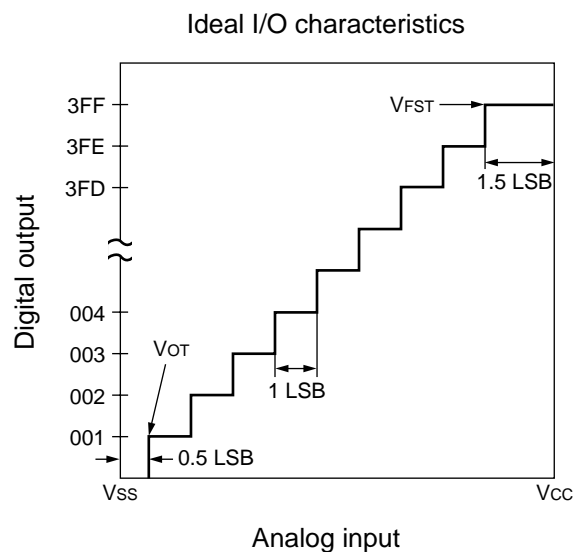
$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\quad (V)$$
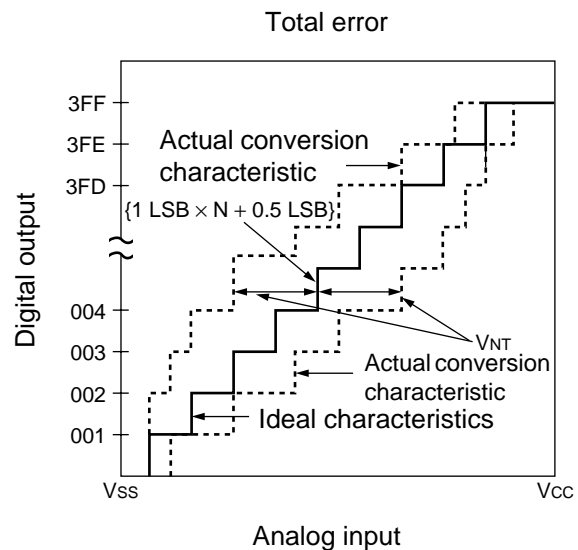
$$\text{Total error in digital output N} = \frac{V_{NT} - \{1\ LSB \times N + 0.5\ LSB\}}{1\ LSB}$$

*(Continued)*

*(Continued)*

### Zero transition error

Digital output

004 — Actual conversion characteristic

003 —

002 — Ideal characteristics

Actual conversion characteristic

001 —

$V_{OT}$ (measurement value)

Vss

Analog input

### Full-scale transition error

Ideal characteristics

Digital output

3FF — Actual conversion characteristic

3FE —

$V_{FST}$ (measurement value)

3FD —

Actual conversion characteristic

3FC —

Vcc

Analog input

### Linearity error

Digital output

Actual conversion characteristic

3FF —
3FE —
3FD — {1 LSB × $V_{OT}$}

$V_{FST}$ (measurement value)

$V_{NT}$

004 —
003 — Actual conversion characteristic

002 — Ideal characteristics
001 —

$V_{OT}$ (measurement value)

Vss                    Vcc

Analog input

### Differential linear error

Ideal characteristics

Digital output

N + 1 — Actual conversion characteristic

$V_{(N+1)T}$

N —

N − 1 — $V_{NT}$

N − 2 — Actual conversion characteristic

Vss                    Vcc

Analog input

$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

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### (3) Precautionary Information of A/D conversion

• Input Impedance of Analog Input Pins

The A/D converter has a sample & hold circuit as shown below, which uses a sample-and-hold capacitor to obtain the voltage at the analog input pin for 16 instruction cycles following the start of A/D conversion. For this reason if the external circuits providing the analog input signal have high output impedance, the analog input voltage may not stabilize within the analog input sampling time. It is therefore recommended that the output impedance of external circuits be reduced to 4 k$\Omega$ or less.

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 $\mu$F for the analog input pin.

Analog input equivalent circuit

Sample-and-hold circuit

Analog input pin

Comparator

R    C

If analog input impedance is 4 k$\Omega$ or more, the use of a capacitor of approximately 0.1 $\mu$F is recommended.

Closes 16 instruction cycles after the start of A/D conversion

Analog channel selector

MB89215        R = approx. 2.2 k$\Omega$,    C = approx. 45 pF
MB89F217, MB89P215 R = approx. 3.2 k$\Omega$, C = approx. 30 pF
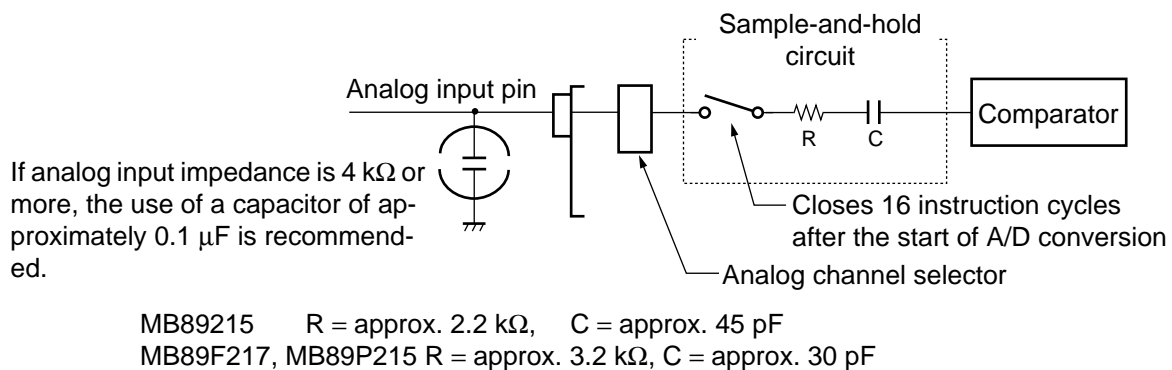
• About errors
The smaller the absolute value $|V_{CC} - V_{SS}|$ is, the greater the relative error becomes.

## 6. Electrical Characteristics of Flash Memory
• Programming and erasing characteristics

| Parameter | | Symbol | Pin Name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | | |
| Power supply current *1 | | $I_{FWE}$ | $V_{CC}$ | $V_{CC} = 5.0$ V | — | — | 40 | mA | |
| Sector erase time | Per 1 sector, constant value independent with sector capacitance | Successful completion time | — | — | — | — | 1 | 15 | s | |
| | | Unsuccessful completion time | — | — | — | — | — | *2 | — | |
| Programming time | Per 1 byte | Successful completion time | — | — | — | — | 8 | 3600 | μs | |
| | | Unsuccessful completion time | — | — | — | — | 650 | 3600 | μs | |

*1 : Embedded Algorithm executing.

*2 : If a fault occurs during sector erasing, detection via $DQ_5$ may not be available ($DQ_5 = 1$ may not occur) . Accordingly, a fault must be assumed after 15 s, even if $DQ_5$ does not go to "1".

## ■ MASK OPTIONS

| No | Part number | MB89215 | MB89F217 | MB89P215 | MB89PV210 |
|---|---|---|---|---|---|
| | Specifying procedure | Setting disallowed | | | |
| 1 | Initial value* selection of internal clock oscillation stabilization wait time (at $F_{CH}$ = 10 MHz)<br>• 01 : $2^{14}/F_{CH}$ (Approx. 1.63 ms)<br>• 10 : $2^{17}/F_{CH}$ (Approx. 13.1 ms)<br>• 11 : $2^{18}/F_{CH}$ (Approx. 26.2 ms) | $2^{18}/Fch$ (Approx. 26.2 ms) | | | |
| 2 | Power-on reset<br>• Power-on reset ON<br>• Power-on reset OFF | Yes | | | |
| 3 | Reset pin output<br>• Reset output ON<br>• Reset output OFF | Yes | | | |

$F_{CH}$ : Base oscillator

\* : Initial value to which the oscillation setting time bit (sync : WT1, WT0) in the system clock control register is set.

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB89215PFV<br>MB89P215PFV | 30-pin Plastic SSOP<br>(FPT-30P-M02) | |
| MB89215PFM<br>MB89F217PFM | 48-pin Plastic QFP<br>(FPT-48P-M13) | |
| MB89PV210CF | 48-pin Ceramic MQFP<br>(MQP-48C-P02) | |

## ■ PACKAGE DIMENSIONS

30-pin Plastic SSOP
(FPT-30P-M02)

Note 1) *1 : Resin protrusion. (Each side +0.15 (.006) Max) .
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
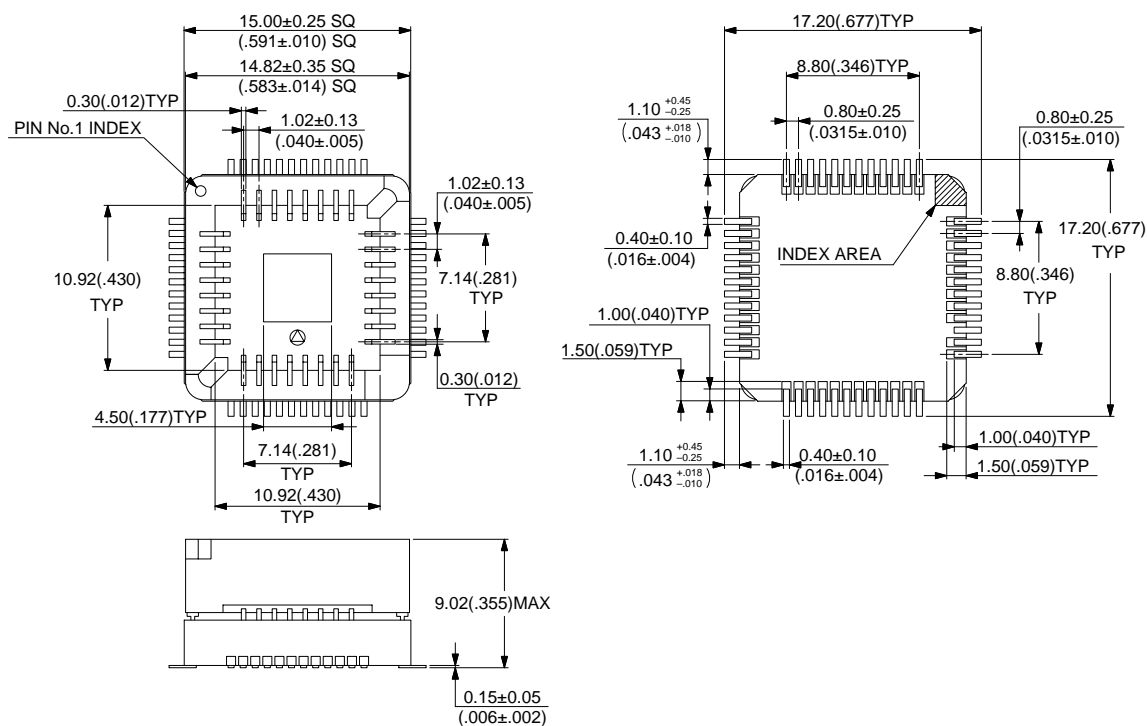Note 4) Pins width do not include tie bar cutting remainder.



*1 9.70±0.10(.382±.004)

INDEX

*2 5.60±0.10 (.220±.004)

7.60±0.20 (.299±.008)

0.65(.026)

0.24 $^{+0.08}_{-0.07}$ (.009 $^{+.003}_{-.003}$)

0.10(.004)

0.17±0.03 (.007±.001)

"A"

Details of "A" part

1.25 $^{+0.20}_{-0.10}$ (.049 $^{+.008}_{-.004}$) (Mounting height)

0.25(.010)

0~8°

0.50±0.20 (.020±.008)

0.60±0.15 (.024±.006)

0.10±0.10 (.004±.004) (Stand off)
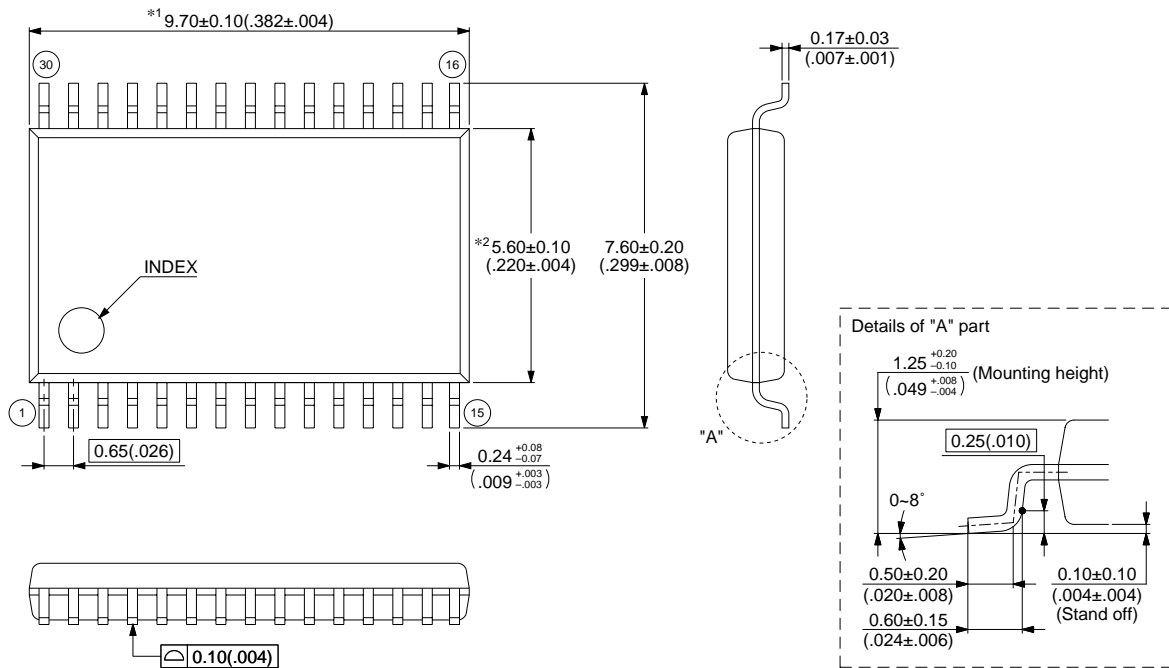
© 2003 FUJITSU LIMITED F30003S-c-3-4

Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

48-pin plastic QFP
(FPT-48P-M13)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

13.10±0.40(.516±.016)SQ

*10.00±0.20(.394±.008)SQ

0.17±0.06
(.007±.002)

0.10(.004)

INDEX

0.80(.031)

0.32±0.05
(.013±.002)

0.20(.008) Ⓜ

"A"

Details of "A" part

$1.95\,^{+0.40}_{-0.20}$ (Mounting height)
$\left(.077\,^{+.016}_{-.008}\right)$

0.25(.010)

0~8°

0.80±0.20
(.031±.008)

0.88±0.15
(.035±.006)

$0.20\,^{+0.10}_{-0.20}$
$\left(.008\,^{+.004}_{-.008}\right)$
(Stand off)
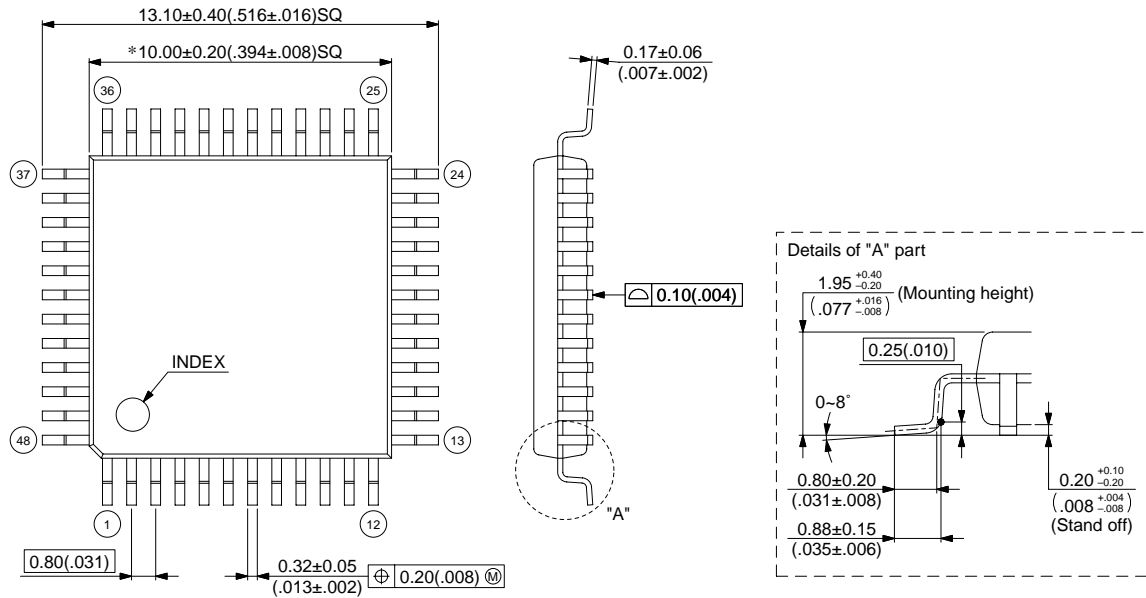
© 2003 FUJITSU LIMITED F48023S-c-3-4

Dimensions in mm (inches)
Note : The values in parentheses are reference values.

*(Continued)*

*(Continued)*

48-pin Ceramic MQFP
(MQP-48C-P02)

15.00±0.25 SQ
(.591±.010) SQ
14.82±0.35 SQ
(.583±.014) SQ

0.30(.012)TYP

PIN No.1 INDEX

1.02±0.13
(.040±.005)

1.02±0.13
(.040±.005)

10.92(.430)
TYP

7.14(.281)
TYP

0.30(.012)
TYP

4.50(.177)TYP

7.14(.281)
TYP
10.92(.430)
TYP

9.02(.355)MAX

0.15±0.05
(.006±.002)

17.20(.677)TYP

8.80(.346)TYP

$1.10 \begin{smallmatrix}+0.45\\-0.25\end{smallmatrix}$
$\left(.043 \begin{smallmatrix}+.018\\-.010\end{smallmatrix}\right)$

0.80±0.25
(.0315±.010)

0.80±0.25
(.0315±.010)

0.40±0.10
(.016±.004)

INDEX AREA

17.20(.677)
TYP

8.80(.346)
TYP

1.00(.040)TYP

1.50(.059)TYP

$1.10 \begin{smallmatrix}+0.45\\-0.25\end{smallmatrix}$
$\left(.043 \begin{smallmatrix}+.018\\-.010\end{smallmatrix}\right)$

0.40±0.10
(.016±.004)

1.00(.040)TYP
1.50(.059)TYP

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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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