Low Voltage / Low Power CMOS 16-bit Microcontrollers

TMP93CW46AF

1. Outline and Device Characteristics

The TMP93CW46AF is high-speed advanced 16-bit microcontrollers to enable low voltage and low power consumption operation. The TMP93CW46AF is housed in 100-pin mini flat package.
The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)
- TLCS-90 instruction mnemonic upward compatible
- 16M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- Micro DMA : 4 channels (1.6 μs / 2 bytes at 20 MHz)

(2) Minimum instruction execution time : 200 ns at 20 MHz

(3) Internal RAM : 4 Kbyte
Internal ROM : 128 Kbyte

(4) External memory expansion
- Can be expanded up to 16M-bytes (for both programs and data).
- Can mix 8- and 16-bit external data buses.
  ··· Dynamic data bus sizing

(5) 8-bit timer : 2 channels

(6) 8-bit PWM timer : 2 channels

(7) 16-bit timer : 2 channels

(8) Serial interface : 5 channels
- UART/Synchronous modes : 4 channels
- UART mode : 1 channel

(9) 10-bit AD converter : 8 channels

(10) Watchdog timer

(11) Chip select/wait controller : 3 blocks

(12) Interrupt functions: 35
- 9 CPU interrupts ··· SWI instruction, and Illegal instruction
- 20 internal interrupts
- 6 external interrupts

7-level priority can be set.

(13) I/O ports : 79
- Large current output : 6 pins, LED direct drive

(14) Standby function
4 halt modes (RUN, IDLE2, IDLE1, STOP)

(15) Clock gear function
- High-frequency clock can be changed fc to fc/16.
- Dual clock operation

(16) Operating voltage
- Vcc = 2.7 to 5.5 V

(17) Package : P-LQFP100-1414-0.50D

Note : Note that TMP93CW46A is different from OTP type TMP93PW46A in the electrical characteristics as follows. See the respective electrical characteristics for details.
- Power supply current Icc
- Large current port I_{OLA}

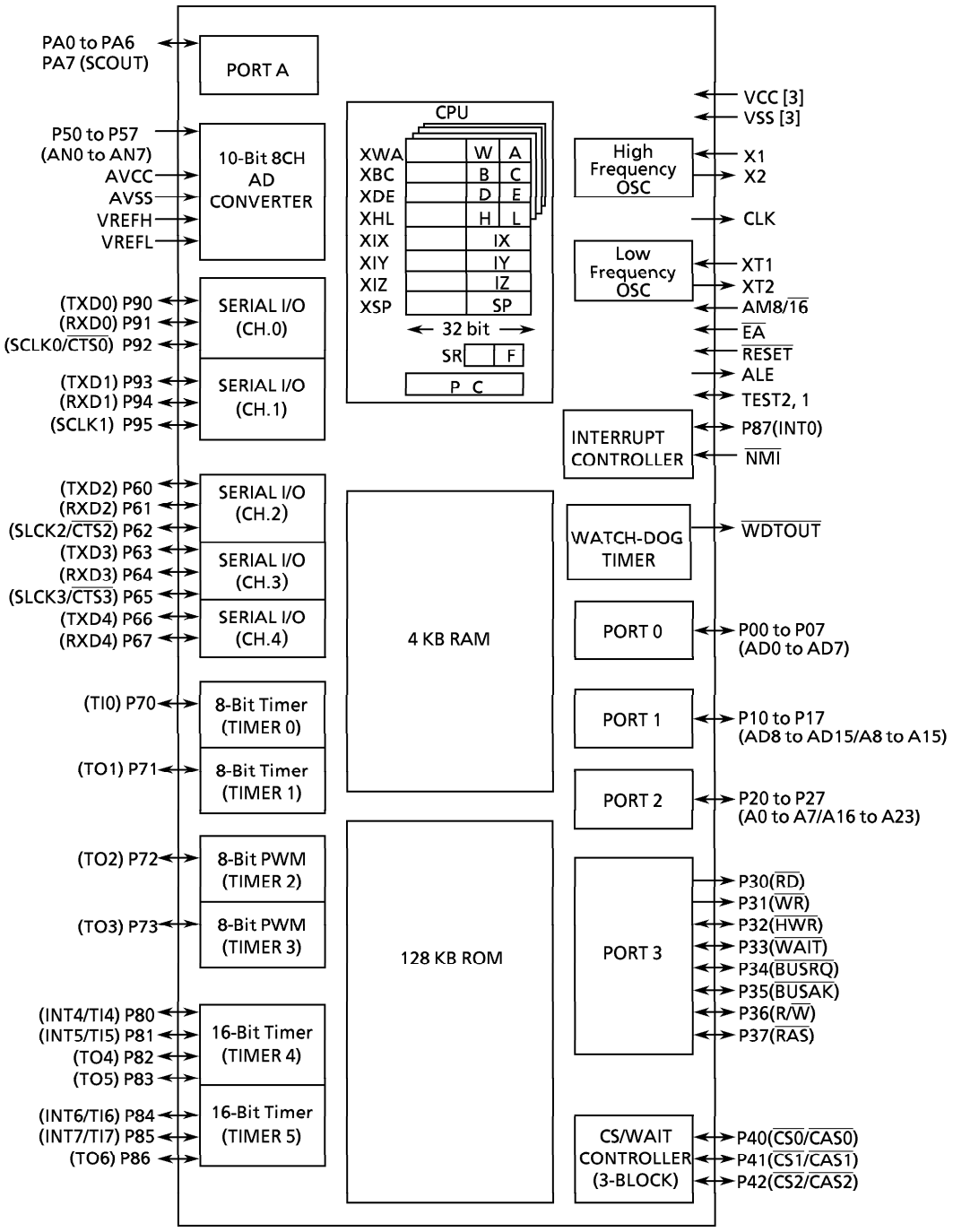


Figure 1.1 TMP93CW46A Block Diagram

2. Pin Assignment and Functions

The assignment of input / output pins for the TMP93CW46AF, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CW46AF.

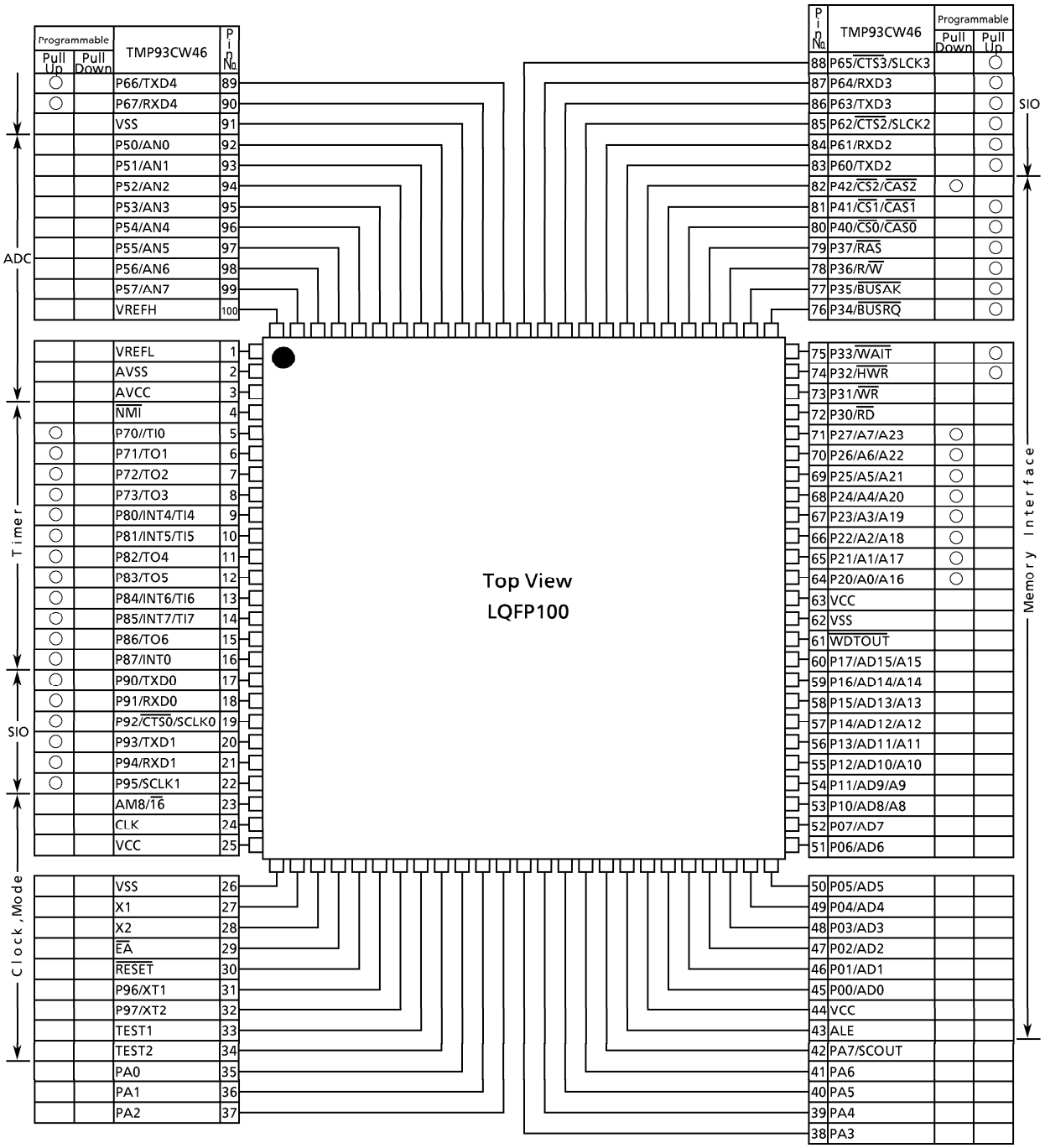


Figure 2.1.1 Pin Assignment (100-pin LQFP)

2.2 Pin Names and Functions

The names of input / output pins and their functions are described below.
Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin name	Number of pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O 3-state	Port 0: I/O port that allows selection of I/O on a bit basis Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O 3-state Output	Port 1: I/O port that allows selection of I/O on a bit basis Address data (upper): Bits 8 to 15 of address/data bus Address: 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to 15, A0 to 23, $\overline{RD}$, $\overline{WR}$,$\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note : This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller, using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.1 Pin Names and Functions (2/4)

Pin name	Number of pins	I/O	Function
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Analog signal input for AD converter
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60 TXD2	1	I/O Output	Port 60: I/O port (with pull-up resistor) Serial send data 2
P61 RXD2	1	I/O Input	Port 61: I/O port (with pull-up resistor) Serial receive data 2
P62 $\overline{CTS2}$ SCLK2	1	I/O Input I/O	Port 62: I/O port (with pull-up resistor) Serial data send enable 2 (Clear To Send) Serial Clock I/O 2
P63 TXD3	1	I/O Output	Port 63: I/O port (with pull-up resistor) Serial receive data 3
P64 RXD3	1	I/O Input	Port 64: I/O port (with pull-up resistor) Serial receive data 3
P65 $\overline{CTS3}$ SCLK3	1	I/O Input I/O	Port 65: I/O port (with pull-up resistor) Serial data send enable 3 (Clear To Send) Serial Clock I/O 3
P66 TXD4	1	I/O Output	Port 66: I/O port (with pull-up resistor) Serial send data 4
P67 RXD4	1	I/O Input	Port 67: I/O port (with pull-up resistor) Serial receive data 4
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output

Table 2.2.1 Pin Names and Functions (3/4)

Pin name	Number of pins	I/O	Function
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count / capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level / rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{\text{CTS0}}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to Send) Serial Clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA5	6	I/O	Port A0 to A5: I/O ports (large current output)
PA6	1	I/O	Port A6: I/O port

Table 2.2.1 Pin Names and Functions (4/4)

Pin name	Number of pins	I/O	Functions
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output : Outputs system clock or 2 times oscillation clock for synchronizing to external circuit.
$\overline{\text{WDTOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs「System Clock ÷ 2」Clock. Pulled-up during reset. can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	Fixed to "1".
AM8 / $\overline{16}$	1	Input	Fixed to "1".
ALE	1	Output	Address Latch Enable (Can be disabled for reducing noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (With pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
XT1 P96	1	Input I/O	Low Frequency Oscillator connecting pin Port 96: I/O port (Open Drain Output)
XT2 P97	1	Output I/O	Low Frequency Oscillator connecting pin Port 97: I/O port (Open Drain Output)
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.
VCC	3		Power supply pin (All VCC pins are connected to the power supply source.)
VSS	3		GND pin (All Vss pins are connected to the GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note : Built-in pull-up / pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

3. Operation

This section describes the functions and basic operational blocks of the TMP93CW46A devices.
See the 「7. Points of Concern and Restrictions」 for the using notice and restrictions for each block.

3.1 CPU

The TMP93CW46A device has a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous chapter).
This section describes CPU functions unique to the TMP93CW46A that are not described in the previous chapter.

3.1.1 Reset

To reset the TMP93CW46A, the $\overline{\text{RESET}}$ input must be kept at 0 for at least 10 system clocks (Resetting initializes the clock gear to 1/16. : 16 μs at 20 MHz) within the operating voltage range and with a stable oscillation.
When reset is accepted, the CPU sets as follows :

- Program Counter (PC) according to Reset Vector that is stored 8000H to 8002H.
  PC (7-0) ← data located at 8000H
  PC (15-8) ← data located at 8001H
  PC (23-16) ← data located at 8002H

Note: The address in which the reset vector is stored depends on the respective derivative products.

- Stack pointer (XSP) for system mode to 100H.
- Status register <IFF2-0> to 111. (Sets mask register to interrupt level 7.)
- Status register <MAX> to 1. (Sets to maximum mode)
- Status register <REP2-0> to 000. (Sets register banks to 0.)

When reset is released, instruction execution starts from PC (reset vector). CPU internal registers other than the above are not changed.
When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input / output port mode.
- Sets $\overline{\text{WDTOUT}}$ pin to "0". (Resetting enables the watchdog timer.)
- Pulls up the CLK pin to 1.
- Sets the ALE pin to High Impeadance (High-Z)

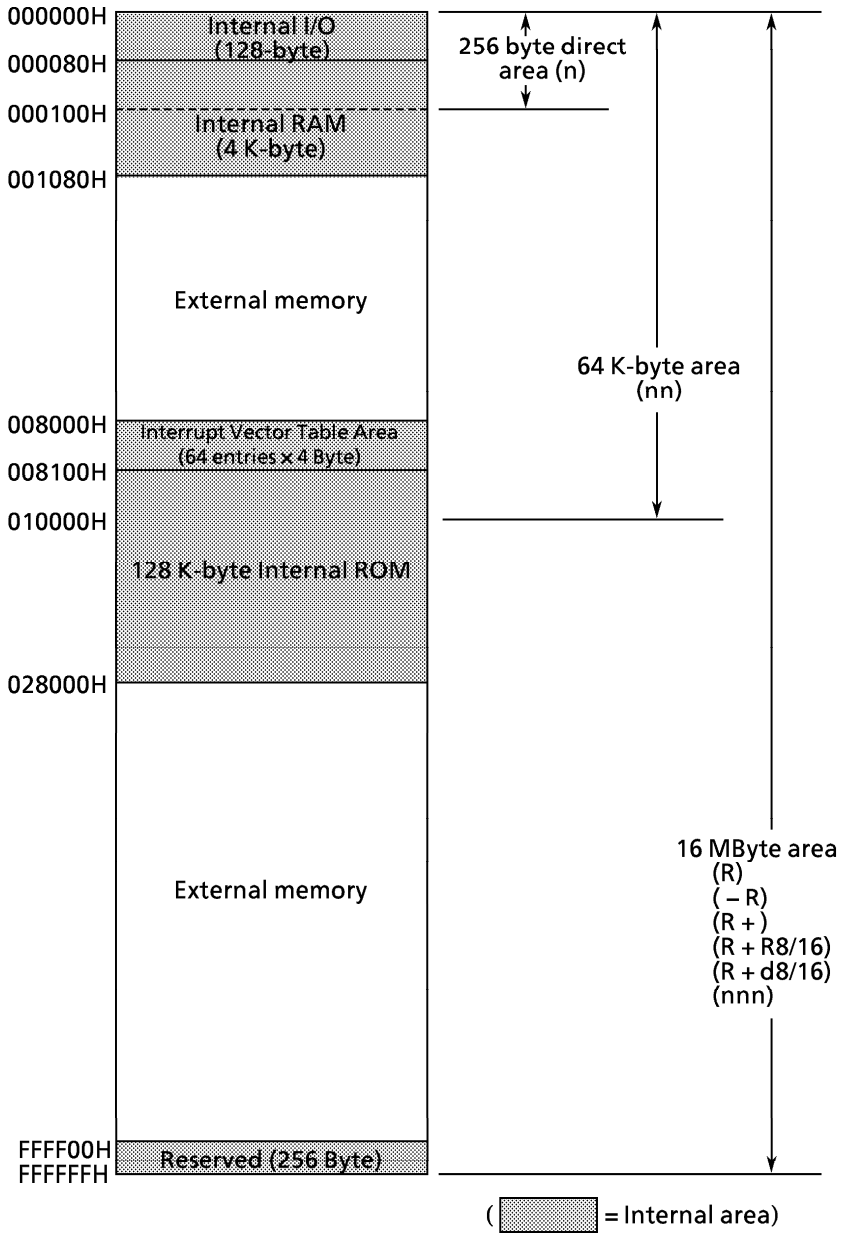
Note 1: By resetting, register in the CPU except program counter (PC), status register (SR) and stack pointer (XSP) and the data in internal RAM are not changed.

Note 2: The CLK pin is pulled up during reset. When the voltage is put down externally, there is possible to cause malfunctions.

Figure 3.1.1 shows the reset timing chart of TMP93CW46A.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CW46A.



Note : The 256 Byte Area from FFFF00H to FFFFFFH can not be used.

Figure 3.2.1 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

"X" used in an expression shows a frequency of clock f_{PH} selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = "0000").

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	− 0.5 to 6.5	V
Input Voltage	V_{IN}	− 0.5 to V_{CC} + 0.5	V
Output Current (per pin; PA0 to 5)	I_{OL1}	20	mA
Output Current (per pin; except PA0 to 5)	I_{OL2}	2	mA
Output Current (PA0 to 5 total)	ΣI_{OL1}	80	mA
Output Current (total)	ΣI_{OL}	120	mA
Output Current (total)	ΣI_{OH}	− 80	mA
Power Dissipation (Ta = 85°C)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	℃
Storage Temperature	T_{STG}	− 65 to 150	℃
Operating Temperature	T_{OPR}	− 40 to 85	℃

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2) (Vss = 0 V, Ta = − 40 to 85°C)

Parameter		Symbol	Condition		Min	Typ. (Note)	Max	Unit
Power Supply Voltage (AVCC = VCC, AVss = Vss)		V_{CC}	fc = 4 to 20 MHz	fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz		2.7			
Input Low Voltage	AD0 to 15	V_{IL}	$V_{CC} \geqq 4.5$ V		−0.3		0.8	V
			$V_{CC} < 4.5$ V				0.6	
	Port2 to A (except P87)	V_{IL1}	V_{CC} = 2.7 to 5.5 V				0.3 V_{CC}	
	RESET, NMI, INT0	V_{IL2}					0.25 V_{CC}	
	EA, AM8/16	V_{IL3}					0.3	
	X1	V_{IL4}					0.2 V_{CC}	
Input High Voltage	AD0 to 15	V_{IH}	$V_{CC} \geqq 4.5$ V		2.2		V_{CC} + 0.3	
			$V_{CC} < 4.5$ V		2.0			
	Port2 to A (except P87)	V_{IH1}	V_{CC} = 2.7 to 5.5 V		0.7 V_{CC}			
	RESET, NMI, INT0	V_{IH2}			0.75 V_{CC}			
	EA, AM8/16	V_{IH3}			V_{CC} − 0.3			
	X1	V_{IH4}			0.8 V_{CC}			

Note : Typical values are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2) (Vss = 0 V, Ta = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA (V_{CC} = 2.7 to 5.5 V)			0.45	V
Output Low Current (PA0 to 5)	I_{OLA}	V_{OL} = 1.0 V (V_{CC} = 3 V ± 10%)	7			mA
		V_{OL} = 1.0 V (V_{CC} = 5 V ± 10%)	16			
Output High Voltage	V_{OH1}	I_{OH} = – 400 μA (V_{CC} = 3 V ± 10%)	2.4			V
	V_{OH2}	I_{OH} = – 400 μA (V_{CC} = 5 V ± 10%)	4.2			
Darlington Drive Current (8 Output Pins Max)	I_{DAR} (Note 2)	V_{EXT} = 1.5 V, R_{EXT} = 1.1 kΩ (V_{CC} = 5 V ± 10% only)	– 1.0		– 3.5	mA
Input Leakage Current	I_{LI}	0.0 ≦ V_{IN} ≦ V_{CC}		0.02	± 5	μA
Output Leakage Current	I_{LO}	0.2 ≦ V_{IN} ≦ V_{CC} – 0.2		0.05	± 10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 V_{CC}, V_{IH2} = 0.8 V_{CC}	2.0		6.0	V
$\overline{RESET}$ Pull Up Resister	R_{RST}	V_{CC} = 5 V ± 10%	50		150	kΩ
		V_{CC} = 3 V ± 10%	80		200	
Pin Capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	V_{TH}		0.4	1.0		V
Programmable Pull Down Resistor	R_{KL}	V_{CC} = 5 V ± 10%	10		80	kΩ
		V_{CC} = 3 V ± 10%	30		150	
Programmable Pull Up Resistor	R_{KH}	V_{CC} = 5 V ± 10%	50		150	
		V_{CC} = 3 V ± 10%	100		300	
NORMAL	I_{CC}	V_{CC} = 5 V ± 10%, fc = 20 MHz		21	28	mA
RUN				17	25	
IDLE2				12.5	17	
IDLE1				2.5	4	
NORMAL		V_{CC} = 3 V ± 10%, fc = 12.5 MHz (Typ. : V_{CC} = 3.0 V)		7	10	mA
RUN				5.5	9	
IDLE2				4.5	6	
IDLE1				0.7	1	
SLOW		V_{CC} = 3 V ± 10%, fs = 32.768 kHz (Typ. : V_{CC} = 3.0 V)		20	35	μA
RUN				16	30	
IDLE2				11	25	
IDLE1				4	15	
STOP		Ta ≦ 50°C, V_{CC} = 2.7 to 5.5 V		0.2	10	μA
		Ta ≦ 70°C			20	
		Ta ≦ 85°C			50	

Note1 : Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.
Note2 : I_{DAR} is guranteed for total of up to 8 ports.

4.3 AC Characteristics

(1) V_{CC} = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	33333	62.5		50		ns
2	CLK pulse width	t_{CLK}	2x – 40		85		60		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE High pulse width	t_{LL}	x – 40		23		10		ns
8	ALE fall→ $\overline{RD}$/$\overline{WR}$ fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ rise→ ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to 15 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to 23 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$fall→ D0 to 15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$rise→ D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$rise→ A0 to 15output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to 15 Valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input ($^{1WAIT}_{+n\ mode}$)	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input ($^{1WAIT}_{+n\ mode}$)	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ Hold ($^{1WAIT}_{+n\ mode}$)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200		200	ns
28	A0 to 23 Valid→ $\overline{RAS}$ fall	t_{ASRH}	1.0x – 40		23		10		ns
29	A0 to 15 Valid→ $\overline{RAS}$ fall	t_{ASRL}	0.5x – 15		16		10		ns
30	$\overline{RAS}$ fall→ D0 to 15 input	t_{RAC}		2.5x – 70		86		55	ns
31	$\overline{RAS}$ fall→ A0 to 15 Hold	t_{RAH}	0.5x – 15		16		10		ns
32	$\overline{RAS}$ Low pulse width	t_{RAS}	2.0x – 40		85		60		ns
33	$\overline{RAS}$ High pulse width	t_{RP}	2.0x – 40		85		60		ns
34	$\overline{CAS}$ fall→ $\overline{RAS}$ rise	t_{RSH}	1.0x – 40		23		10		ns
35	$\overline{RAS}$ rise→ $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		6		0		ns
36	$\overline{RAS}$ fall→ $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		23		10		ns
37	$\overline{CAS}$ fall→ D0 to 15 input	t_{CAC}		1.5x – 65		29		10	ns
38	$\overline{CAS}$ Low pulse width	t_{CAS}	1.5x – 30		64		40		ns

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, RD, WR, HWR, R/W, CLK, RAS, CAS0 to CAS2)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC} / Low 0.2 × V_{CC} (Except for AD0 to AD15)

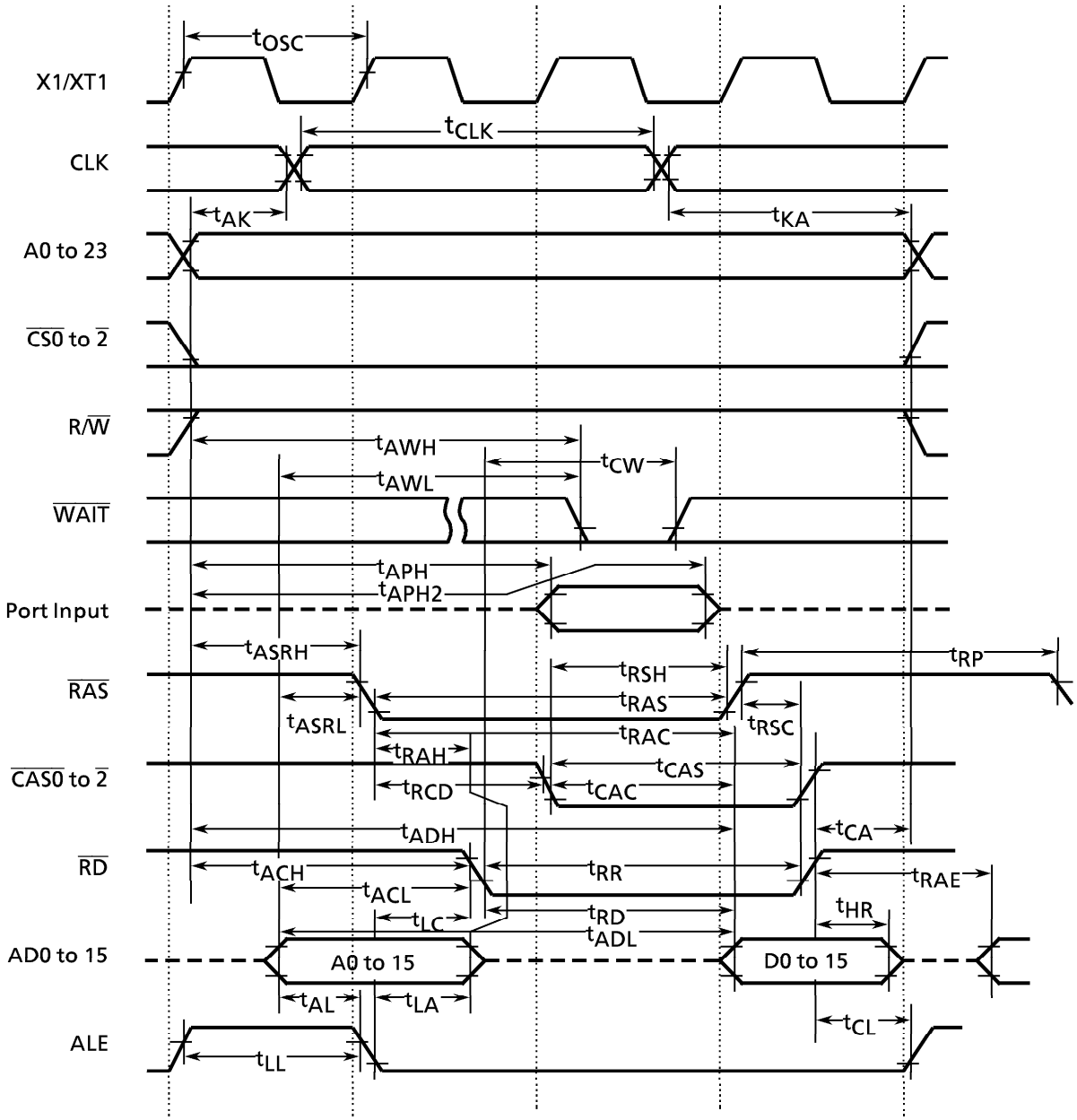
(2) V_{CC} = 3 V ± 10%

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	80	33333	80		ns
2	CLK pulse width	t_{CLK}	2x – 40		120		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5x – 30		10		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5x – 80		40		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5x – 35		5		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5x – 35		5		ns
7	ALE High pulse width	t_{LL}	x – 60		20		ns
8	ALE fall→ $\overline{RD}/\overline{WR}$ fall	t_{LC}	0.5x – 35		5		ns
9	$\overline{RD}/\overline{WR}$ rise→ ALE rise	t_{CL}	0.5x – 40		0		ns
10	A0 to 15 Valid→ $\overline{RD}/\overline{WR}$ fall	t_{ACL}	x – 50		30		ns
11	A0 to 23 Valid→ $\overline{RD}/\overline{WR}$ fall	t_{ACH}	1.5x – 50		70		ns
12	$\overline{RD}/\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5x – 40		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0x – 110		130	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5x – 125		155	ns
15	$\overline{RD}$fall→ D0 to 15 input	t_{RD}		2.0x – 115		45	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		120		ns
17	$\overline{RD}$rise→ D0 to 15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$rise→ A0 to 15output	t_{RAE}	x – 25		55		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		120		ns
20	D0 to 15 Valid→ $\overline{WR}$rise	t_{DW}	2.0x – 120		40		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5x – 40		0		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)	t_{AWH}		3.5x – 130		150	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input (1WAIT + n mode)	t_{AWL}		3.0x – 100		140	ns
24	$\overline{RD}/\overline{WR}$ fall→$\overline{WAIT}$ Hold (1WAIT + n mode)	t_{CW}	2.0x + 0		160		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5x – 195		5	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		250		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200	ns
28	A0 to 23 Valid→ $\overline{RAS}$ fall	t_{ASRH}	1.0x – 60		20		ns
29	A0 to 15 Valid→ $\overline{RAS}$ fall	t_{ASRL}	0.5x – 40		0		ns
30	$\overline{RAS}$ fall→ D0 to 15 input	t_{RAC}		2.5x – 90		110	ns
31	$\overline{RAS}$ fall→ A0 to 15 Hold	t_{RAH}	0.5x – 25		15		ns
32	$\overline{RAS}$ Low pulse width	t_{RAS}	2.0x – 40		120		ns
33	$\overline{RAS}$ High pulse width	t_{RP}	2.0x – 40		120		ns
34	$\overline{CAS}$ fall→ $\overline{RAS}$ rise	t_{RSH}	1.0x – 55		25		ns
35	$\overline{RAS}$ rise→ $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		15		ns
36	$\overline{RAS}$ fall→ $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		40		ns
37	$\overline{CAS}$ fall→ D0 to 15 input	t_{CAC}		1.5x – 120		0	ns
38	$\overline{CAS}$ Low pulse width	t_{CAS}	1.5x – 40		80		ns

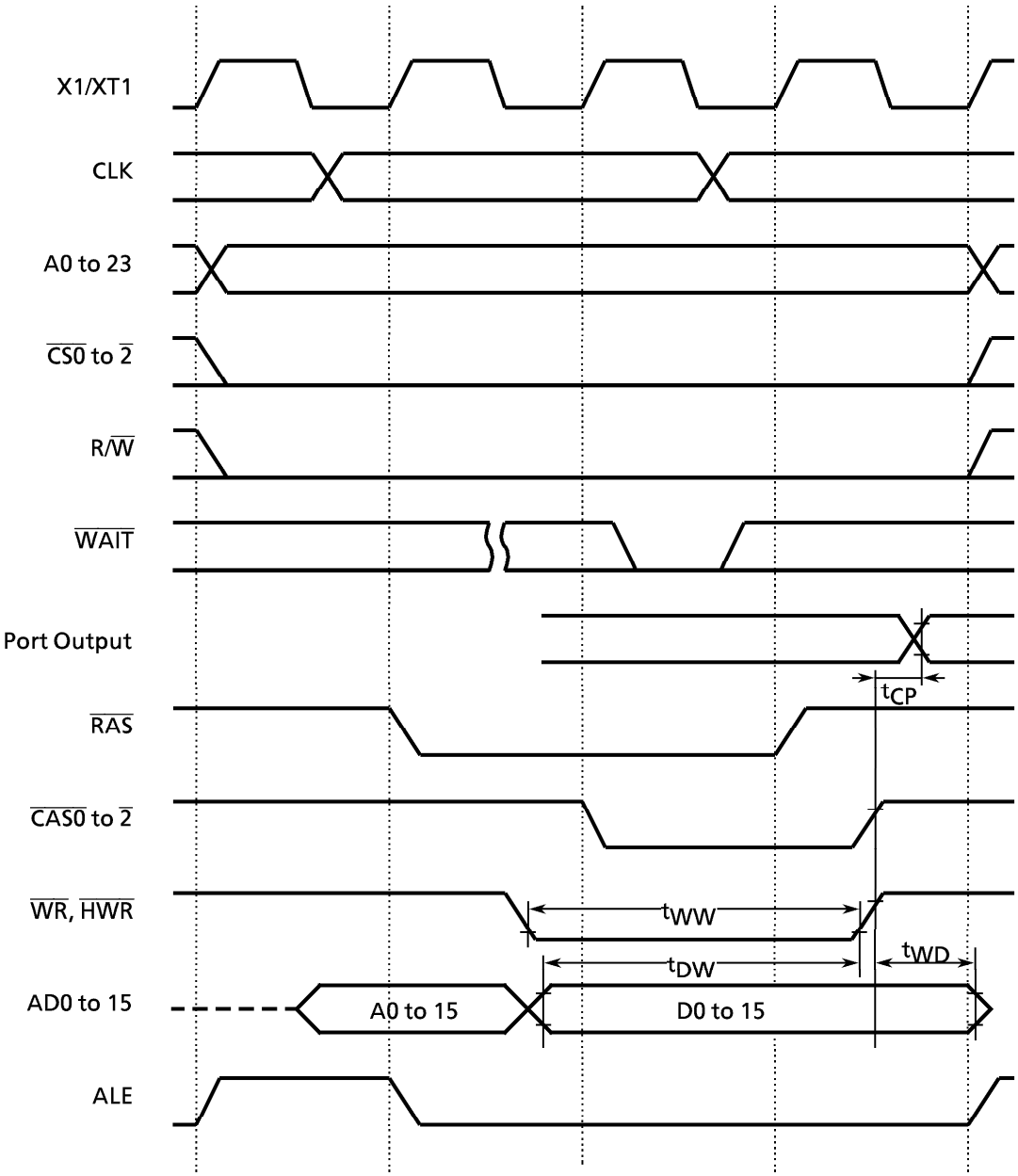
AC Measuring Conditions

- Output Level : High 0.7 × V_{CC} / Low 0.3 × V_{CC}, CL = 50 pF
- Input Level : High 0.9 × V_{CC} / Low 0.1 × V_{CC}

(1) Read Cycle


X1/XT1
CLK
A0 to 23
CS0 to 2
R/W
WAIT
Port Input
RAS
CAS0 to 2
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tASRH
tASRL
tRSH
tRAS
tRAC
tRAH
tRCD
tCAS
tCAC
tRSC
tRP
tADH
tACH
tACL
tLC
tRR
tRD
tADL
tCA
tRAE
tHR
A0 to 15
D0 to 15
tAL
tLA
tLL
tCL

(2) Write Cycle



4.4 AD Conversion Characteristics (Vss = 0 V, AVcc = Vcc, AVss = Vss, Ta = – 40 to 85°C)

Parameter	Symbol	Power Supply	Min	Typ.	Max	Unit
Analog reference voltage (+)	V_{REFH}	V_{CC} = 5 V ± 10%	V_{CC} – 1.5 V	V_{CC}	V_{CC}	V
		V_{CC} = 3 V ± 10%	V_{CC} – 0.2 V	V_{CC}	V_{CC}	
Analog reference voltage (–)	V_{REFL}	V_{CC} = 5 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
		V_{CC} = 3 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)	V_{CC} = 5 V ± 10%		0.5	1.5	mA
		V_{CC} = 3 V ± 10%		0.3	0.9	
<VREFON> = 0		V_{CC} = 2.7 to 5.5V		0.02	5.0	μA
Error	—	V_{CC} = 5 V ± 10%		± 1.0	± 3.0	LSB
		V_{CC} = 3 V ± 10%		± 1.0	± 3.0	

Note 1: $1LSB = (V_{REFH} - V_{REFL}) / 2^{10}$ [V]
Note 2: Minimum operation frequency
The operation of this AD converter is guaranteed only when fc (high frequency oscillator) is used. (It is not guaranteed when fs is used.) Additionally, it is guaranteed with $f_{FPH} \geqq 4$ MHz.
Note 3: The value I_{CC} includes the current with flows through AVCC pin.
Note 4: The operation of this AD converter is guaranteed at 5 V ± 10%.

4.5 Serial Channel Timing

(1) SCLK Input Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	16X		488 μs		1.28 μs		0.8 μs	
Output Data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 – 5X – 50		91.5 μs		190 ns		100 ns	
SCLK rising edge→ Output Data hold	t_{OHS}	5X – 100		152 μs		300 ns		150 ns	
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		0	
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} – 5X – 100		336 μs		780 ns		450 ns

(2) SCLK Output Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle (programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28 μs	655.36 μs	0.8 μs	409.6 μs
Output Data → SCLK rising edge	t_{OSS}	t_{SCY} – 2X – 150		427 μs		970 ns		550 ns	
SCLK rising edge→ Output Data hold	t_{OHS}	2X – 80		60 μs		80 ns		20 ns	
SCLK rising edge→ Input Data hold	t_{HSR}	0		0		0		0	
SCLK rising edge→ effective data input	t_{SRD}		t_{SCY} – 2X – 150		428 μs		970 ns		550 ns

(3) SCLK Input Mode (UART mode)

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	4X + 20		122 μs		340 ns		220 ns	
Low level SCLK Pulse width	t_{SCYL}	2X + 5		6 μs		165 ns		105 ns	
High level SCLK Pulse width	t_{SCYH}	2X + 5		6 μs		165 ns		105 ns	

Note : fs is used as system clock (f_{SYS}) or fs is used as input clock to prescaler.

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		740		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		360		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 interrupts

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 Low level pulse width	t_{INTAL}	4X		320		200		ns
$\overline{NMI}$, INT0 High level pulse width	t_{INTAH}	4X		320		200		ns

(2) INT4 to 7

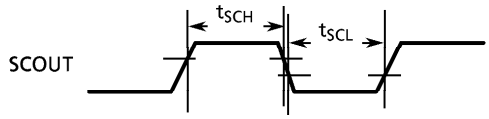
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT4 to INT7 Low level pulse width	t_{INTBL}	4X + 100		420		300		ns
INT4 to INT7 High level pulse width	t_{INTBH}	4X + 100		420		300		ns

4.8 SCOUT pin AC characteristics

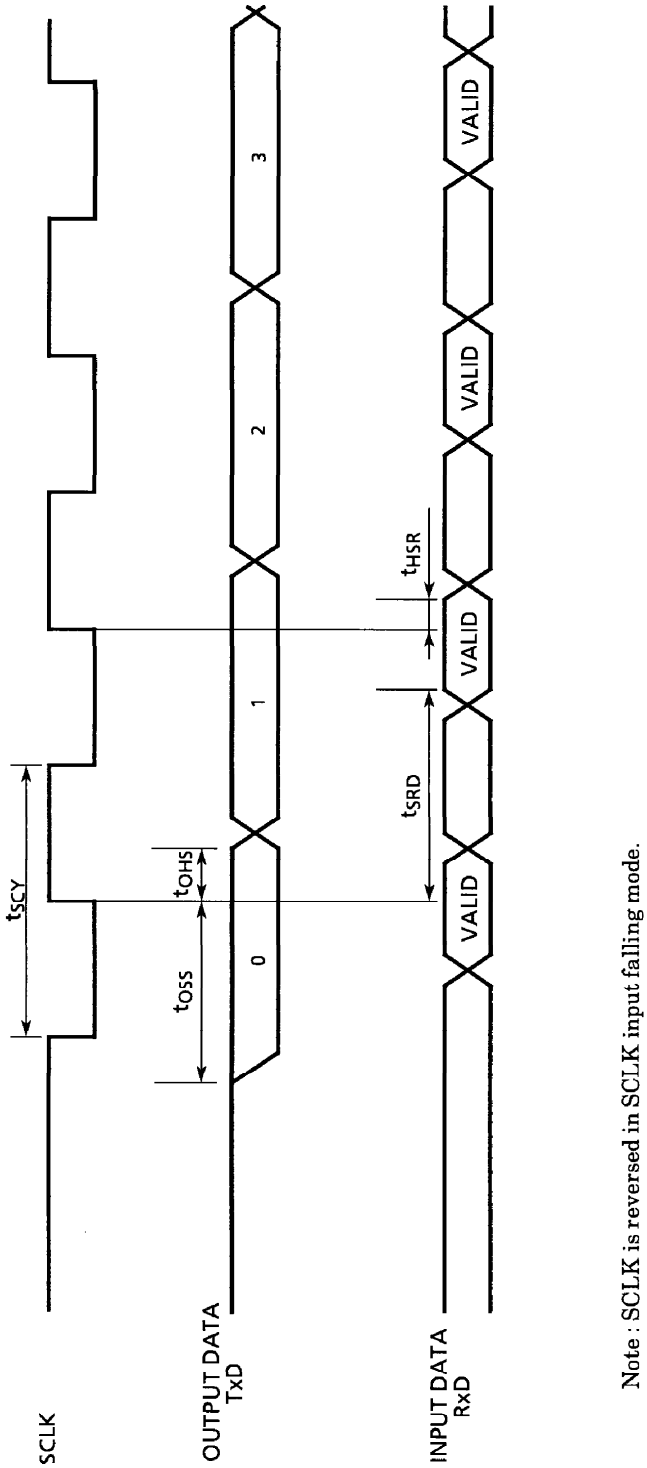
Parameter	Symbol	Variable		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max
High-level pulse width	t_{SCH}						
VCC = 5 V ± 10%		0.5X–10		30		15	
VCC = 3 V ± 10%		0.5X–20		20		—	—
Low-level pulse width	t_{SCL}						
VCC = 5 V ± 10%		0.5X–10		30		15	
VCC = 3 V ± 10%		0.5X–20		20		—	—

Measurement condition

- Output level : High 2.2 V / Low 0.8 V, CL = 10 pF

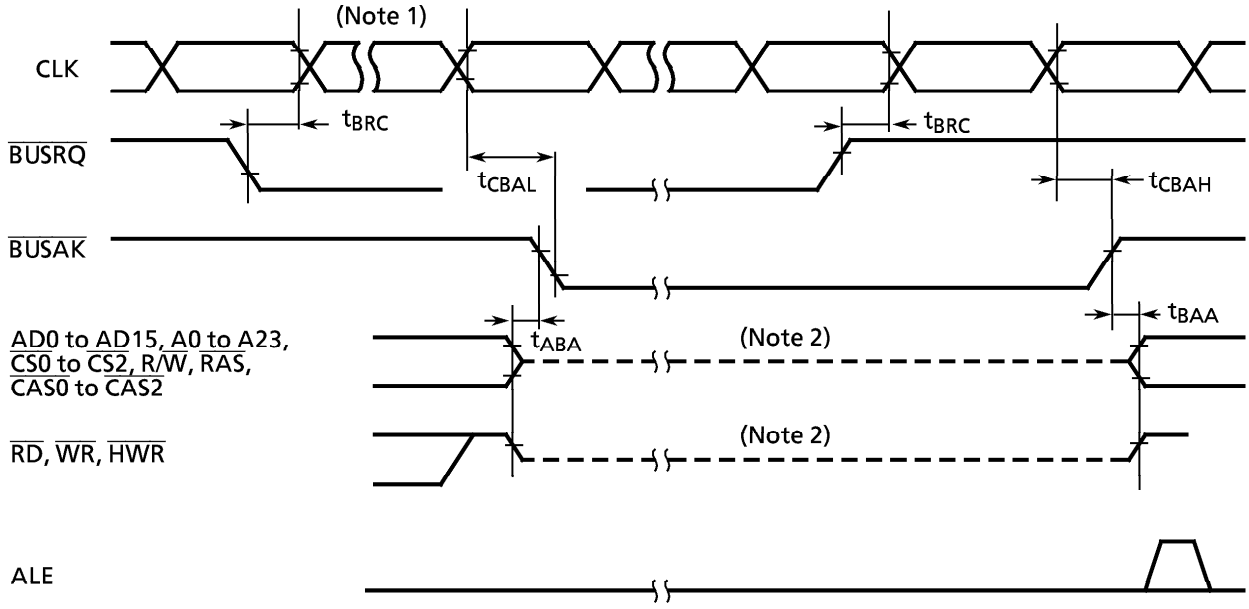


4.9 Timing Chart for I/O Interface Mode



Note : SCLK is reversed in SCLK input falling mode.

4.10 Timing Chart for Bus Request ($\overline{BUSRQ}$) / Bus Acknowledge ($\overline{BUSAK}$)



Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{BUSRQ}$ set-up time to CLK	t_{BRC}	120		120		120		ns
CLK→ $\overline{BUSAK}$ falling edge	t_{CBAL}		1.5x + 120		240		195	ns
CLK→ $\overline{BUSAK}$ rising edge	t_{CBAH}		0.5x + 40		80		65	ns
Output Buffer is off to $\overline{BUSAK}$ ↓	t_{ABA}	0	80	0	80	0	80	ns
$\overline{BUSAK}$ ↑ to Output Buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1 : The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2 : This line only shows the output buffer is off-state.
It doen't indicate the signal level is fixed.
Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level-fix will be delayed.
The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.