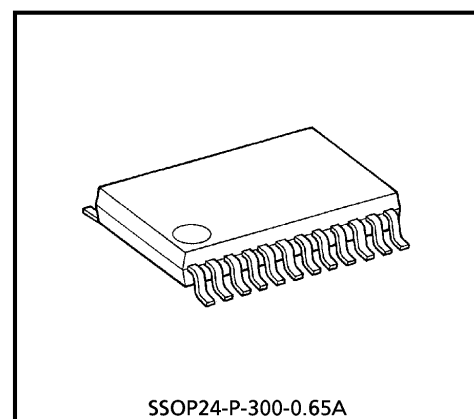


TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX646FS

LOW VOLTAGE OCTAL BUS TRANSCEIVER / REGISTER WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX646 is a high performance CMOS OCTAL BUS TRANSCEIVER / REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs. This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.



Weight : 0.14g (Typ.)

FEATURES

- Low voltage operation : $V_{CC} = 2.0 \sim 3.6V$
- High speed operation : $t_{pd} = 7.0ns$ (Max.) ($V_{CC} = 3.0 \sim 3.6V$)
- Output current : $|I_{OH}| / I_{OL} = 24mA$ (Min.) ($V_{CC} = 3.0V$)
- Latch-up performance : $\pm 500mA$
- Available in SSOP.
- Bidirectional interface between 5V and 3.3V signals.
- Power down protection is provided on all inputs.
- Pin and function compatible with the 74 series (74AC / HC / F / ALS / LS etc.) 646 type.

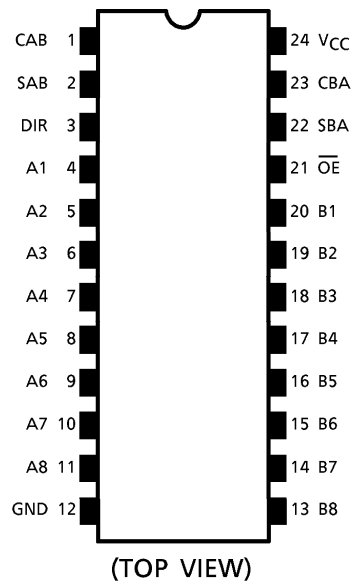
(Note) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

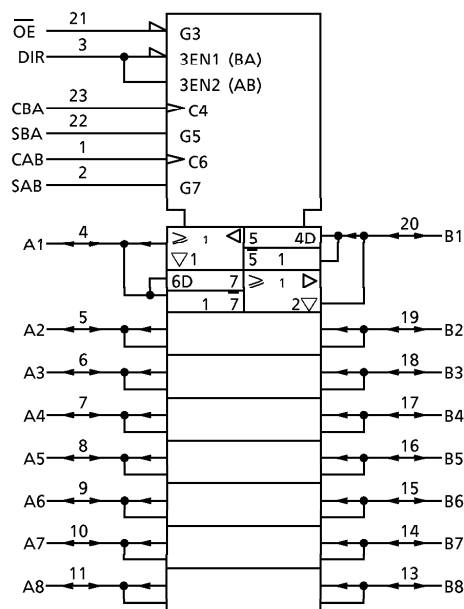
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PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

CONTROL INPUTS						BUS		FUNCTION
\overline{OE}	DIR	CAB	CBA	SAB	SBA	A	B	
H	X	X*	X*	X	X	INPUT	INPUT	The output functions of A and B Busses are disabled.
		Z	Z			Z	Z	
L	X			X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
		X*	X*	L	X	INPUT	OUTPUT	The data on the A bus are displayed on the B bus.
						L	L	
						H	H	
			X*	L	X	L	L	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
						H	H	
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
			X*	H	X	L	L	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
						H	H	
L	L	X*	X*	X	L	OUTPUT	INPUT	The data on the B Bus are displayed on the A bus.
						L	L	
						H	H	
		X*		X	L	L	L	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
						H	H	
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*		X	H	L	L	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
						H	H	

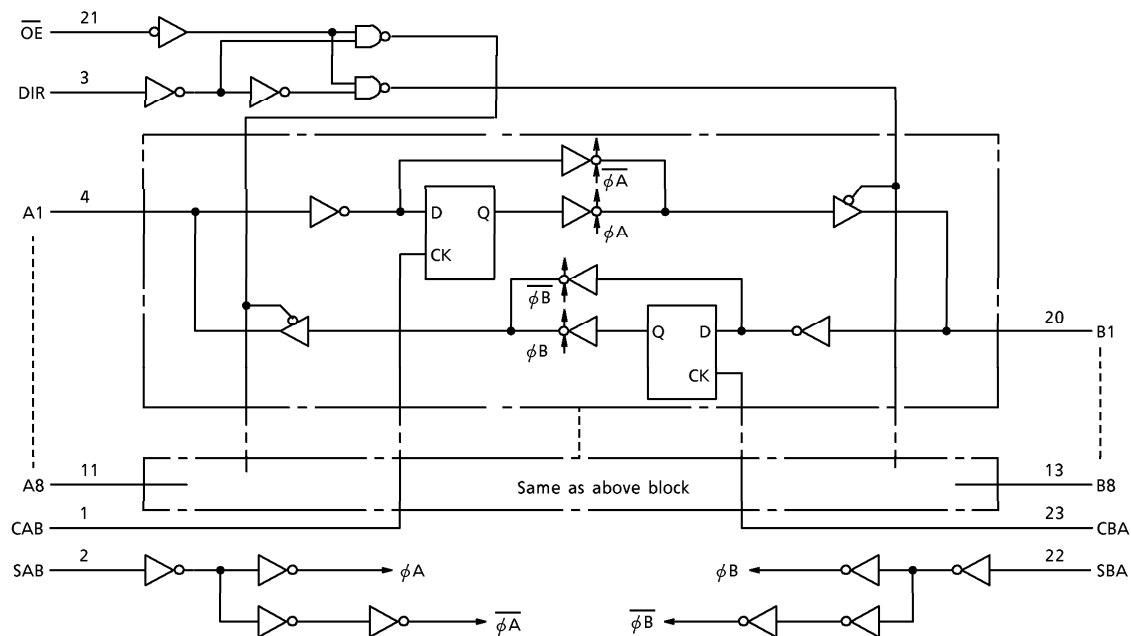
X : Don't care

Z : High Impedance

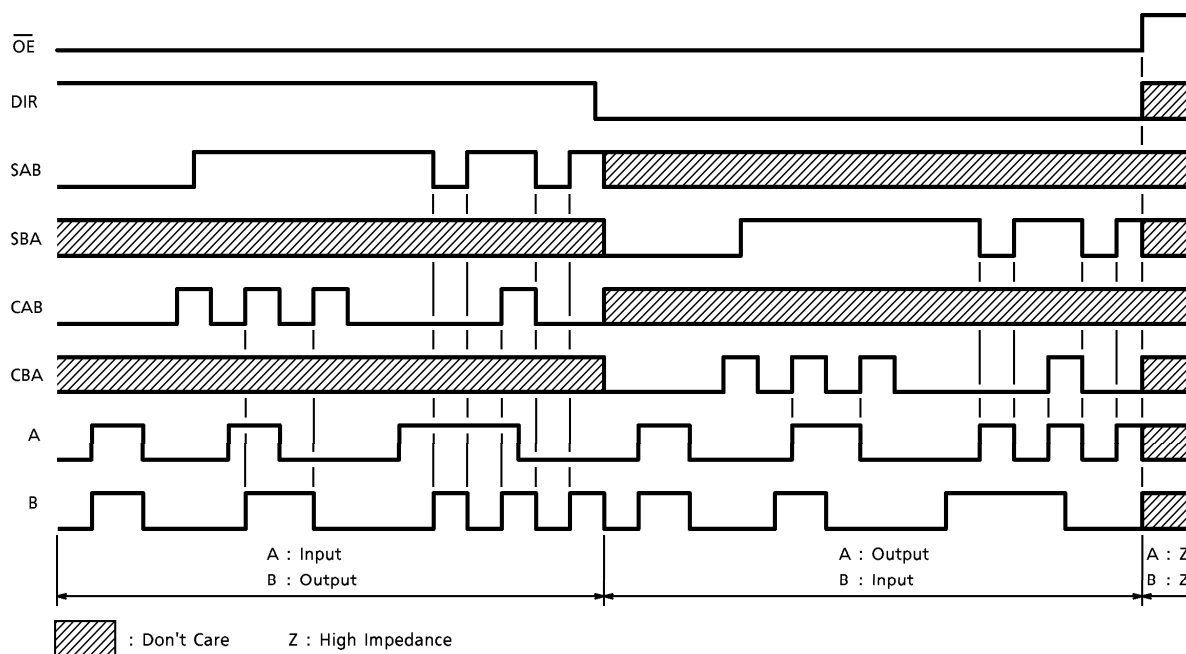
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

* The clocks are not internally with either \overline{OE} or DIR. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

SYSTEM DIAGRAM



TIMING CHART



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage (DIR, \overline{OE} , CAB, CBA, SAB, SBA)	V_{IN}	$-0.5 \sim 7.0$	V
DC Bus I/O Voltage	$V_{I/O}$	$-0.5 \sim 7.0$ (Note 1)	V
		$-0.5 \sim V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	180	mW
DC V_{CC} / Ground Current	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

(Note 1) Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note 4)	
Input Voltage (DIR, \overline{OE} , CAB, CBA, SAB, SBA)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~5.5 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	± 24 (Note 7)	mA
		± 12 (Note 8)	
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise And Fall Time	dt / dv	0~10 (Note 9)	ns / V

(Note 4) Data Retention Only.

(Note 5) Off-State

(Note 6) High or Low State.

(Note 7) $V_{CC} = 3.0 \sim 3.6\text{V}$ (Note 8) $V_{CC} = 2.7 \sim 3.0\text{V}$ (Note 9) $V_{IN} = 0.8 \sim 2.0\text{V}$, $V_{CC} = 3.0\text{V}$

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V _{IH}			2.7~3.6	2.0	—	V
	"L" Level	V _{IL}			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = - 12mA	2.7	2.2	—	
				I _{OH} = - 18mA	3.0	2.4	—	
				I _{OH} = - 24mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	—	0.2	
				I _{OL} = 12mA	2.7	—	0.4	
				I _{OL} = 16mA	3.0	—	0.4	
				I _{OL} = 24mA	3.0	—	0.55	
Input Leakage Current		I _{IN}	V _{IN} = 0~5.5V	2.7~3.6	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~5.5V	2.7~3.6	—	± 5.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} / V _{OUT} = 5.5V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND	2.7~3.6	—	10.0	μA	
			V _{IN} / V _{OUT} = 3.6~5.5V	2.7~3.6	—	± 10.0		
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6V	2.7~3.6	—	500		

AC characteristic (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Maximum Clock Frequency	f _{MAX}	(Fig.1, 2)	2.7	—	—	MHz
			3.3 ± 0.3	150	—	
Propagation Delay Time (An, Bn-Bn, An)	t _{pLH} t _{pHL}	(Fig.1, 2)	2.7	—	8.0	ns
			3.3 ± 0.3	1.5	7.0	
Propagation Delay Time (CAB, CBA-Bn, An)	t _{pLH} t _{pHL}	(Fig.1, 5)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Propagation Delay Time (SAB, SBA-Bn, An)	t _{pLH} t _{pHL}	(Fig.1, 2)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output Enable Time (OE, DIR-An, Bn)	t _{pZL} t _{pZH}	(Fig.1, 3, 4)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output Disable Time (OE, DIR-An, Bn)	t _{pLZ} t _{pHZ}	(Fig.1, 3, 4)	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Minimum Pulse Width	t _w (H) t _w (L)	(Fig.1, 5)	2.7	3.3	—	ns
			3.3 ± 0.3	3.3	—	
Minimum Set-up Time	t _s	(Fig.1, 5)	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum Hold Time	t _h	(Fig.1, 5)	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output To Output Skew	t _{osLH} t _{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.

(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)DYNAMIC SWITCHING CHARACTERISTICS (Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

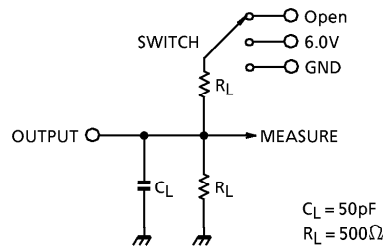
CAPACITIVE CHARACTERISTICS (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}	DIR, $\overline{\text{OE}}$, CAB, CBA, SAB, SBA	3.3 ± 0.3	7	pF
Bus Input Capacitance	C _{I/O}	An, Bn	3.3 ± 0.3	8	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10MHz (Note 11)	3.3 ± 0.3	25	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
 Average operating current can be obtained by the equation :
 $I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

TEST CIRCUIT

Fig.1



PARAMETER	SWITCH
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0V
t _{pHZ} , t _{pZH}	GND
t _w , t _s , t _h , f _{MAX}	Open

AC WAVEFORM

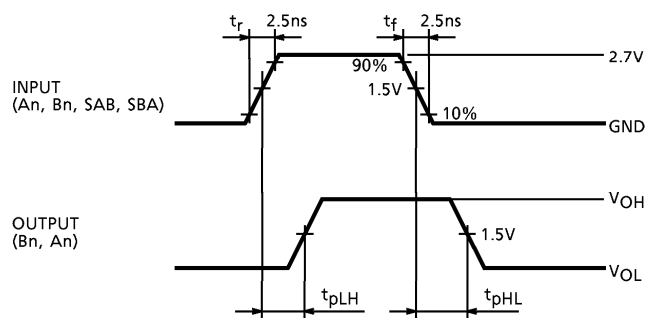
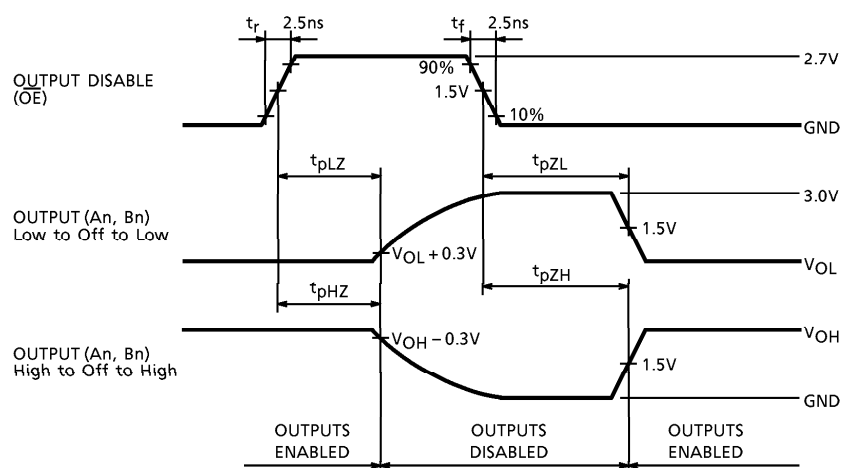
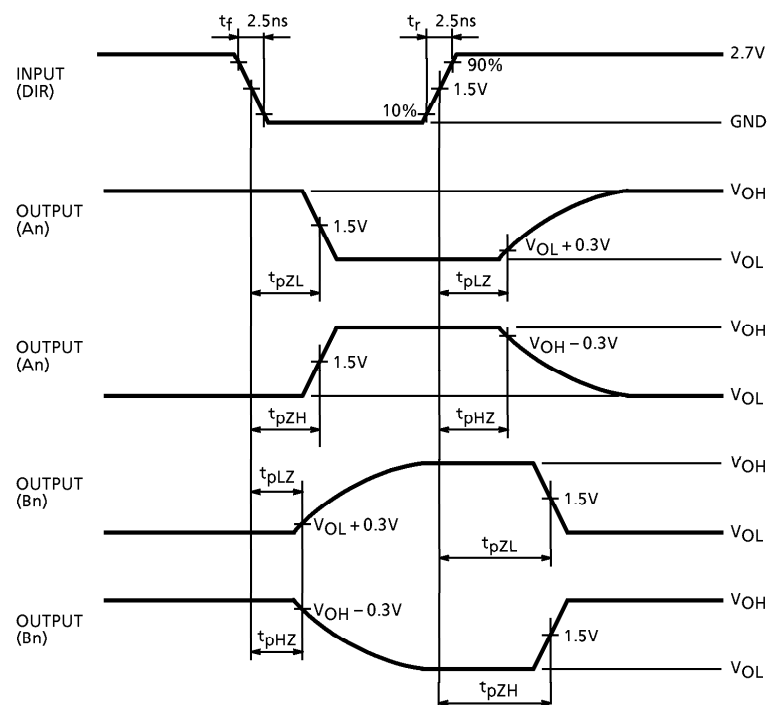
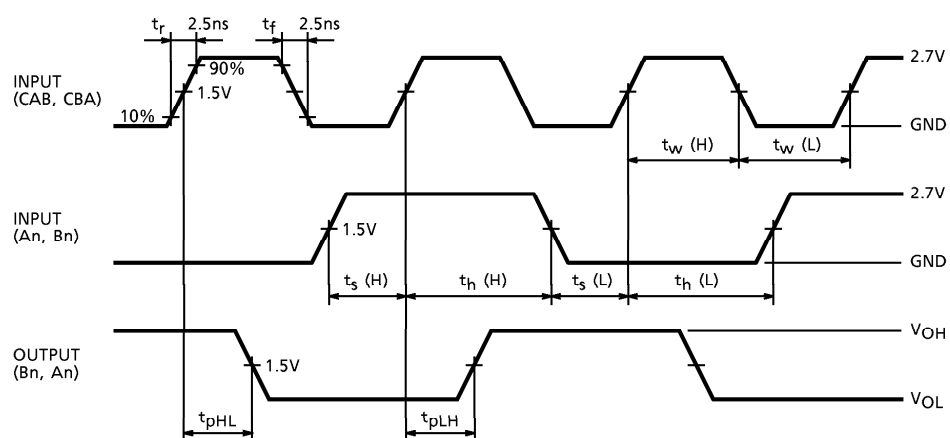
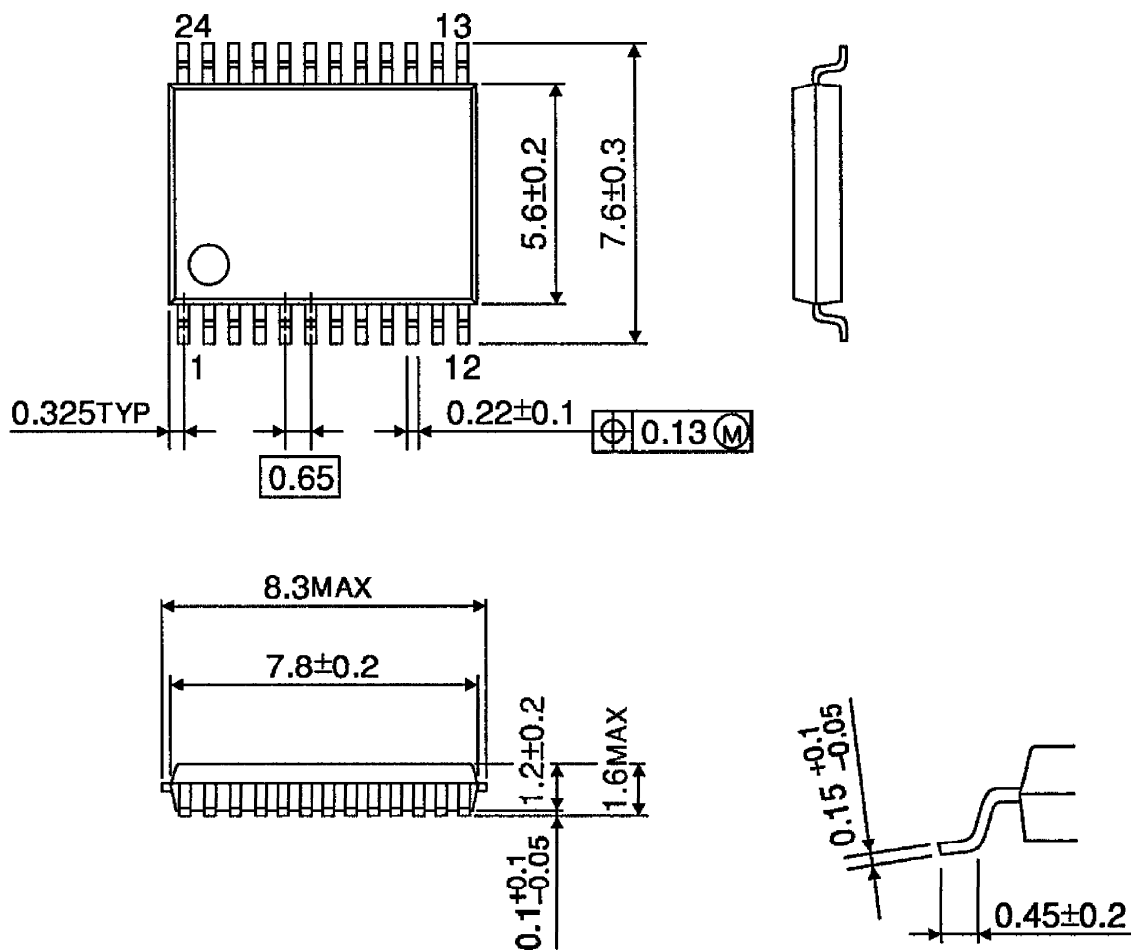
Fig.2 t_{pLH} , t_{pHL} Fig.3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} 

Fig.4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} Fig.5 t_{pLH} , t_{pHL} , t_w , t_s , t_h 

OUTLINE DRAWING

SSOP24-P-300-0.65A

Unit : mm



Weight : 0.14g (Typ.)