

TC74ACT373P, TC74ACT373F, TC74ACT373FW, TC74ACT373FT

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74ACT373 is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. These 8-bit D-type latches are controlled by a latch enable (LE) and a output enable input ($\overline{OE}$).

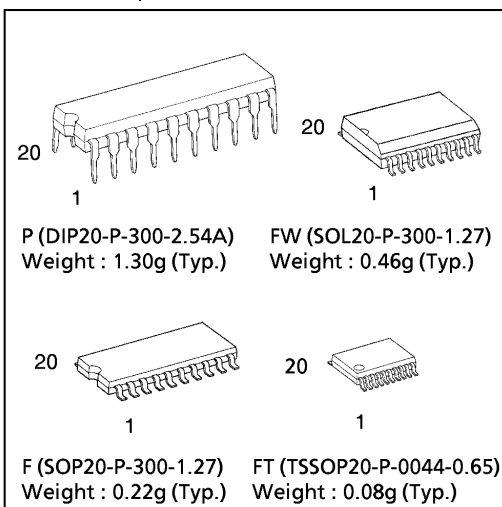
When the ($\overline{OE}$) input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

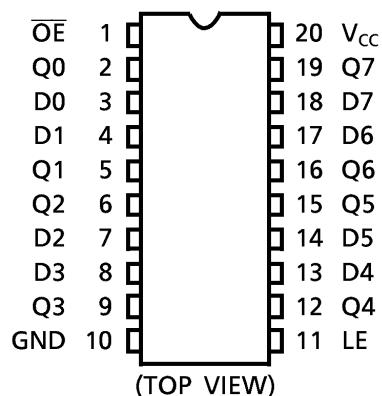
FEATURES:

- High Speed..... $t_{pd} = 5.2\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs..... $V_{IL} = 0.8\text{V}(\text{Max.})$
 $V_{IH} = 2.0\text{V}(\text{Min.})$
- Symmetrical Output Impedance..... $|I_{OH}| = |I_{OL}| = 24\text{mA}(\text{Min.})$
 Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{PLH} \approx t_{PHL}$
- Pin and Function Compatible with 74F373

(Note) The JEDEC SOP (FW) is not available in Japan.



PIN ASSIGNMENT



TRUTH TABLE

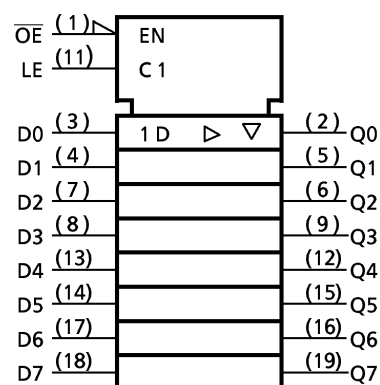
INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X : Don't Care

Z : High Impedance

Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

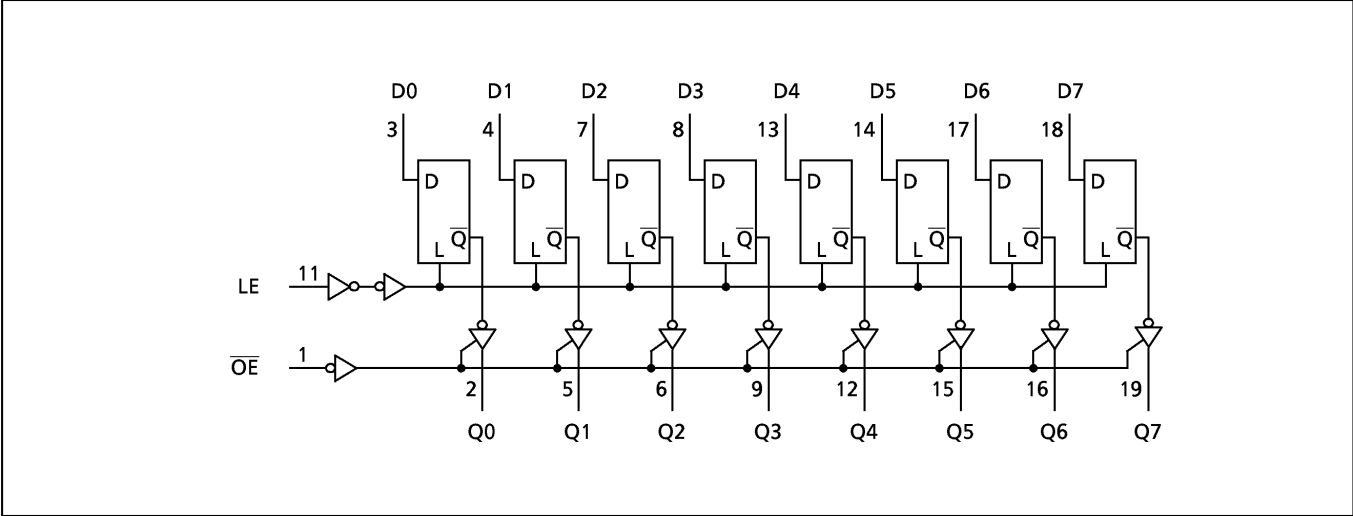
IEC LOGIC SYMBOL



961001EBA2

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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	0~10	ns/V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\mu\text{A}$ $I_{OH} = -24\text{mA}$ $I_{OH} = -75\text{mA}^*$	4.5 4.5 5.5	4.4 3.94 —	4.5 — —	— — —	4.4 3.80 3.85	— — —	V
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50\mu\text{A}$ $I_{OL} = 24\text{mA}$ $I_{OL} = 75\text{mA}^*$	4.5 4.5 5.5	— — —	0.0 — —	0.1 0.36 —	— — —	0.1 0.44 1.65	V
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } GND$		5.5	—	—	± 0.5	—	± 5.0	μA
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } GND$		5.5	—	—	± 0.1	—	± 1.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } GND$		5.5	—	—	8.0	—	80.0	
	I_C	PER INPUT : $V_{IN} = 3.4\text{V}$ OTHER INPUT : $V_{CC} \text{ or } GND$		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		$T_a = 25^\circ\text{C}$	$T_a = 25^\circ\text{C}$	$T_a = -40 \sim 85^\circ\text{C}$	UNIT
				V_{CC}	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_W (H)$			5.0 ± 0.5	—	5.0	ns
Minimum Set - up Time	t_s			5.0 ± 0.5	—	2.0	
Minimum Hold Time	t_h			5.0 ± 0.5	—	3.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.
Propagation Delay Time (LE—Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.8	9.2	1.0	10.5
Propagation Delay Time (D—Q)	t_{pLH} t_{pHL}		5.0 ± 0.5	—	5.9	9.6	1.0	11.0
Output Enable Time	t_{pZL} t_{pZH}		5.0 ± 0.5	—	6.5	10.5	1.0	12.0
Output Disable Time	t_{pLZ} t_{pHZ}		5.0 ± 0.5	—	5.5	7.8	1.0	9.0
Input Capacitance	C _{IN}			—	5	10	—	10
Output Capacitance	C _{OUT}			—	10	—	—	—
Power Dissipation Capacitance	C _{PD} (1)			—	32	—	—	—

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

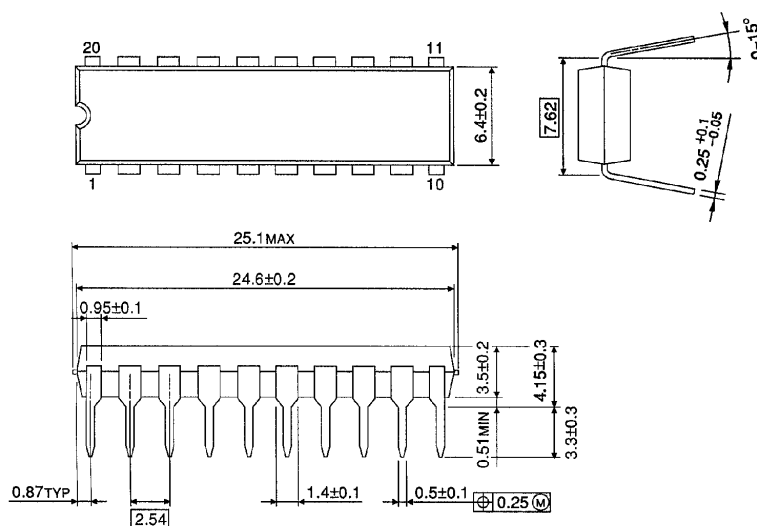
$$I_{\text{CC}}(\text{opr.}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/8 \text{ (per Latch)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{\text{PD}}(\text{total}) = 20 + 12 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

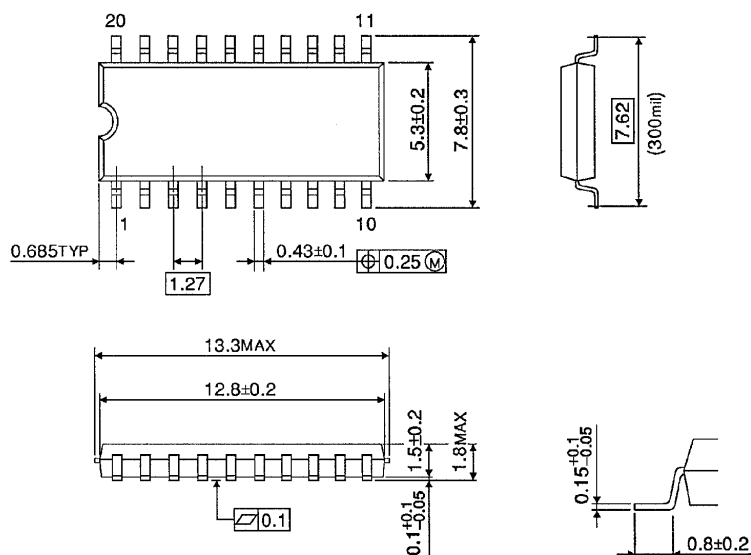
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

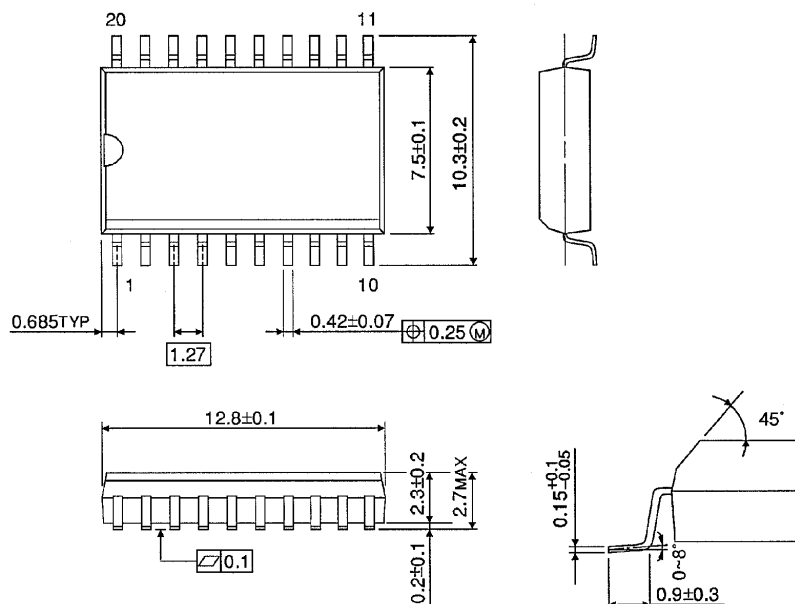


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)

Unit in mm

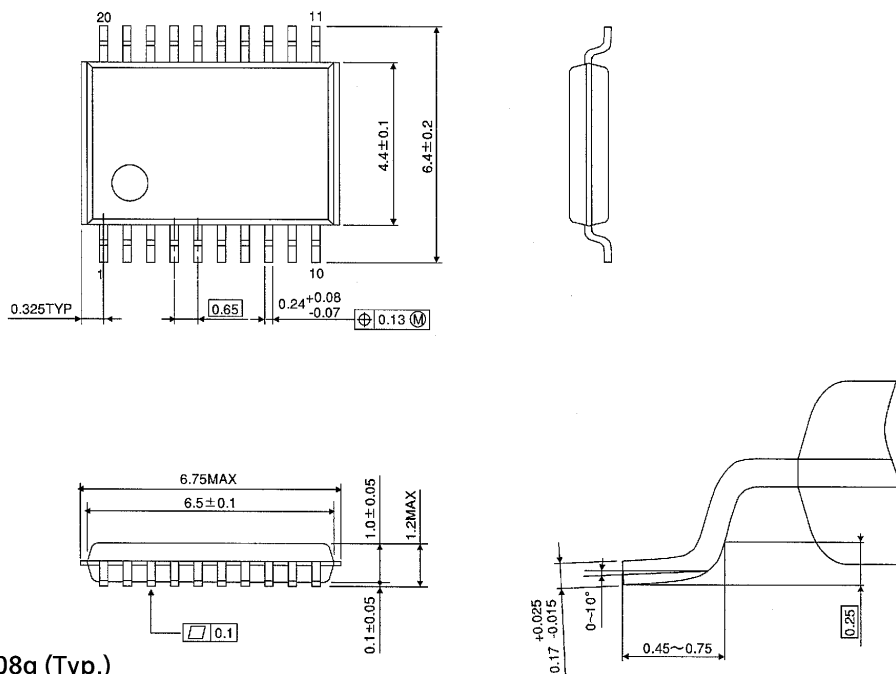
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)