# S6A2067

## 80 SEG DRIVER FOR STN LCD

Jan. 2002.

Ver. 0.1



**Precautions for Light**

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

## INTRODUCTION

The S6A2067 is a LCD driver IC which is fabricated by low power CMOS technology. Basically this LSI consists of 40 x 2 bit bi-directional shift register, 40 x 2 bit data latch and 40 x 2 bit LCD driver (refer to Figure 1). This IC can be used as segment driver.

## FUNCTION

— Dot matrix LCD driver with 80 channel output.

— Input/Output signal
  – Output: 40 x 2 channel waveform for LCD driving
  – Input: Serial display data and control signal pulse from the controller IC.
    Bias voltage (V1 to V4)

## FEATURES

— Display driving bias: static - 1/5

— Power supply voltage: 2.7V to 5.5V

— Supply voltage for display: 3.0V to 13.0V ($V_{LCD} = V_{DD} - V_{EE}$)

— Interface

| Driver (cascade connection) | Controller |
|---|---|
| S6A0065, Other S6A2067 | S6A0069<br>S6A0070<br>S6A0073 |

— CMOS Process

— 100QFP or bare chip available

## BLOCK DIAGRAM

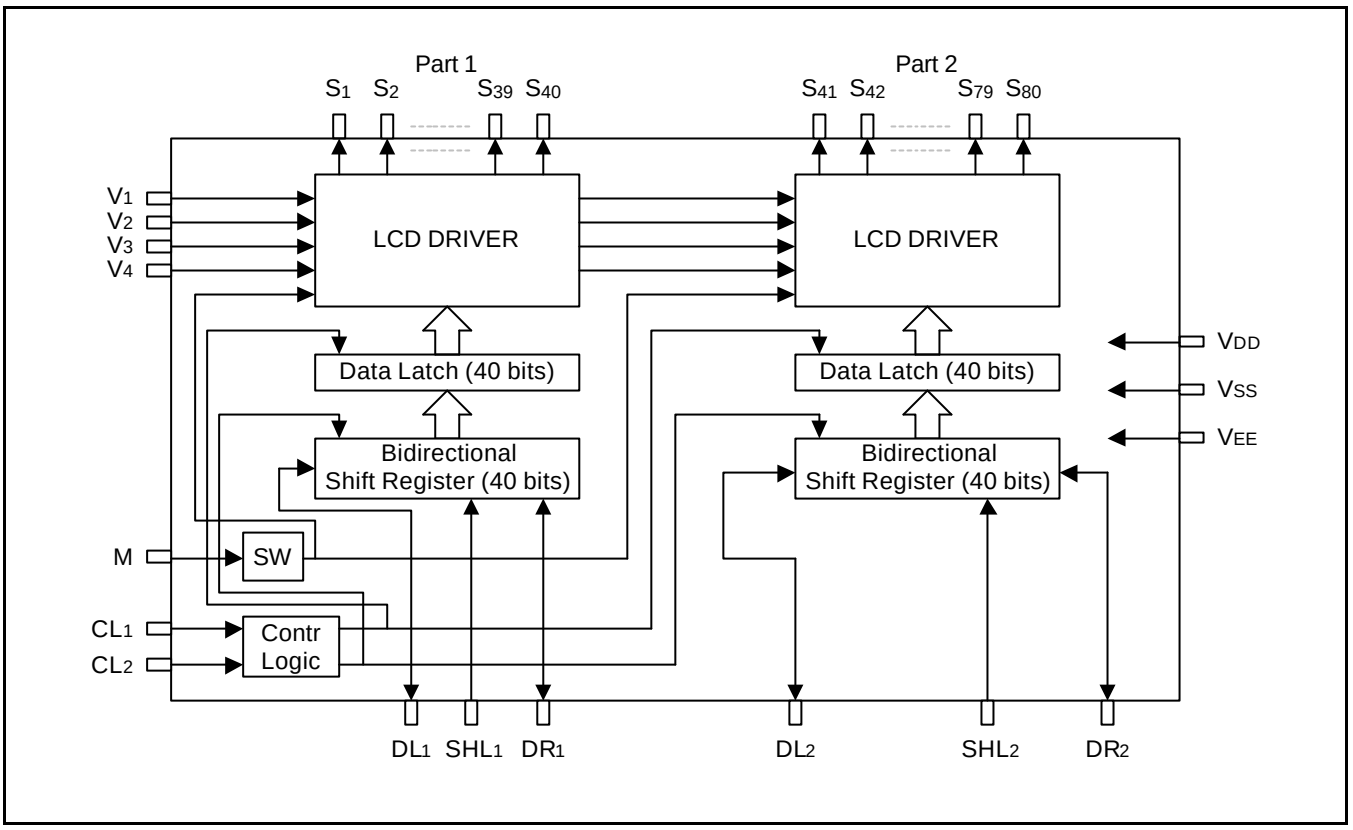



**Figure 1. S6A2067 Functional Block Diagram**

## PIN CONFIGURATION

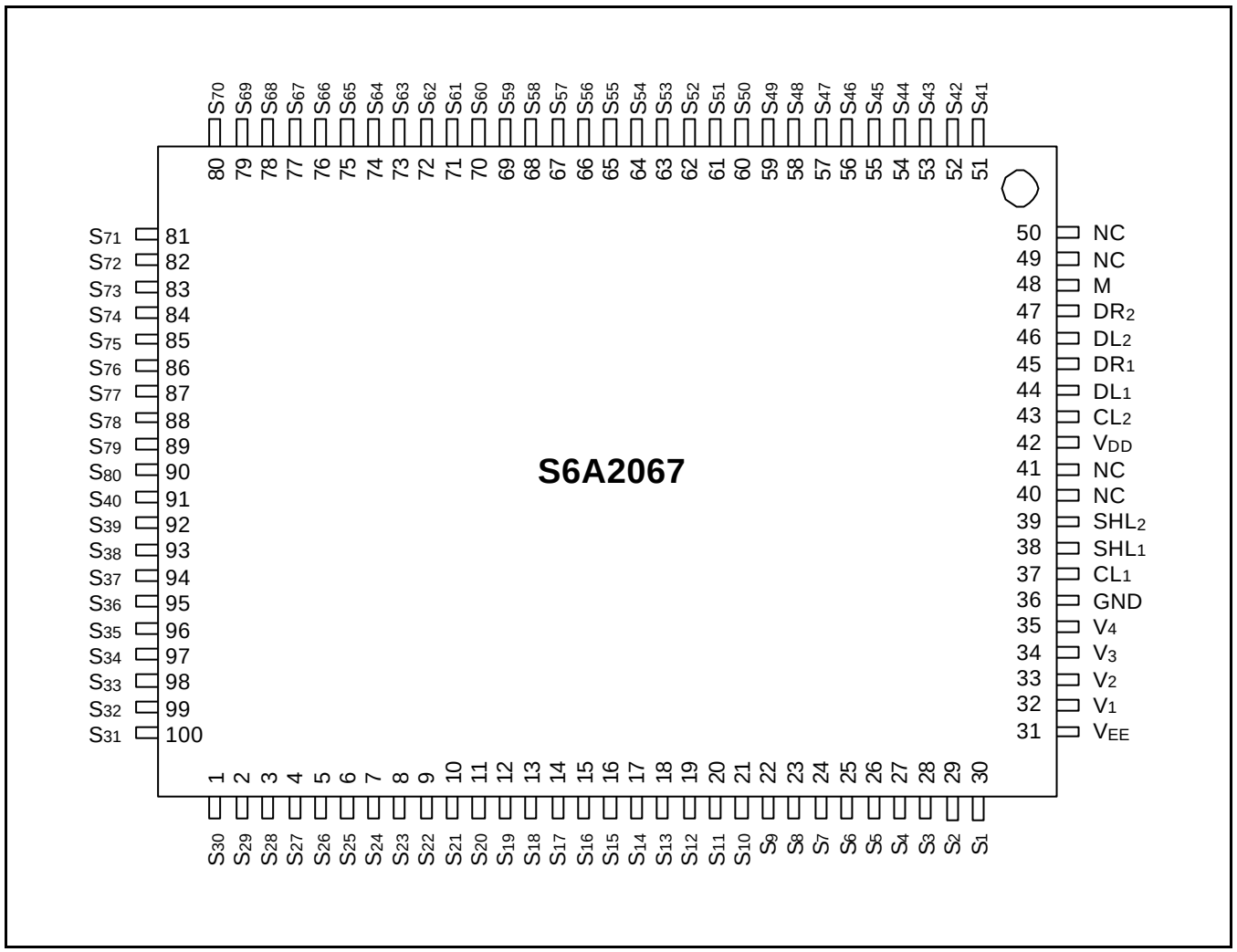
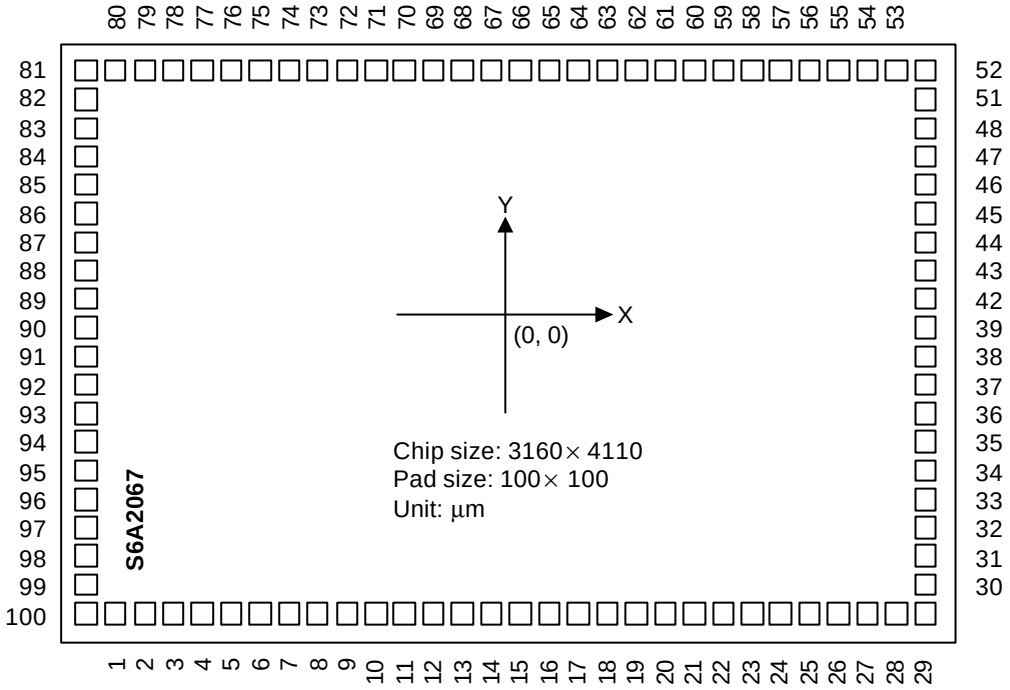



**Figure 2. 100 QFP Top View**

## PAD DIAGRAM


80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53
81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100
52 51 48 47 46 45 44 43 42 39 38 37 36 35 34 33 32 31 30
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
Y
X
(0, 0)
S6A2067
Chip size: 3160× 4110
Pad size: 100× 100
Unit: µm

## PAD CENTER COORDINATES

| Pad | Pad | Coordinate | | Pad | Pad | Coordinate | | Pad | Pad | Coordinate | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Num. | Name | X | Y | Num. | Name | X | Y | Num. | Name | X | Y |
| 1 | S30 | -1352 | 1687 | 33 | V2 | -712 | -1827 | 69 | S59 | 1352 | 312 |
| 2 | S29 | -1352 | 1562 | 34 | V3 | -587 | -1827 | 70 | S60 | 1352 | 437 |
| 3 | S28 | -1352 | 1437 | 35 | V4 | -462 | -1827 | 71 | S61 | 1352 | 562 |
| 4 | S27 | -1352 | 1312 | 36 | V5 | -313 | -1827 | 72 | S62 | 1352 | 687 |
| 5 | S26 | -1352 | 1187 | 37 | CL1 | -188 | -1827 | 73 | S63 | 1352 | 812 |
| 6 | S25 | -1352 | 1062 | 38 | SHL1 | -63 | -1827 | 74 | S64 | 1352 | 937 |
| 7 | S24 | -1352 | 937 | 39 | SHL2 | 62 | -1827 | 75 | S65 | 1352 | 1062 |
| 8 | S23 | -1352 | 812 | 42 | VDD | 187 | -1827 | 76 | S66 | 1352 | 1187 |
| 9 | S22 | -1352 | 687 | 43 | CL2 | 312 | -1827 | 77 | S67 | 1352 | 1312 |
| 10 | S21 | -1352 | 562 | 44 | DL1 | 437 | -1827 | 78 | S68 | 1352 | 1437 |
| 11 | S20 | -1352 | 437 | 45 | DR1 | 562 | -1827 | 79 | S69 | 1352 | 1562 |
| 12 | S19 | -1352 | 312 | 46 | DL2 | 687 | -1827 | 80 | S70 | 1352 | 1687 |
| 13 | S18 | -1352 | 187 | 47 | DR2 | 812 | -1827 | 81 | S71 | 1352 | 1812 |
| 14 | S17 | -1352 | 62 | 48 | M | 937 | -1827 | 82 | S72 | 1062 | 1827 |
| 15 | S16 | -1352 | -63 | 51 | S41 | 1086 | -1827 | 83 | S73 | 937 | 1827 |
| 16 | S15 | -1352 | -188 | 52 | S42 | 1352 | -1813 | 84 | S74 | 812 | 1827 |
| 17 | S14 | -1352 | -313 | 53 | S43 | 1352 | -1688 | 85 | S75 | 687 | 1827 |
| 18 | S13 | -1352 | -438 | 54 | S44 | 1352 | -1563 | 86 | S76 | 562 | 1827 |
| 19 | S12 | -1352 | -563 | 55 | S45 | 1352 | -1438 | 87 | S77 | 437 | 1827 |
| 20 | S11 | -1352 | -688 | 56 | S46 | 1352 | -1313 | 88 | S78 | 312 | 1827 |
| 21 | S10 | -1352 | -813 | 57 | S47 | 1352 | -1188 | 89 | S79 | 187 | 1827 |
| 22 | S9 | -1352 | -938 | 58 | S48 | 1352 | -1063 | 90 | S80 | 62 | 1827 |
| 23 | S8 | -1352 | -1063 | 59 | S49 | 1352 | -938 | 91 | S40 | -63 | 1827 |
| 24 | S7 | -1352 | -1188 | 60 | S50 | 1352 | -813 | 92 | S39 | -188 | 1827 |
| 25 | S6 | -1352 | -1313 | 61 | S51 | 1352 | -688 | 93 | S38 | -313 | 1827 |
| 26 | S5 | -1352 | -1438 | 62 | S52 | 1352 | -563 | 94 | S37 | -438 | 1827 |
| 27 | S4 | -1352 | -1563 | 63 | S53 | 1352 | -438 | 95 | S36 | -563 | 1827 |
| 28 | S3 | -1352 | -1688 | 64 | S54 | 1352 | -313 | 96 | S35 | -688 | 1827 |
| 29 | S2 | -1352 | -1813 | 65 | S55 | 1352 | -188 | 97 | S34 | -813 | 1827 |
| 30 | S1 | -1087 | -1827 | 66 | S56 | 1352 | -63 | 98 | S33 | -938 | 1827 |
| 31 | VEE | -962 | -1827 | 67 | S57 | 1352 | 62 | 99 | S32 | -1063 | 1827 |
| 32 | V1 | -837 | -1827 | 68 | S58 | 1352 | 187 | 100 | S31 | -1352 | 1827 |

**NOTE:** S6A2067 Marking: easy to find the PAD No.6, No.90.

## PIN DESCRIPTION

<table>
<tr><th>PIN (NO.)</th><th>I/O</th><th colspan="2">Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>$V_{DD}$(42)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (2.7 - .5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>$V_{SS}$(GND)(36)</td><td>0V (GND)</td></tr>
<tr><td>$V_{EE}$(31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V1, V2(32,33)</td><td>Input</td><td colspan="2" rowspan="2">LCD driver output voltage level</td><td>Bias voltage level for LCD drive (Select level)</td><td rowspan="2">Power</td></tr>
<tr><td>V3, V4(34,35)</td><td>Input</td><td>Bias voltage level for LCD drive (Non-select level)</td></tr>
<tr><td>S1 - S40</td><td>Output</td><td rowspan="3">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL1(38)</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of shift register<br><table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>VDD</td><td>OUT</td><td>IN</td></tr><tr><td>VSS</td><td>IN</td><td>OUT</td></tr></table></td><td>$V_{DD}$ or $V_{SS}$</td></tr>
<tr><td>DL1, DR1 (44,45)</td><td>Input Output</td><td>Data Input/output of shift register (part 1)</td><td>Controller or S6A2067/ S6A0065</td></tr>
<tr><td>S41 - S80</td><td>Output</td><td rowspan="3">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>SHL2 (39)</td><td>Input</td><td>Data Interface</td><td>Selection of the shift direction of shift register<br><table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>VDD</td><td>OUT</td><td>IN</td></tr><tr><td>VSS</td><td>IN</td><td>OUT</td></tr></table></td><td>$V_{DD}$ or $V_{SS}$</td></tr>
<tr><td>DL2, DR2 (46,47)</td><td>Input Output</td><td>Data Input/output of shift register (part 2)</td><td>Controller or S6A2067/ S6A0065</td></tr>
<tr><td>M(48)</td><td>Input</td><td></td><td>Alternated signal for LCD driver output</td><td>The alternating signal to convert LCD drive waveform to AC</td><td rowspan="2">Controller</td></tr>
<tr><td>CL1, CL2 (37,43)</td><td>Input</td><td></td><td>Data shift/ latch clock</td><td>CL1 : Data latch clock<br>CL2 : Data shift clock</td></tr>
<tr><td>NC (40,41,49,50)</td><td></td><td></td><td></td><td>No connection</td><td>NC</td></tr>
</table>

## MAXIMUM ABSOLUTE LIMIT

($T_A$ = 25°C)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Operating Voltage | $V_{DD}$ | -0.3 - +7.0 | V |
| Driver Supply Voltage | $V_{LCD}$ | $V_{DD}$-15.0 - $V_{DD}$+0.3 | V |
| Input Voltage 1 | $V_{IN1}$ | -0.3 - $V_{DD}$+0.3 | V |
| Input Voltage 2 (V1 - V4) | $V_{IN2}$ | $V_{DD}$+0.3 - $V_{EE}$-0.3 | V |
| Operating Temperature | $T_{OPR}$ | -30 - +85 | °C |
| Storage Temperature | $T_{STG}$ | -55 - +125 | °C |

**NOTES:**
1. Voltage greater than above may damage the circuit
2. $V_{EE}$: connect a protection resistor (220Ω ±5%)

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{DD}$ = 2.7 to 5.5V, $V_{DD}$-$V_{EE}$ = 3 - 13V, $V_{SS}$ = 0V, $T_A$ = -30 to 85°C)

| Characteristic | Symbol | Test condition | Min | Max | Unit | Applicable pin |
|---|---|---|---|---|---|---|
| Operating Current | $I_{DD}$ | $f_{CL2}$ = 400kHz | – | 1 | mA | $V_{DD}$, $V_{EE}$ |
| Supply Current | $I_{EE}$ | $f_{CL1}$ = 1kHz | – | 10 | µA | |
| Input High Voltage | $V_{IH}$ | – | 0.7$V_{DD}$ | $V_{DD}$ | V | CL1, $CL_2$,$DL_1$, |
| Input Low Voltage | $V_{IL}$ | | 0 | 0.3$V_{DD}$ | | $DL_2$, $DR_1$, $DR_2$, |
| Input Leakage Current | $I_{LKG}$ | $V_{IN}$ = 0 - $V_{DD}$ | -5 | 5 | µA | SHL1, SHL2, M |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -0.4mA | VDD-0.4 | – | V | $DL_1$, $DL_2$, |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = +0.4mA | | 0.4 | | $DR_1$, $DR_2$ |
| Voltage Descending | $V_{D1}$ | $I_{ON}$ = 0.1mA for one of S1 - S80 | – | 1.1 | | V (V1-V4)-S (S1-S80) |
| | $V_{D2}$ | $I_{ON}$ = 0.05mA for each S1 - S80 | – | 1.5 | | |
| Leakage Current | $I_V$ | $V_{IN}$ = $V_{DD}$ - $V_{EE}$ (Output S1 - S80: floating) | -10 | 10 | µA | V1 - V4 |

### AC Characteristics

($V_{DD}$ = 2.7 to 5.5V, $V_{DD}$-$V_{EE}$ = 3 - 13V, $V_{SS}$ = 0V, $T_A$ = -30 to 85°C)

| Characteristic | Symbol | Test condition | Min | Max | Unit | Applicable pin |
|---|---|---|---|---|---|---|
| Data Shift Frequency | $f_{CL}$ | – | – | 400 | kHz | CL2 |
| Clock High Level Width | $t_{WCKH}$ | – | 800 | – | ns | CL1, CL2 |
| Clock Low Level Width | $t_{WCKL}$ | – | 800 | – | | CL2 |
| Clock Set-up Time | $t_{SL}$ | from $CL_2$ to $CL_1$ | 500 | – | | CL1,CL2 |
| | $t_{LS}$ | from $CL_1$ to $CL_2$ | 500 | – | | |
| Clock Rise/Fall Time | $t_R/t_F$ | – | – | 200 | | |
| Data Set-up Time | $t_{SU}$ | – | 300 | – | | DL1,DL2,DR1,DR2 |
| Data Hold Time | $t_{DH}$ | – | 300 | – | | DL1,DL2,DR1,DR2 |
| Data Delay Time | $t_D$ | $C_L$ = 15pF | – | 500 | | DL1,DL2,DR1,DR2 |

## TIMING CHARACTERISTICS

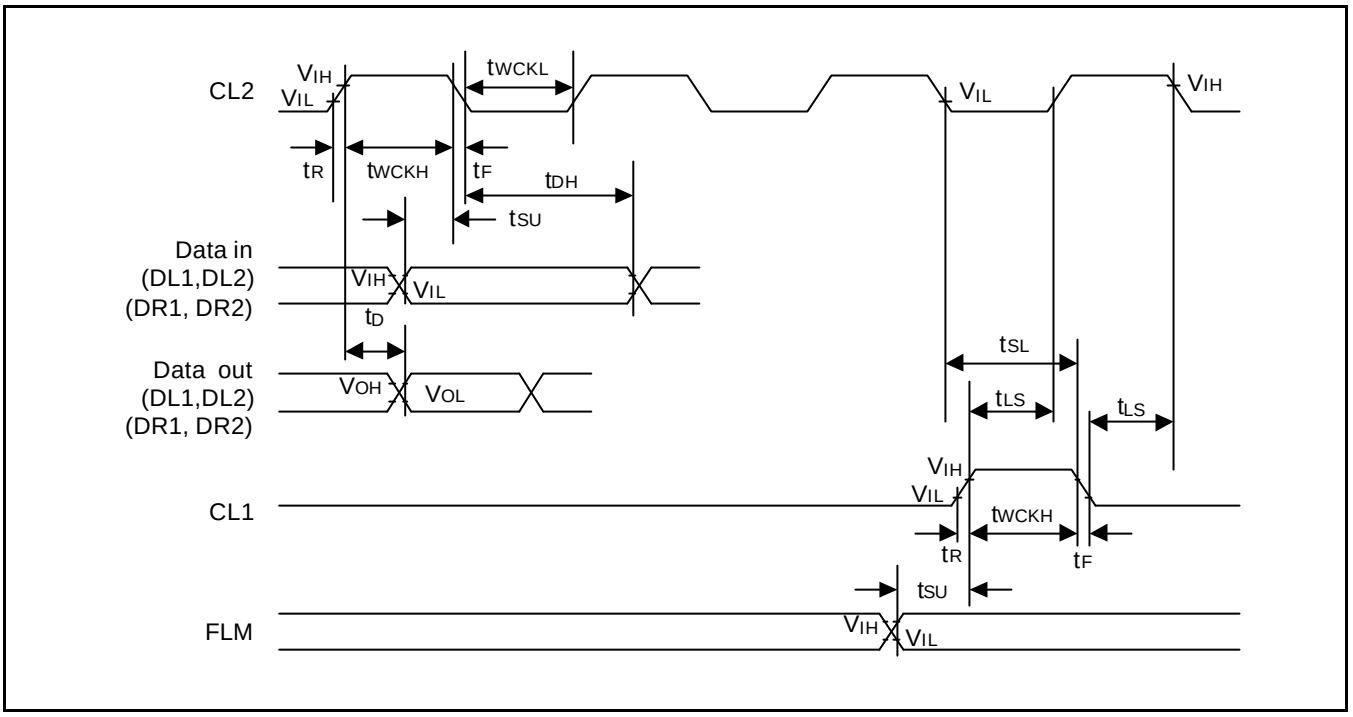
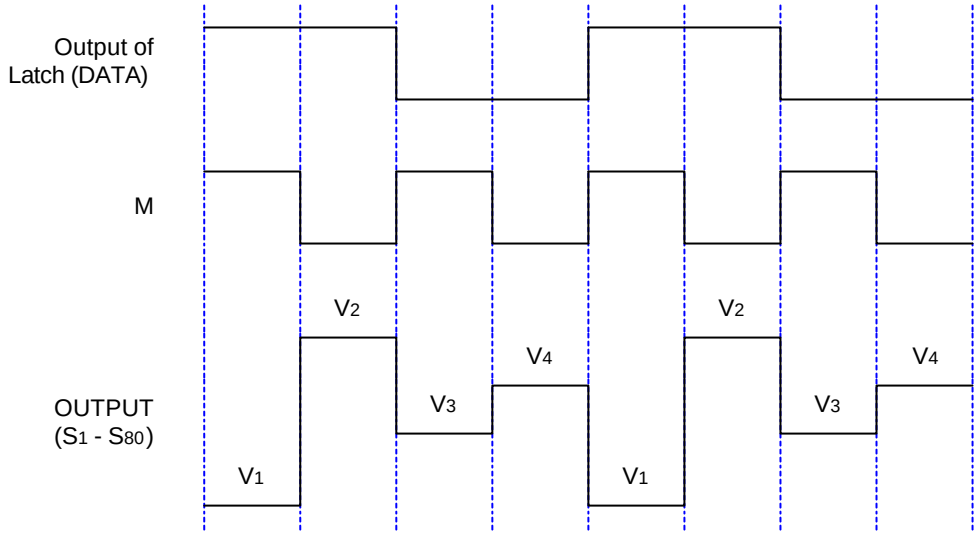



**Figure 3. AC Characteristics**

## LCD OUTPUT WAVEFORMS



## APPLICATION CIRCUIT