

M5M5V416BWG

PRELIMINARY

Notice: This is not a final specification.
Some parametric limits are subject to change

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM**DESCRIPTION**

The M5M5V416B is a family of low voltage 4-Mbit static RAMs organized as 262,144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.25μm CMOS technology.

The M5M5V416B is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5V416BWG is packaged in a CSP (chip scale package), with the outline of 7mm x 8.5mm, ball matrix of 6 x 8 (48pin) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

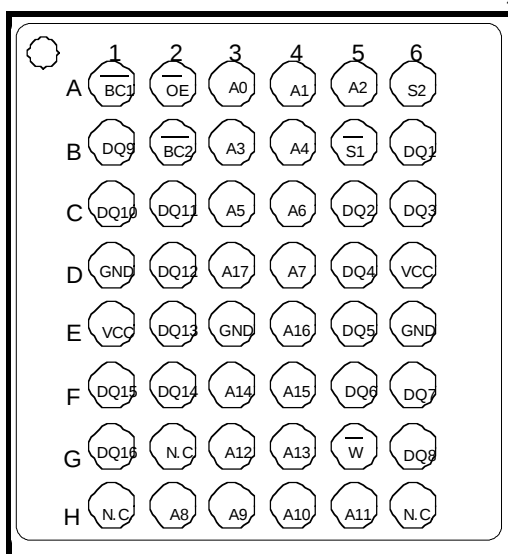
From the point of operating temperature, the family is divided into three versions; "Standard", "W-version", and "I-version".

Those are summarized in the part name table below.

FEATURES

- Single +2.7~+3.6V power supply
- Small stand-by current: 0.3μA(3V,typ.)
- No clocks, No refresh
- Data retention supply voltage =2.0V to 3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by $\overline{S1}$, $S2$, $\overline{BC1}$ and $\overline{BC2}$
- Common Data I/O
- Three-state outputs: OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Process technology: 0.25μm CMOS
- Package: 48pin 7mm x 8.5mm CSP

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current I _{cc} (PD), V _{cc} =3.0V						Active current I _{cc1} (3.0V, typ.)
				typical *		Ratings (max.)				
				25°C	40°C	25°C	40°C	70°C	85°C	
Standard 0 ~ +70°C	M5M5V416BWG -70L	2.7 ~ 3.6V	70ns	---	---	---	---	20μA	---	40mA (10MHz) 5mA (1MHz)
	M5M5V416BWG -85L		85ns							
	M5M5V416BWG -10L		100ns							
	M5M5V416BWG -70H	2.7 ~ 3.6V	70ns	0.3μA	1μA	1μA	3μA	10μA	---	
	M5M5V416BWG -85H		85ns							
	M5M5V416BWG -10H		100ns							
W-version -20 ~ +85°C	M5M5V416BWG -70LW	2.7 ~ 3.6V	70ns	---	---	---	---	20μA	40μA	
	M5M5V416BWG -85LW		85ns							
	M5M5V416BWG -10LW		100ns							
	M5M5V416BWG -70HW	2.7 ~ 3.6V	70ns	0.3μA	1μA	1μA	3μA	10μA	20μA	
	M5M5V416BWG -85HW		85ns							
	M5M5V416BWG -10HW		100ns							
I-version -40 ~ +85°C	M5M5V416WG -70LI	2.7 ~ 3.6V	70ns	---	---	---	---	20μA	40μA	
	M5M5V416BWG -85LI		85ns							
	M5M5V416BWG -10LI		100ns							
	M5M5V416BWG -70HI	2.7 ~ 3.6V	70ns	0.3μA	1μA	1μA	3μA	10μA	20μA	
	M5M5V416BWG -85HI		85ns							
	M5M5V416BWG -10HI		100ns							

**PIN CONFIGURATION
(TOP VIEW)**

Outline: 48FHA
NC: No Connection

* "typical" parameter is sampled, not 100% tested.

Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
$\overline{S1}$	Chip select input 1
$S2$	Chip select input 2
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
$\overline{BC1}$	Lower Byte (DQ1 ~ 8)
$\overline{BC2}$	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply



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FUNCTION

The M5M5V416BWG is organized as 262,144-words by 16-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

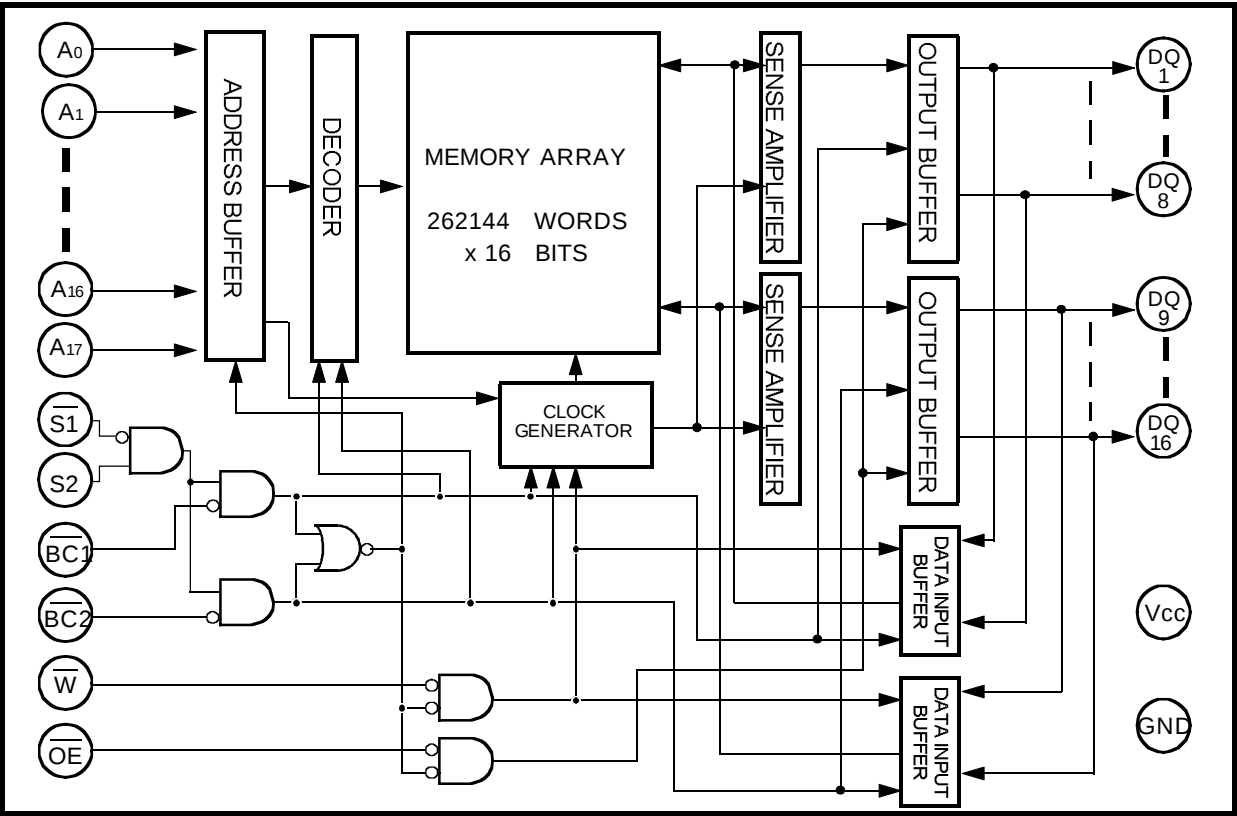
The operation mode are determined by a combination of the device control inputs $\overline{BC1}$, $\overline{BC2}$, $\overline{S1}$, $S2$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write operation is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{BC1}$ and/or $\overline{BC2}$ and the low level $\overline{S1}$ and the high level $S2$. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{BC1}$ and/or $\overline{BC2}$ and $\overline{S1}$ and $S2$ are in an active state($\overline{S1}=L, S2=H$).

When setting $\overline{BC1}$ at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting $\overline{BC2}$ at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

BLOCK DIAGRAM



When setting $\overline{BC1}$ and $\overline{BC2}$ at a high level or $\overline{S1}$ at a high level or $S2$ at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{BC1}$, $\overline{BC2}$ and $\overline{S1}$, $S2$.

The power supply current is reduced as low as 0.3μA(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S1}$	$S2$	$\overline{BC1}$	$\overline{BC2}$	$\overline{W}$	$\overline{OE}$	Mode	DQ1-8	DQ9-16	Icc
H	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
L	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	—	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	—	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	—	High-Z	High-Z	Active

M5M5V416BWG**PRELIMINARY**Notice: This is not a final specification.
Some parametric limits are subject to change**4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM****ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Units
V _{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V _I	Input voltage	With respect to GND	-0.5* ~ V _{CC} + 0.5	
V _O	Output voltage	With respect to GND	0 ~ V _{CC}	
P _d	Power dissipation	T _a =25°C	700	mW
T _a	Operating temperature	Standard (-L, -H)	0 ~ +70	°C
		W-version (-LW, -HW)	-20 ~ +85	
		I-version (-LI, -HI)	-40 ~ +85	
T _{stg}	Storage temperature		-65 ~ +150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units		
			Min	Typ	Max			
V _{IH}	High-level input voltage		2.2		V _{CC} +0.3V	V		
V _{IL}	Low-level input voltage		-0.3 *		0.6			
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA	2.4					
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA	V _{CC} -0.5V					
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4			
I _I	Input leakage current	V _I =0 ~ V _{CC}			±1	μA		
I _O	Output leakage current	$\overline{BC1}$ and $\overline{BC2}$ =V _{IH} or $\overline{S1}$ =V _{IH} or S2=V _{IH} or $\overline{OE}$ =V _{IH} , V _{I/O} =0 ~ V _{CC}			±1			
I _{CC1}	Active supply current (AC,MOS level)	$\overline{BC1}$ and $\overline{BC2}$ ≤ 0.2V, $\overline{S1}$ ≤ 0.2V, S2≥ V _{CC} -0.2V other inputs ≤0.2V or ≥ V _{CC} -0.2V Output - open (duty 100%)	f = 10MHz	-	40	50	mA	
			f = 1MHz	-	5	10		
I _{CC2}	Active supply current (AC,TTL level)	$\overline{BC1}$ and $\overline{BC2}$ =V _{IL} , $\overline{S}$ =V _{IL} ,S2=V _{IH} other pins =V _{IH} or V _{IL} Output - open (duty 100%)	f = 10MHz	-	40	50		
			f = 1MHz	-	5	10		
I _{CC3}	Stand by supply current (AC,MOS level)	< 1 > $\overline{S1}$ ≥ V _{CC} - 0.2V, other inputs = 0 ~ V _{CC} < 2 > S2 ≤0.2V, other inputs = 0 ~ V _{CC} < 3 > $\overline{BC1}$ and $\overline{BC2}$ ≥ V _{CC} - 0.2V $\overline{S1}$ ≤ 0.2V, S2 ≥ V _{CC} - 0.2V Other inputs=0~V _{CC}	-LW, -LI	+70 ~ +85°C	-	-	48	μA
			-L, -LW, -LI	+70°C	-	-	24	
			-HW, -HI	+70 ~ +85°C	-	-	24	
			-H, -HW, -HI	+40 ~ +70°C	-	-	12	
				+25 ~ +40°C	-	1	3.6	
			-H	0 ~ +25°C	-	0.3	1.2	
			-HW	- 20 ~ +25°C	-	0.3	1.2	
			-HI	- 40 ~ +25°C	-	0.3	1.2	
I _{CC4}	Stand by supply current (AC,TTL level)	$\overline{BC1}$ and $\overline{BC2}$ =V _{IH} or $\overline{S1}$ =V _{IH} or S2=V _{IL} Other inputs= 0 ~ V _{CC}	-	-	0.5	mA		

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

* -3.0V in case of AC (Pulse width ≤ 30ns)

Note 2: Typical value is for V_{CC}=3.0V and T_a=25°C**CAPACITANCE**(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			10	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	

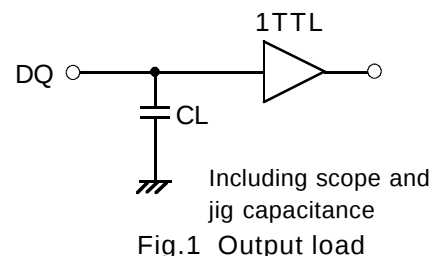


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4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM**AC ELECTRICAL CHARACTERISTICS**(V_{CC}=2.7 ~ 3.6V, unless otherwise noted)**(1) TEST CONDITIONS**

Supply voltage	2.7V~3.6V
Input pulse	V _{IH} =2.4V, V _{IL} =0.4V
Input rise time and fall time	5ns
Reference level	V _{OH} =V _{OL} =1.5V Transition is measured ±500mV from steady state voltage.(for t _{en} , t _{dis})
Output loads	Fig.1, CL=30pF CL=5pF (for t _{en} , t _{dis})

**(2) READ CYCLE**

Symbol	Parameter	Limits						Units
		70L,70H,70LW 70HW,70LI,70HI		85L,85H,85LW 85HW,85LI,85HI		10L,10H,10LW 10HW,10LI,10HI		
		Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	70		85		100		ns
t _a (A)	Address access time		70		85		100	ns
t _a (S1)	Chip select 1 access time		70		85		100	ns
t _a (S2)	Chip select 2 access time		70		85		100	ns
t _a (BC1)	Byte control 1 access time		70		85		100	ns
t _a (BC2)	Byte control 2 access time		70		85		100	ns
t _a (OE)	Output enable access time		35		45		50	ns
t _{dis} (S1)	Output disable time after S1 high		25		30		35	ns
t _{dis} (S2)	Output disable time after S2 low		25		30		35	ns
t _{dis} (BC1)	Output disable time after BC1 high		25		30		35	ns
t _{dis} (BC2)	Output disable time after BC2 high		25		30		35	ns
t _{dis} (OE)	Output disable time after OE high		25		30		35	ns
t _{en} (S1)	Output enable time after S1 low	10		10		10		ns
t _{en} (S2)	Output enable time after S2 high	10		10		10		ns
t _{en} (BC1)	Output enable time after BC1 low	10		10		10		ns
t _{en} (BC2)	Output enable time after BC2 low	10		10		10		ns
t _{en} (OE)	Output enable time after OE low			5		5		ns
t _v (A)	Data valid time after address	10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits						Units
		70L,70H,70LW 70HW,70LI,70HI		85L,85H,85LW 85HW,85LI,85HI		10L,10H,10LW 10HW,10LI,10HI		
		Min	Max	Min	Max	Min	Max	
t _{cw}	Write cycle time	70		85		100		ns
t _{w(W)}	Write pulse width	55		60		75		ns
t _{su(A)}	Address setup time	0		0		0		ns
t _{su(A-WH)}	Address setup time with respect to $\overline{W}$	65		70		85		ns
t _{su(BC1)}	Byte control 1 setup time	65		70		85		ns
t _{su(BC2)}	Byte control 2 setup time	65		70		85		ns
t _{su(S1)}	Chip select 1 setup time	65		70		85		ns
t _{su(S2)}	Chip select 2 setup time	65		70		85		ns
t _{su(D)}	Data setup time	35		35		40		ns
t _{h(D)}	Data hold time	0		0		0		ns
t _{rec(W)}	Write recovery time	0		0		0		ns
t _{dis(W)}	Output disable time from $\overline{W}$ low		25		30		35	ns
t _{dis(OE)}	Output disable time from $\overline{OE}$ high		25		30		35	ns
t _{en(W)}	Output enable time f from $\overline{W}$ high	5		5		5		ns
t _{en(OE)}	Output enable time f from $\overline{OE}$ low	5		5		5		ns



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(4)TIMING DIAGRAMS

Read cycle

The diagram illustrates the timing relationships for a read cycle. The signals and their timing parameters are as follows:

- A0~17**: Address bus. Timing parameters: t_{CR} (Read cycle time), $t_a(A)$ (Address setup time), $t_v(A)$ (Address hold time).
- BC1, BC2**: Bank/Column address strobes. Timing parameters: $t_a(BC1)$ or $t_a(BC2)$ (Setup time), $t_{dis}(BC1)$ or $t_{dis}(BC2)$ (Hold time). (Note3)
- S1**: Sense amplifier enable. Timing parameters: $t_a(S1)$ (Setup time), $t_{dis}(S1)$ (Hold time). (Note3)
- S2**: Sense amplifier enable. Timing parameters: $t_a(S2)$ (Setup time), $t_{dis}(S2)$ (Hold time). (Note3)
- OE**: Output enable. Timing parameters: $t_a(OE)$ (Setup time), $t_{dis}(OE)$ (Hold time). (Note3)
- W = "H" level**: Write enable. Timing parameters: $t_{en}(OE)$ (Output enable delay), $t_{dis}(OE)$ (Output enable hold time). (Note3)
- DQ1~16**: Data bus. Timing parameters: $t_{en}(BC1)$, $t_{en}(BC2)$, $t_{en}(S1)$, $t_{en}(S2)$ (Setup times), $t_{dis}(BC1)$, $t_{dis}(BC2)$, $t_{dis}(S1)$, $t_{dis}(S2)$ (Hold times). (Note3)
- VALID DATA**: Period during which data is valid on the data bus.

Write cycle (W control mode)

The diagram illustrates the timing relationships for a write cycle in W control mode. The signals and their timing parameters are as follows:

- A0-17:** Address bus. Timing parameter: t_{cw} (Write Cycle Width).
- BC1, BC2:** Bank/Column address strobes. Timing parameter: $t_{su}(BC1) \text{ or } t_{su}(BC2)$.
- S1:** Sense amplifier enable. Timing parameter: $t_{su}(S1)$.
- S2:** Sense amplifier enable. Timing parameter: $t_{su}(S2)$.
- OE:** Output Enable. Timing parameters: $t_{su}(A-WH)$, $t_{w}(W)$, $t_{rec}(W)$, $t_{dis}(OE)$, $t_{en}(OE)$.
- W:** Write Enable. Timing parameters: $t_{su}(A)$, $t_{dis}(W)$, $t_{en}(W)$.
- DQ1-16:** Data bus. Timing parameters: $t_{dis}(OE)$, $t_{su}(D)$, $t_{th}(D)$.

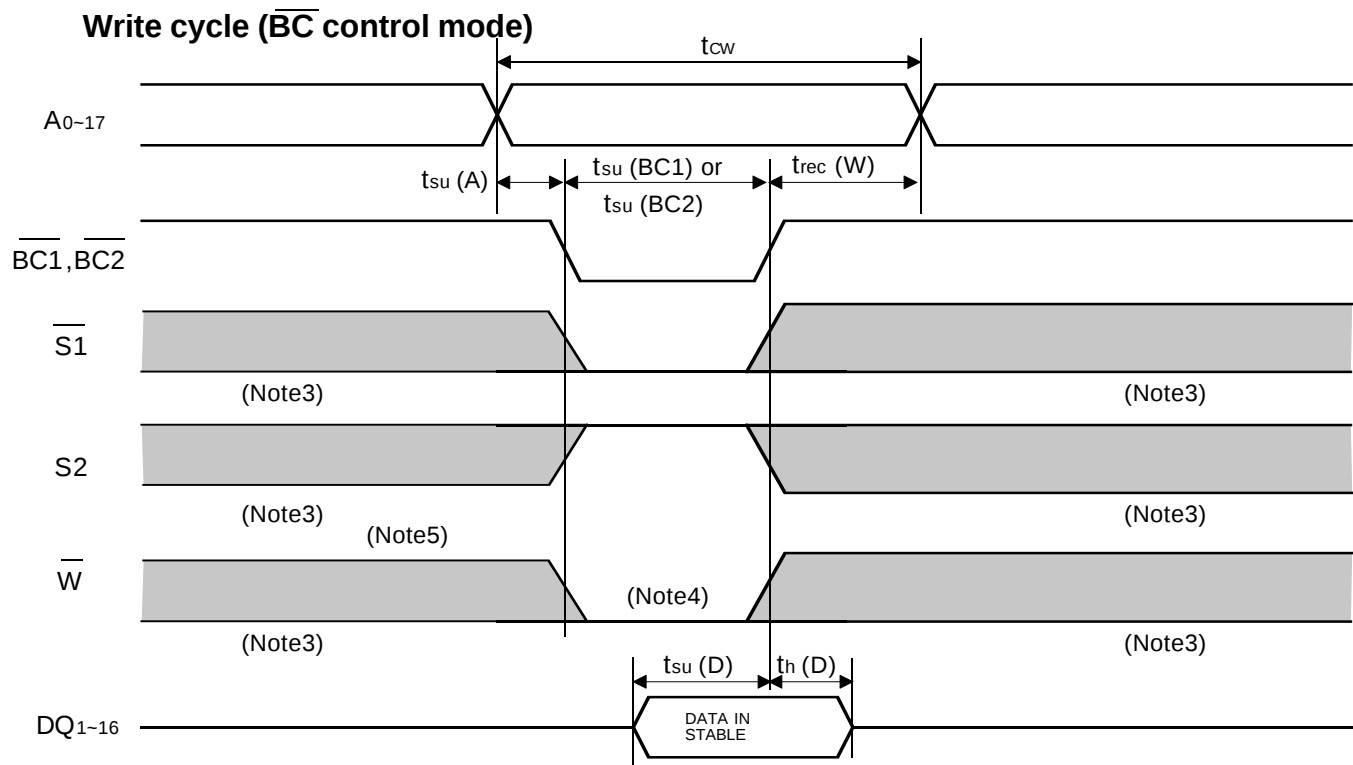
Additional labels include (Note3) for several signals and "DATA IN STABLE" for the data bus during the write cycle.

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Note 3: Hatching indicates the state is "don't care".
Note 4: A Write occurs during $\overline{S1}$ low, $S2$ high overlaps $\overline{BC1}$ and/or $\overline{BC2}$ low and $\overline{W}$ low.
Note 5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{BC1}$ and/or $\overline{BC2}$ or the falling edge of $\overline{S1}$ or rising edge of $S2$, the outputs are maintained in the high impedance state.
Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

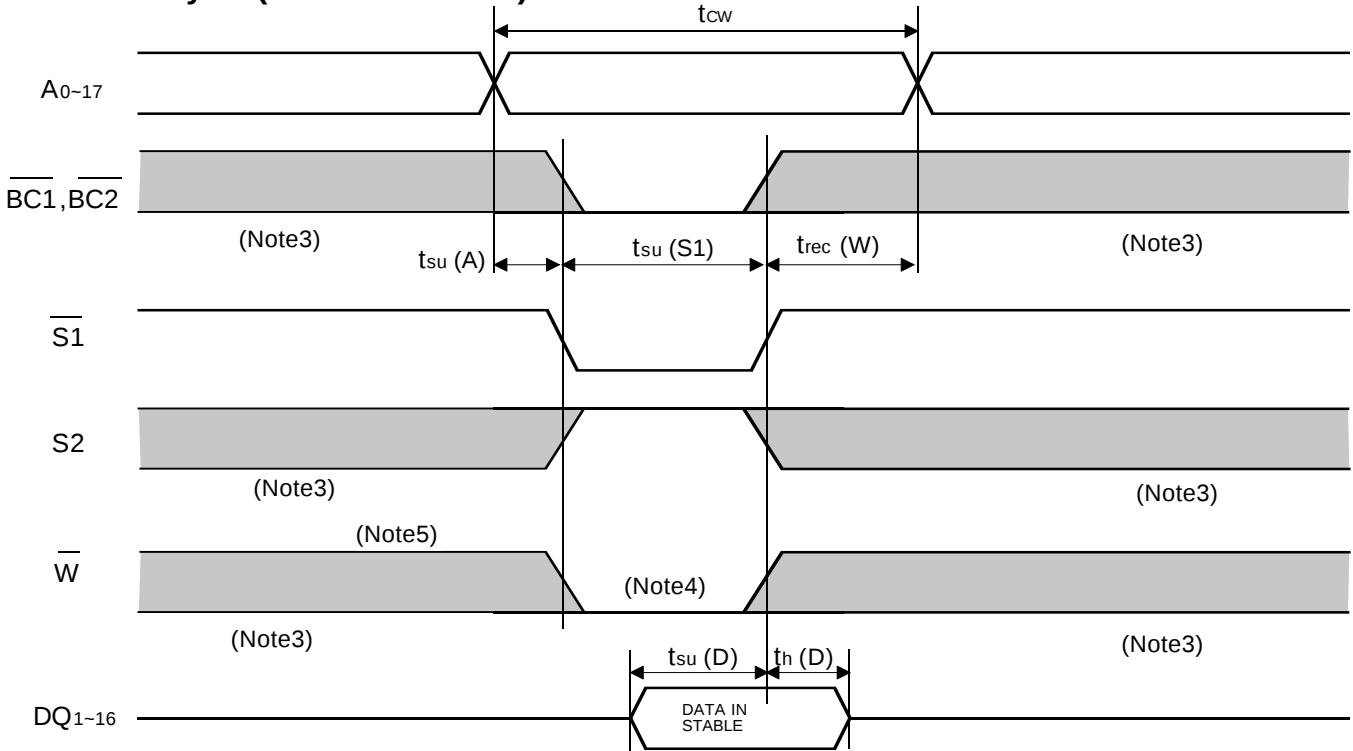
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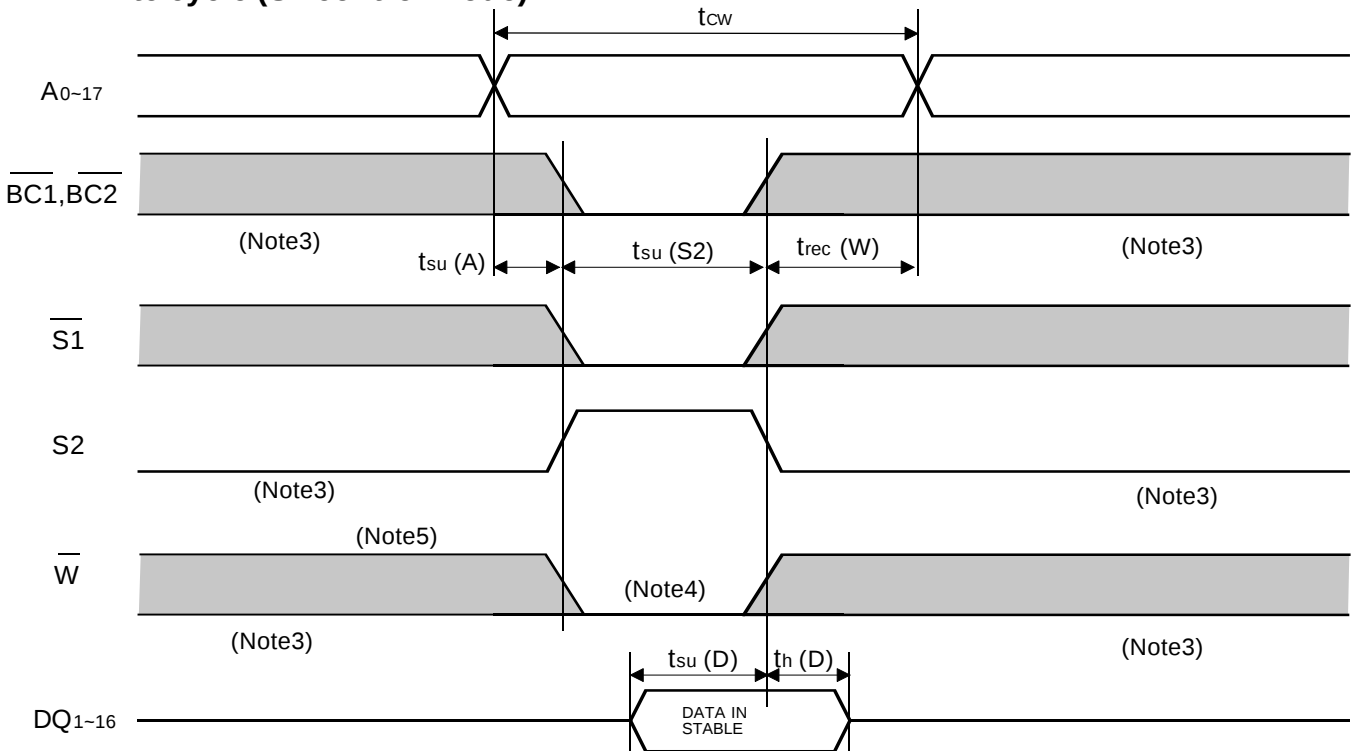
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Write cycle ($\overline{S1}$ control mode)



Write cycle ($\overline{S2}$ control mode)



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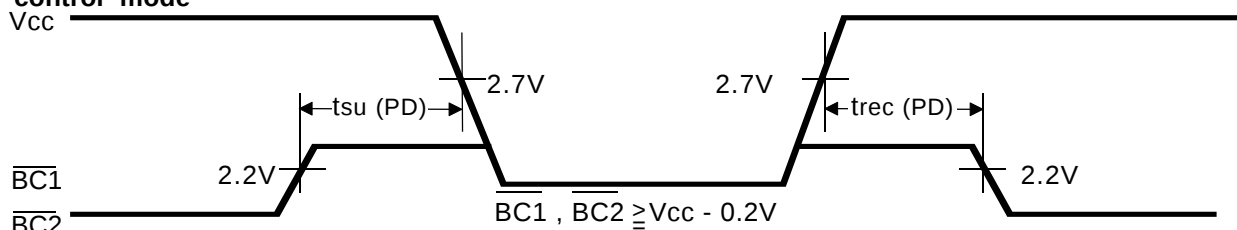
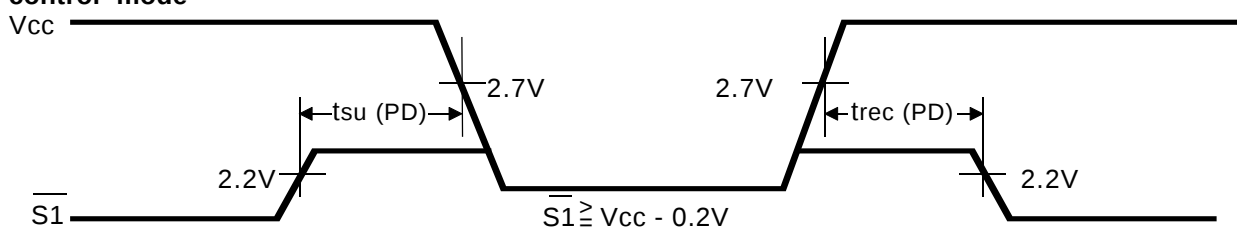
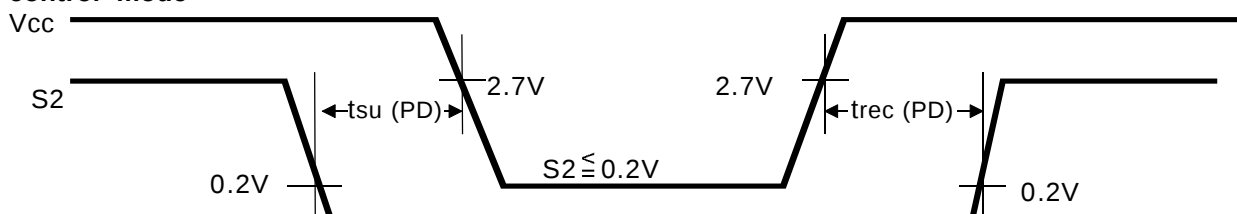
4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM**POWER DOWN CHARACTERISTICS****(1) ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test conditions			Limits			Units
					Min	Typ	Max	
VCC (PD)	Power down supply voltage				2.0			V
VI (BC)	Byte control input $\overline{BC1}$ & $\overline{BC2}$				2.0			V
VI ($\overline{S1}$)	Chip select input $\overline{S1}$				2.0			V
VI (S2)	Chip select input S2						0.2	V
ICC (PD)	Power down supply current	Vcc=3.0V 1) $\overline{BC1}$ and $\overline{BC2} \geq V_{cc}-0.2V$ $S1 \leq 0.2V$ or $S2 \geq V_{cc}-0.2V$ other inputs=0~3V 2) $S1 \geq V_{cc} - 0.2V$ other inputs=0~3V 3) $S2 \leq 0.2V$ other inputs=0~3V	-LW, -LI	+70 ~ +85°C	-	-	40	μA
			-L, -LW, -LI	+70°C	-	-	20	μA
			-HW, -HI	+70 ~ +85°C	-	-	20	μA
			-H, -HW, -HI	+40 ~ +70°C	-	-	10	μA
				+25 ~ +40°C	-	1	3	μA
			-H	0 ~ +25°C	-	0.3	1	μA
			-HW	-20 ~ +25°C	-	0.3	1	μA
			-HI	-40 ~ +25°C	-	0.3	1	μA

Typical value is for Ta=25°C

(2) TIMING REQUIREMENTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM **$\overline{BC}$ control mode** **$\overline{S1}$ control mode****S2 control mode**

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Revision History

<u>Revision No.</u>	<u>History</u>	<u>Date</u>	<u>Remark</u>
W01	The first edition	'98 . 07 . 23	Preliminary
W02	Font problem fixed	'98 . 08 . 27	Preliminary
W03	70ns version added	'98 . 12 . 16	Preliminary



48FHA

48pin 7.0X8.5mm body M-CSP

EIAJ Package Code	JEDEC Code	Weight(g)
-	-	

