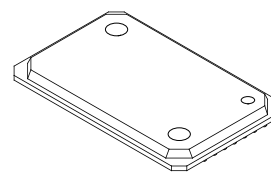


Description

The CXK77V1840GB is a high speed CMOS synchronous static RAM with common I/O pins, organized as 262,144-words by 18-bits. This synchronous SRAM integrates input registers, high speed SRAM and output registers onto a single monolithic IC. All input signals except $\overline{OE}$ are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. Asynchronous $\overline{OE}$ adds the flexibility of data bus control. 125 MHz operation is obtained from a single 3.3 V power supply.

119 pin BGA (Plastic)



Features

- Fast cycle time:

	(Cycle)	(Frequency)
CXK77V1840GB-8	8 ns	125 MHz
CXK77V1840GB-10	10 ns	100 MHz
CXK77V1840GB-12	12 ns	83.3 MHz
- Fast clock to data valid

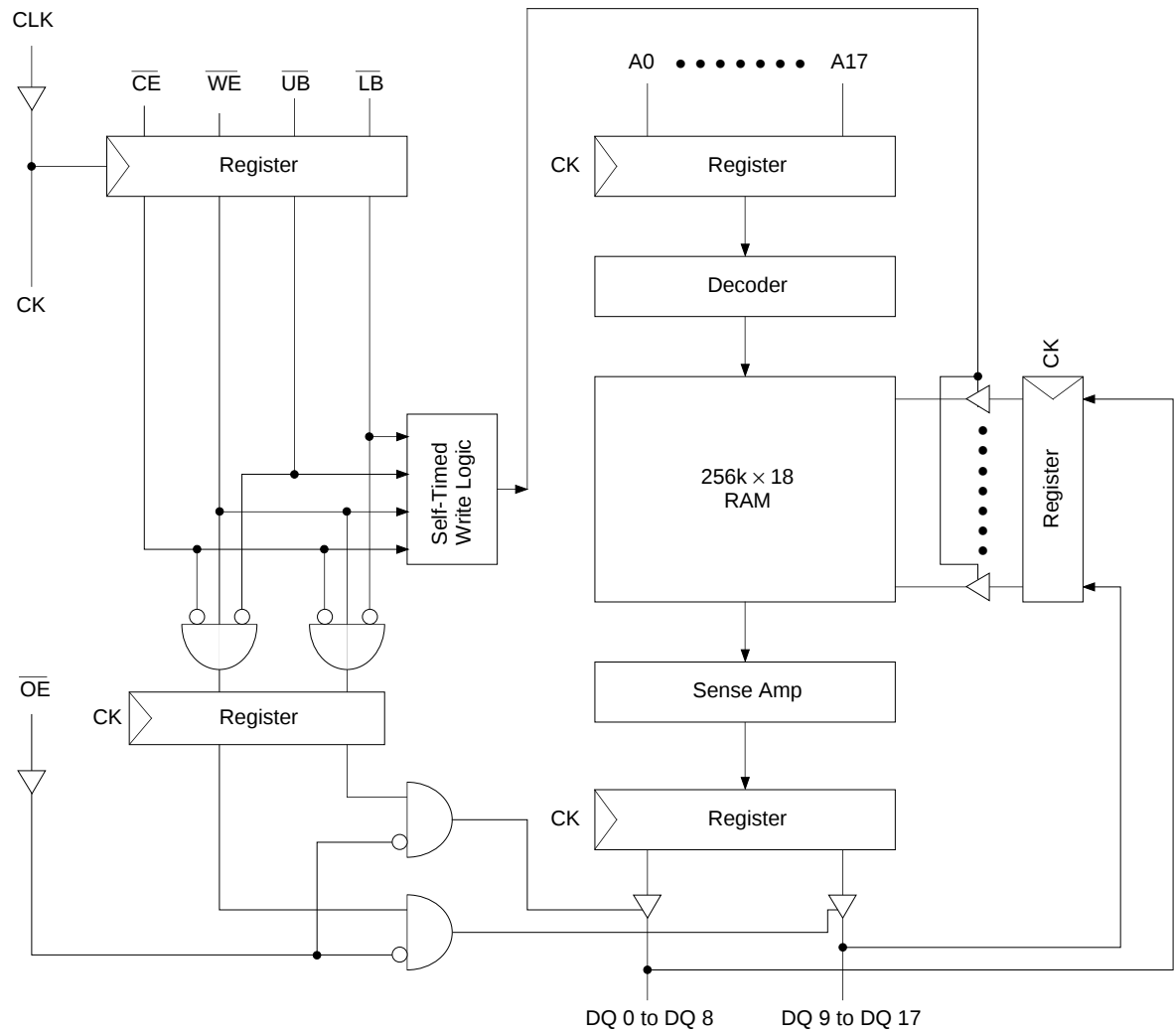
CXK77V1840GB-8	4 ns
CXK77V1840GB-10	5.5 ns
CXK77V1840GB-12	7.5 ns
- High speed, low power consumption
- Single +3.3 V power supply: 3.3 V +10 % –5 %
- Inputs and outputs are LVTTL/LVCMOS compatible
- Byte Select capability
- Asynchronous $\overline{OE}$
- Common data input and output
- All inputs (except $\overline{OE}$) and outputs are registered on a single clock edge
- Self-timed write cycle
- Package

CXK77V1840GB	7 × 17 Plastic Ball Grid Array with 50 mil pitch
--------------	--

Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)

CXK77V1840GB

	1	2	3	4	5	6	7
A	V _{DDQ}	A0	A2	NC	A5	A8	V _{DDQ}
B	NC	NC	A3	NC	A6	NC	NC
C	NC	A1	A4	V _{DD}	A7	A9	NC
D	DQ8	NC	V _{SS}	NC	V _{SS}	DQ9	NC
E	NC	DQ7	V _{SS}	$\overline{\text{CE}}$	V _{SS}	NC	DQ10
F	V _{DDQ}	NC	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQ11	V _{DDQ}
G	NC	DQ6	$\overline{\text{LB}}$	NC	V _{SS}	NC	DQ12
H	DQ5	NC	V _{SS}	NC	V _{SS}	DQ13	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQ4	V _{SS}	CLK	V _{SS}	NC	DQ14
L	DQ3	NC	V _{SS}	NC	$\overline{\text{UB}}$	DQ15	NC
M	V _{DDQ}	DQ2	V _{SS}	$\overline{\text{WE}}$	V _{SS}	NC	V _{DDQ}
N	DQ1	NC	V _{SS}	A13	V _{SS}	DQ16	NC
P	NC	DQ0	V _{SS}	A14	V _{SS}	NC	DQ17
R	NC	A16	NC	V _{DD}	NC	A10	NC
T	NC	A17	A15	NC	A12	A11	NC
U	V _{DDQ}	NC	NC	NC	NC	NC	V _{DDQ}

Pin Description

Symbol	Description	Symbol	Description
A0 to A17	Address input	CLK	Clock input
DQ0 to DQ8	Lower Byte Data input/output	$\overline{\text{LB}}$	Lower Byte enable input
DQ9 to DQ17	Upper Byte Data input/output	$\overline{\text{UB}}$	Upper Byte enable input
V _{DD}	+3.3 V power supply	$\overline{\text{CE}}$	Chip Enable input
V _{DDQ}	+3.3 V output power supply	$\overline{\text{WE}}$	Write Enable input
V _{SS}	Ground	$\overline{\text{OE}}$	Output Enable input

For proper operation, $V_{DD} \geq V_{DDQ}$ at all times including power up.

Absolute Maximum Ratings

(Ta=25 °C, GND=0 V)

Item	Symbol	Rating	Unit
Supply voltage	V _{DD}	−0.5 to +4.6	V
Input voltage	V _{IN}	−0.5 to V _{CC} +0.5 (4.6 V max.)	V
Output voltage	V _O	−0.5 to V _{CC} +0.5 (4.6 V max.)	V
Allowable power dissipation	P _D	1.7	W
Operating temperature	T _{opr}	0 to 70	°C
Storage temperature	T _{stg}	−55 to 150	°C
Soldering temperature time	T _{solder}	235 · 10	°C · sec

Truth Table

$\overline{\text{CE}}$ (t _n)	$\overline{\text{WE}}$ (t _n)	$\overline{\text{UB}}$ (t _n)	$\overline{\text{LB}}$ (t _n)	$\overline{\text{OE}}$	Mode	DQ0-17 (t _n)	DQ0-17 (t _n +1)	V _{DD} Current
H	X	X	X	X	Deselect	Don't care	Hi-Z	I _{SB}
L	H	X	X	H	Read, output Hi-z	Don't care	Hi-Z	I _{CC}
L	H	H	H	X				
L	H	L	L	L	Read bits 0-17	Don't care	DOUT (t _n)	I _{CC}
L	H	H	L	L	Read bits 0-8	Don't care	DOUT (t _n)	I _{CC}
L	H	L	H	L	Read bits 9-17	Don't care	DOUT (t _n)	I _{CC}
L	L	L	L	X	Write bits 0-17	Din (t _n)	Hi-Z	I _{CC}
L	L	H	L	X	Write bits 0-8	Din (t _n)	Hi-Z	I _{CC}
L	L	L	H	X	Write bits 9-17	Din (t _n)	Hi-Z	I _{CC}

DC Recommended Operating Conditions

(Ta=25 °C, GND=0 V)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DD}	3.135	3.3	3.6	V
Output supply voltage	V _{DDQ} *1	3.135	3.3	3.6	V
Input high voltage	V _{IH}	2.0	—	V _{DD} +0.3*2	V
Input low voltage	V _{IL}	−0.3*2	—	0.8	V

*1 V_{DDQ} must be ≤V_{DD} at all times including power up*2 V_{IL}=−1.5 V Min. and V_{IH}=V_{DD} +1.5 V for pulse width less than 5 ns.

Electrical Characteristics

• DC and Operating characteristics

(V_{DD}=3.3 V +10 % -5 %, GND=0 V, Ta=0 to 70 °C)

Item	Symbol	Test Conditions		Min	Typ* ¹	Max	Unit
Input leakage current	I _{LI}	V _{IN} =GND to V _{DD}		-1	—	1	μA
Output leakage current	I _{LO}	V _O =GND to V _{DD} $\overline{OE}$ =V _{IH}		-1	—	1	μA
Operating power supply current	I _{CC}	Cycle=min. Duty=100 % I _{out} =0 mA	-8	—	—	330* ²	mA
			-10	—	—	270* ²	
			-12	—	—	250* ²	
Standby Current	I _{SB}	$\overline{CE} \geq V_{IH}$ Cycle=min. Duty=100 % I _{out} =0 mA	-8	—	—	260* ²	mA
			-10	—	—	200* ²	
			-12	—	—	200* ²	
Output high voltage	V _{OH}	I _{OH} =-2.0 mA		2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.0 mA		—	—	0.4	V

*1 V_{DD}=3.3 V, Ta=25 °C

*2 For Address increment pattern only

• I/O capacitance

(Ta=25 °C, f=1 MHz)

Item	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0 V	—	7	pF
Output capacitance	C _{OUT}	V _{OUT} =0 V	—	10	pF
Clock input capacitance	C _{CLK}	V _{IN} =0 V	—	8	pF

Note) These parameters are sampled and are not 100 % tested.

• AC ELECTRICAL CHARACTERISTICS

Item	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Clock period	tCP	8	—	10	—	12	—	ns
Clock pulse high	tCH	2.5	—	3.5	—	4.5	—	ns
Clock pulse low	tCL	2.5	—	3.5	—	4.5	—	ns
Setup time	tS	1.5	—	2.5	—	3	—	ns
Hold time	tH	0.5	—	0.5	—	0.5	—	ns
Clock to output	tCQ	1	4	1	5.5	1	7.5	ns
Clock to output high impedance	tHZ*2	—	3.5	—	5	—	6	ns
Clock to output low impedance	tLZ*2	1	—	1	—	1	—	ns
OE to output	tOE	1	3.5	1	5	1	5	ns
OE to output high impedance	tOHZ*2	—	3.5	—	4.5	—	5.5	ns
OE to output low impedance	tOLZ*2	0.5	—	0.5	—	0.5	—	ns

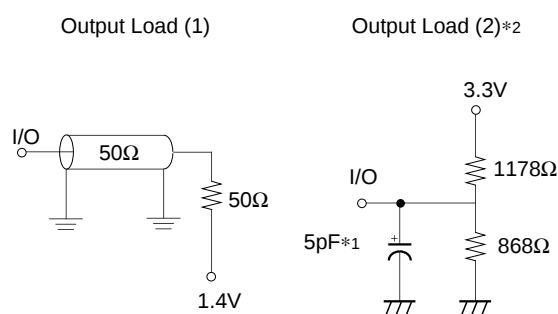
1. All parameters are specified over the range 0-70 °C
2. These parameters are measured at ± 200 mV from steady voltage with output load (2).
3. They are sampled and are not 100 % tested.

AC characteristics

• AC test conditions

($V_{DD}=3.3$ V ± 10 % -5 %, $T_a=0$ to 70 °C)

Item	Conditions
Input pulse high level	$V_{IH}=2.4$ V
Input pulse low level	$V_{IL}=0.4$ V
Input rise time	1 V/ns
Input fall time	1 V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load conditions	Fig. 1

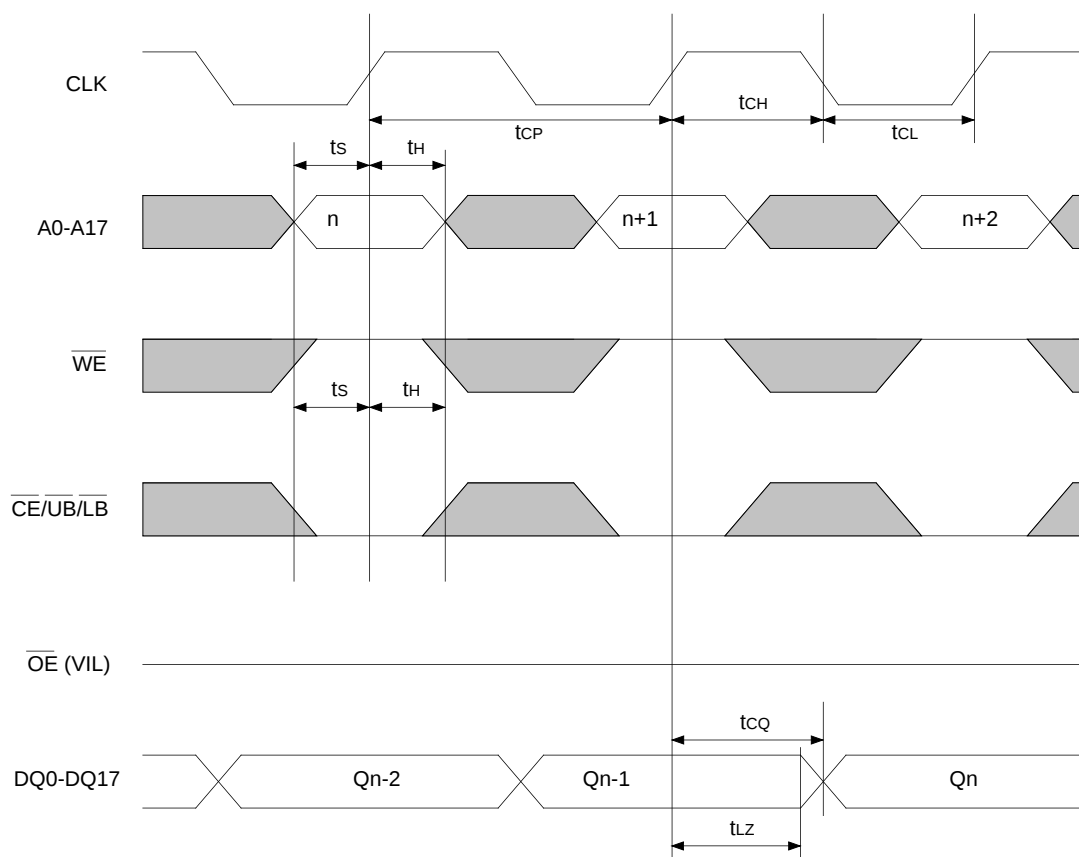


[*1] Including scope and jig capacitance.

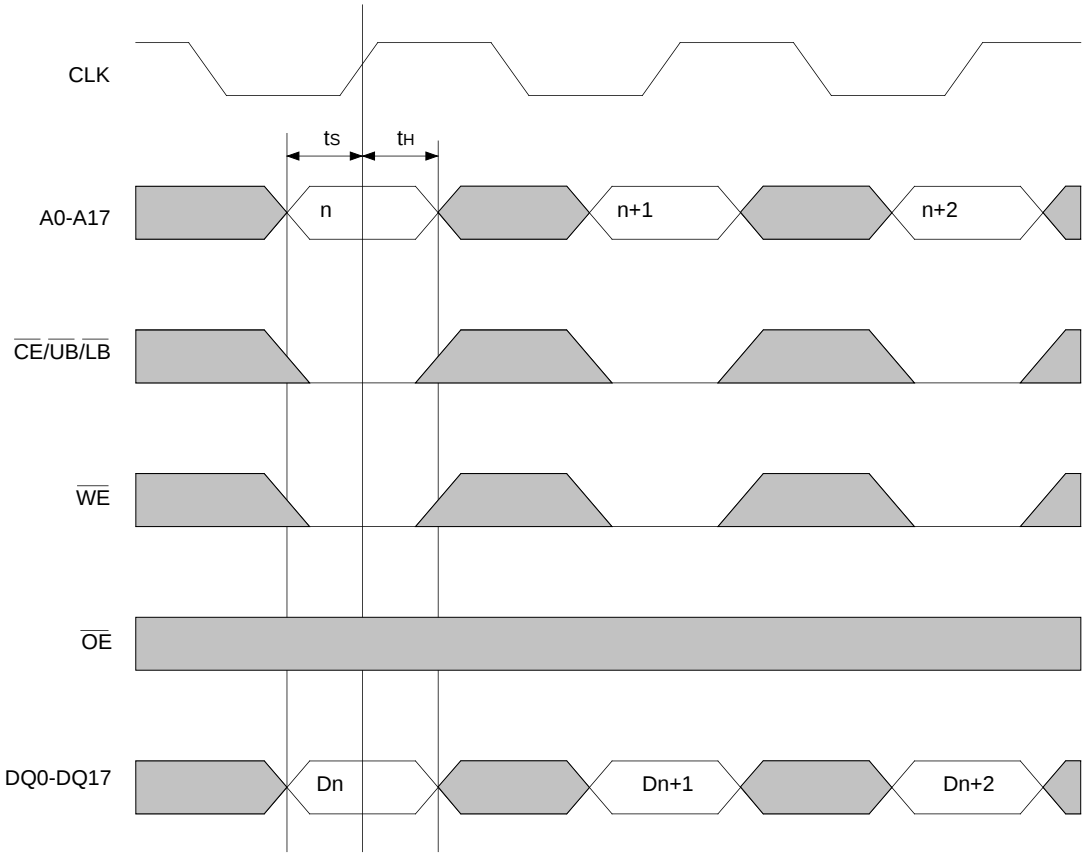
[*2] For tLZ, tHZ, tOLZ, tOHZ.

Timing Waveform

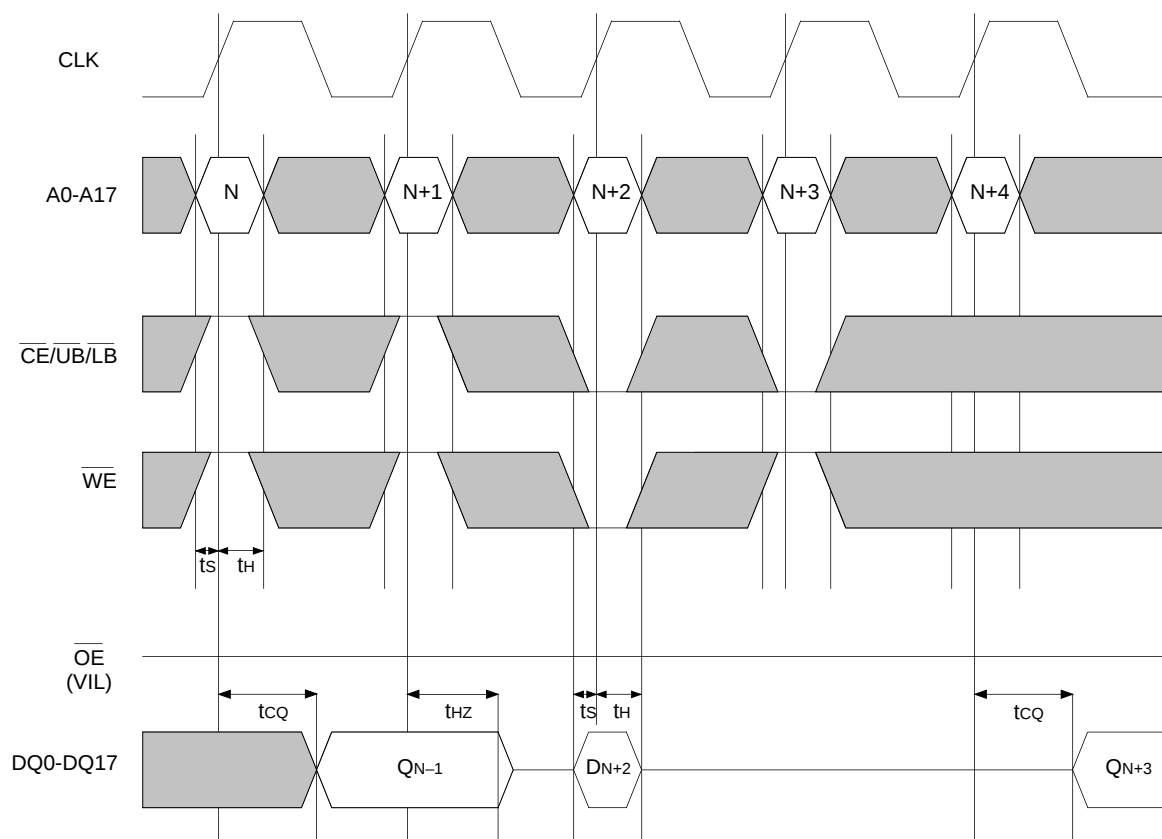
• Read Cycle



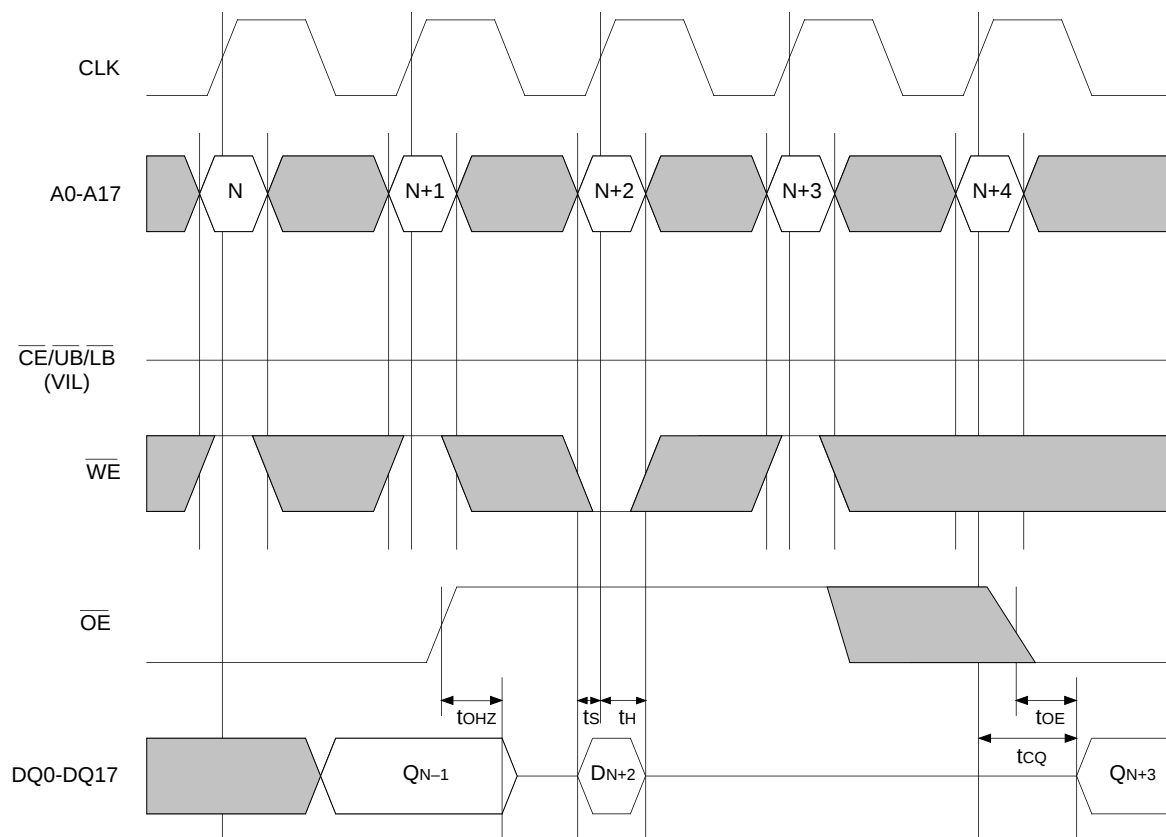
• Write Cycle



• Read/Write Cycle ($\overline{CE}/\overline{UB}/\overline{LB}$ control)

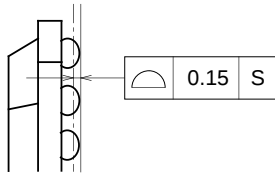
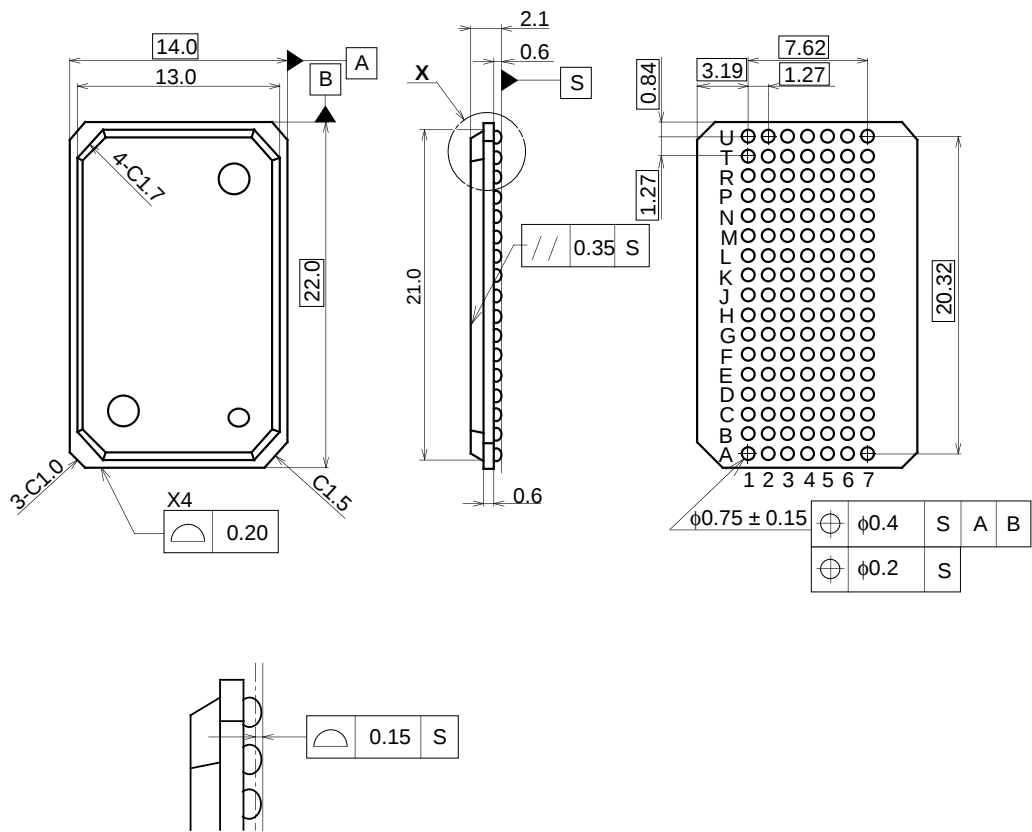


• Read/Write Cycle ($\overline{OE}$ control)



Package Outline Unit : mm

119 TERMINAL BGA (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	BGA-119P-02	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	BGA119-P-1422-1.27	LEAD TREATMENT	COPPER-CLAD LAMINATE
JEDEC CODE	_____	LEAD MATERIAL	SOLDER
		PACKAGE MASS	1.1g