

PRELIMINARY DATA SHEET

CDC1631F-E Automotive Controller

ARM

Edition Aug. 2, 2004
6251-617-1PD

 MICRONAS

Contents

Page	Section	Title
3	1.	Introduction
3	1.1.	Features
7	1.2.	Abbreviations
8	1.3.	Block Diagram
9	2.	Package and Pins
9	2.1.	Package Outline Dimensions
10	2.2.	Pin Assignment
11	2.3.	External Components
12	3.	Electrical Data
12	3.1.	Absolute Maximum Ratings
13	3.2.	Recommended Operating Conditions
14	3.3.	Characteristics
15	3.4.	Recommended Crystal Characteristics
16	4.	CPU, RAM, ROM and Banking
17	5.	Core Logic
17	5.1.	Control Register CR
18	6.	Interrupt Controller (IR)
18	6.1.	Interrupt Assignment
20	7.	Hardware Options
20	7.1.	Functional Description
20	7.2.	Listing of Dedicated Addresses and Corresponding Hardware Options
22	8.	Register Cross Reference Table
26	8.1.	Modified Registers
27	9.	Differences
28	10.	Data Sheet History

1. Introduction

Release Note: Revision bars indicate significant changes to the previous edition.

The device is a microcontroller for use in automotive applications. The on-chip CPU is a 65C816, an upgrade of the 65C02 with 16-bit internal data and 24-bit address bus. The chip consists of timer/counters, an interrupt controller, a multichannel A/D converter, a stepper motor and LCD driver, a UART and a CAN interface and PWM outputs. This document provides ROM hardware-specific information. General information on operating the IC can be found in the document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

1.1. Features

Table 1–1: CDC16xxF Family Feature List

This device:								
Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E Mask ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Core								
CPU	16-bit 65C816, featuring software compatibility with its 8-bit NMOS and CMOS 6502-series predecessors							
CPU-active operation modes	FAST, SLOW and DEEP SLOW			FAST and SLOW				
Power-saving operation modes (CPU inactive)	WAKE and IDLE			-				
EMI reduction mode	selectable in FAST mode							
Oscillators	4-MHz to 12-MHz quartz, RC			4-MHz to 12-MHz quartz				
RAM	6 Kbyte		2 Kbyte	6 Kbyte		2.75 Kbyte	4 Kbyte	6 Kbyte
ROM	ROMless, external program storage with up to 16 Mbyte, internal 2-Kbyte boot ROM	256-Kbyte Flash, bottom boot configuration, internal 2-Kbyte boot ROM	64 Kbyte	ROMless, external program storage with up to 16 Mbyte, internal 2-Kbyte boot ROM	256-Kbyte Flash, bottom boot configuration, internal 2-Kbyte boot ROM	90 Kbyte	128 Kbyte	216 Kbyte
Multiplier, 8 by 8 bit	✓			-				

Table 1–1: CDC16xxF Family Feature List, continued

This device:								
Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E Mask ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Digital watchdog	✓							
Central clock divider	✓							
Interrupt controller expanding NMI	16 inputs,15 priority levels							
Port interrupts including slope selection	4 inputs							
Port wake-up inputs including slope / level selection	10			-				
Patch module	10 ROM locations		5 ROM loca- tions	10 ROM locations		5 ROM loca- tions	6 ROM locations	
Boot system	allows in-system downloading of code and data into RAM via serial link		-	allows in-system downloading of code and data into RAM via serial link		-		
Analog								
Reset/Alarm	Combined input for regulator input supervision							
Clock and supply supervision	✓							
10-bit ADC, charge balance type	9 channels (5 channels selectable as digital input)							
ADC reference	VREF pin							
Comparators	P06COMP with 1/2 AVDD reference							
LCD	internal processing of all analog voltages for the LCD driver							

Table 1–1: CDC16xxF Family Feature List, continued

This device:								
Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E Mask ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Communication								
DMA	1 DMA channel for serving the graphics bus interface	-	-	1 DMA channel for serving the graphics bus interface	-	-	1 DMA channel for serving the graphics bus interface	-
UART	3: UART0, UART1 and UART2	1: UART0	-	3: UART0, UART1 and UART2	1: UART0	-	3: UART0, UART1 and UART2	-
Synchronous serial peripheral interfaces	2: SPI0 and SPI1	1: SPI0	-	2: SPI0 and SPI1	1: SPI0	-	2: SPI0 and SPI1	-
Full CAN modules V2.0B	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN000F)	1: CAN0 with 256-byte object RAM (LCAN000F)	-	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN0009)	1: CAN0 with 256-byte object RAM (LCAN0009)	-	2: CAN0 and CAN1 with 256-byte object RAM each (LCAN0009)	-
DIGITbus	1 master module	-	-	1 master module	-	-	1 master module	-
Input & Output								
Universal ports selectable as 4:1-mux LCD segment/backplane lines or digital I/O ports	up to 52 I/O or 48 LCD segment lines (=192 segments), in groups of two, configurable as I/O or LCD							
Universal port slew rate	HW-preselectable							
Stepper motor control modules with high current ports	5 modules, 24 dI/dt-controlled ports							
8-bit PWM modules	5 modules: PWM0, PWM1, PWM2, PWM3 and PWM4	3 modules: PWM0, PWM1, PWM2	-	5 modules: PWM0, PWM1, PWM2, PWM3 and PWM4	2 modules: PWM0, PWM1	-	5 modules: PWM0, PWM1, PWM2, PWM3 and PWM4	-
Audio module with auto-decay	✓							
SW-selectable clock outputs	2							
Polling/flash timer output	1 high current port output operable in power-saving operation modes			-				

Table 1–1: CDC16xxF Family Feature List, continued

This device:								
Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E Mask ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Timers & Counters								
16-bit free-running counters with capture/compare modules	CCC0 with 3CAPCOM							
16-bit timers	1: T0							
8-bit timers	2: T1 and T2							
Real time clock, delivering hours, minutes and seconds	✓			-				
Miscellaneous								
Scalable layout in CAN, RAM and ROM	-	✓		-	✓			
Various HW options selectable at random	most options SW-programmable, copy from user program storage during system start-up		mask-programmed according to user specification	most options SW-programmable, copy from user program storage during system start-up		mask-programmed according to user specification		
Core bond-out	✓	-		✓	-			
Supply voltage	4.5 V to 5.5 V							
Temperature range	T _{case} : 0 to +70 °C	T _{case} : −40 to +105 °C		T _{amb} : −40 °C to +85 °C				
Package								
Type	ceramic 177PGA	PMQFP100-1 0.65-mm pitch		ceramic 177PGA	PMQFP100-1 0.65-mm pitch			
Bonded pins	176	100		176	100			

1.2. Abbreviations

ADC	Analog-to-Digital Converter
AM	Audio Module
CAN	Controller Area Network
CAPCOM	Capture/Compare
CCC	Capture/Compare Counter
CPU	Central Processing Unit
DMA	Direct Memory Access
ERM	EMI Reduction Module
IR	Interrupt Controller
LCD	Liquid Crystal Display
P06COMP	P0.6 Alarm Comparator
PINT	Port Interrupt Module
PSM	Power Saving Module
PWM	Pulse Width Modulator
RTC	Real Time Clock
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T	Timer
UART	Universal Asynchronous Receiver/Transmitter

1.3. Block Diagram

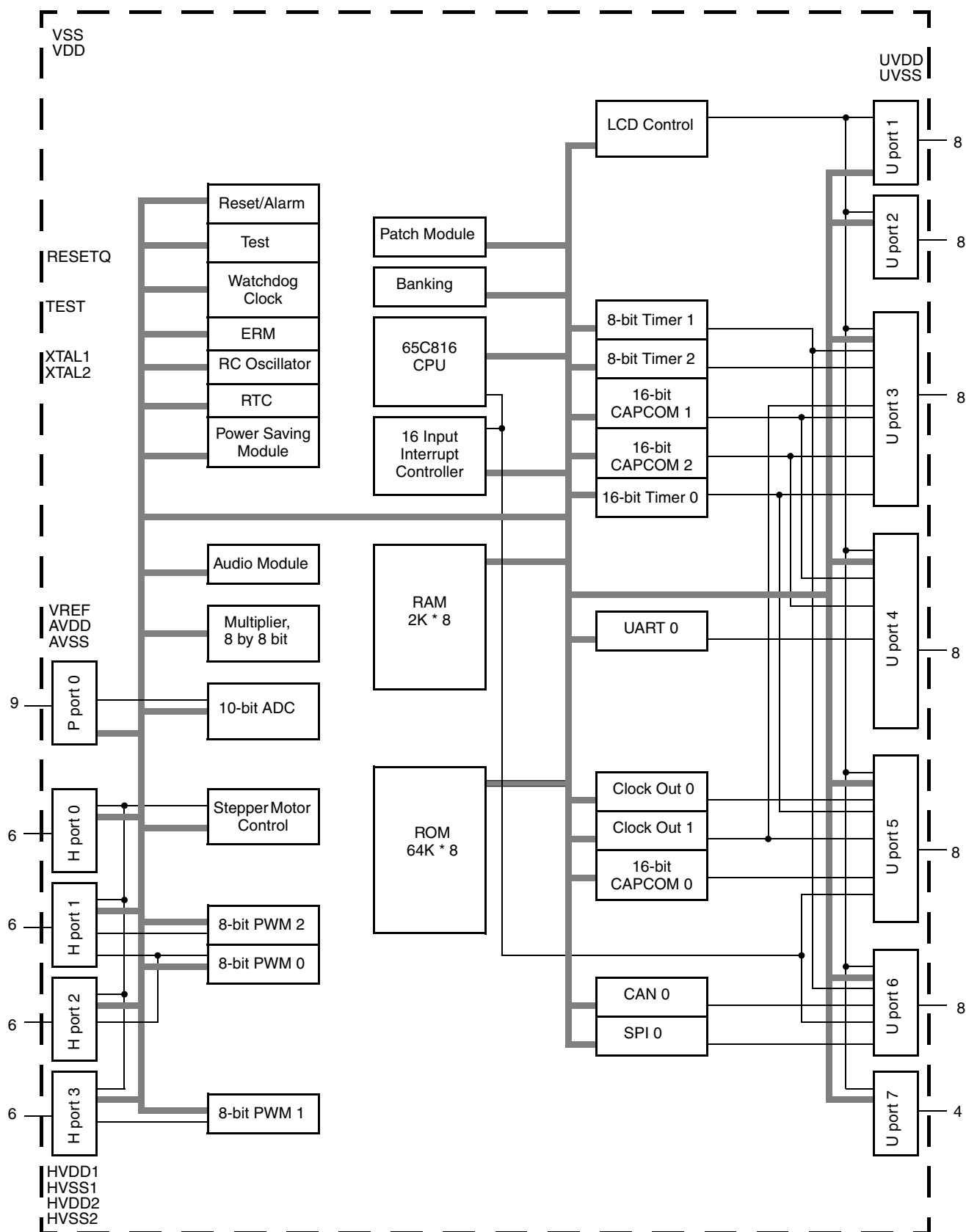


Fig. 1-1: CDC1631F-E block diagram

2. Package and Pins

2.1. Package Outline Dimensions

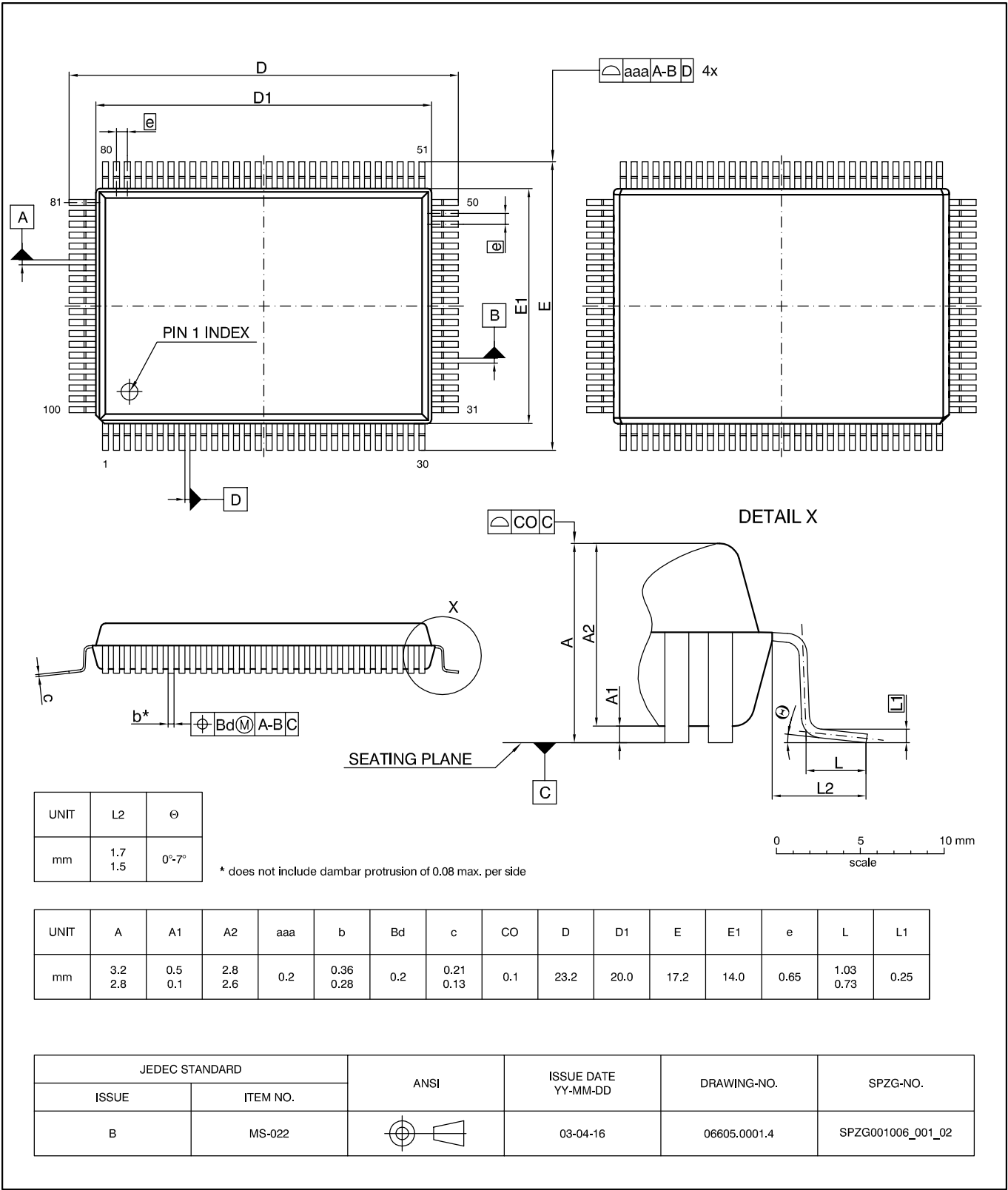


Fig. 2-1:
PMQFP100-1: Plastic Metric Quad Flat Package, 100 leads, 14 × 20 × 2.7 mm³
Ordering code: QB
Weight approximately 1.7 g

2.2. Pin Assignment

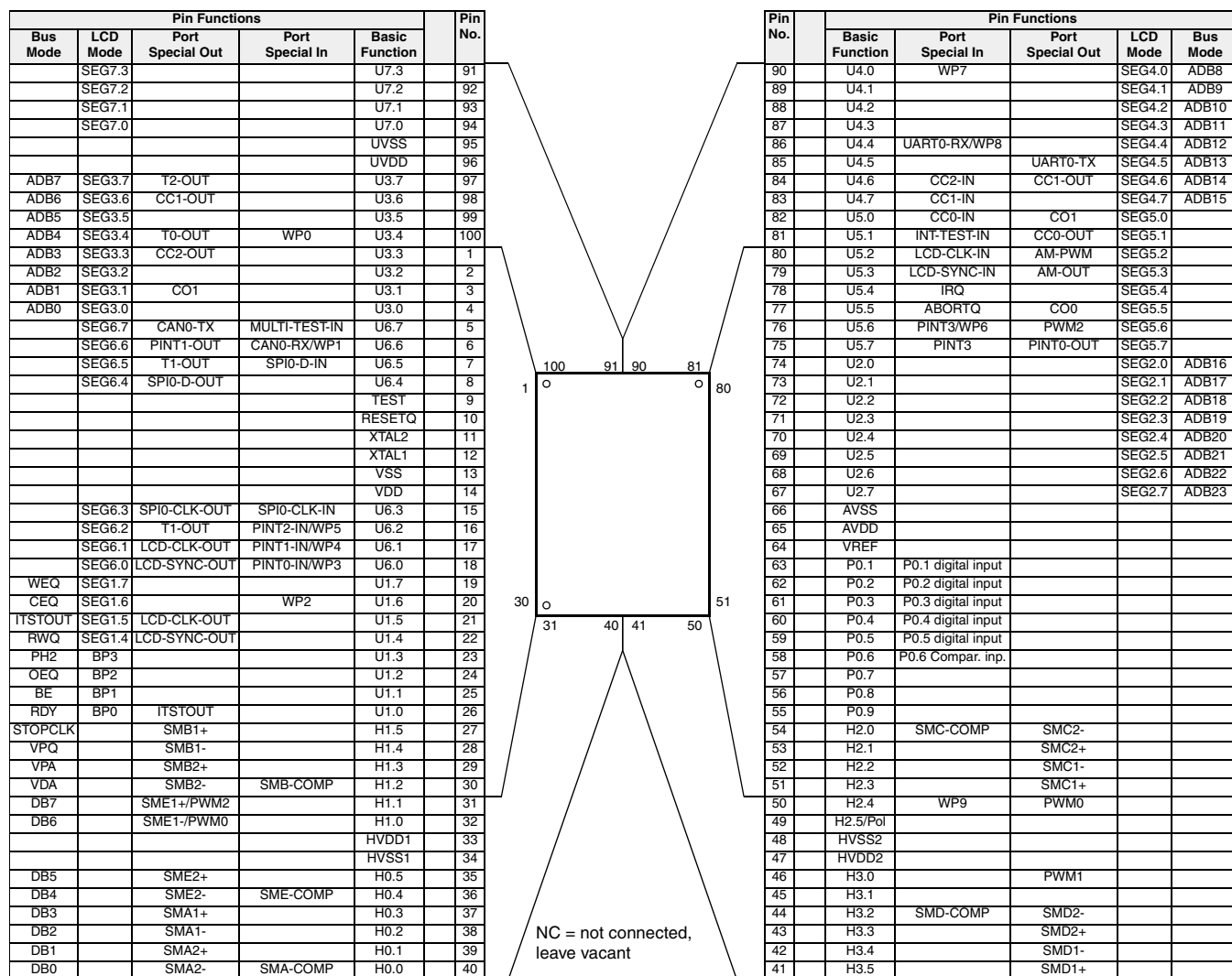


Fig. 2-1: Pin Assignment for PMQFP100-1 Package

2.3. External Components

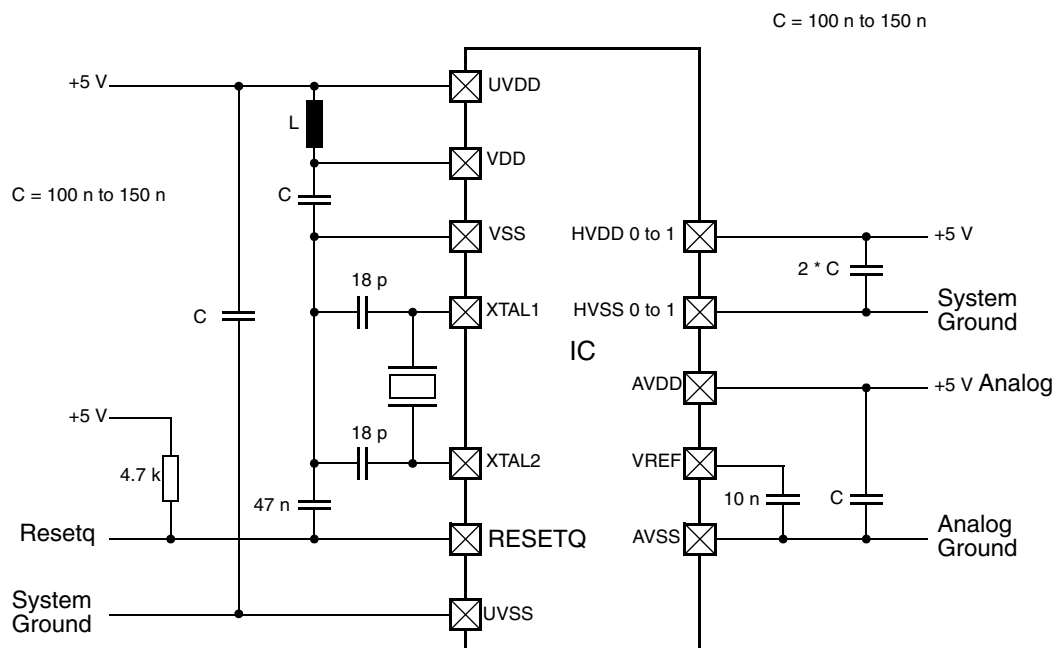


Fig. 2–2: Recommended external supply and quartz connection for low electromagnetic interference (EMI)

To provide effective decoupling and to improve EMC behavior, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. A frequency too low will reduce decoupling effectiveness, increase RF emissions and may affect device operation adversely.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other printed circuit board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a 47 nF capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, to prevent XTAL2 from coupling into RESETQ, and to guarantee a time constant of $\geq 200 \mu\text{s}$, sufficient for proper Wake Reset functionality.

3. Electrical Data

3.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum ratings conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

Table 3–1: All voltages listed are referenced to ground ($UV_{SS} = HV_{SSn} = AV_{SS} = 0V$), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Core supply voltage Port supply voltage Analog supply voltage SM supply voltage 1 SM supply voltage 2	VDD UVDD AVDD HVDD1 HVDD2	–0.3	6.0	V
ΔV_{DD}	Voltage difference between VDD and AVDD, resp. UVDD	VDD, AVDD UVDD	–0.5	0.5	V
I_{SUP}	Core supply current Port supply current	VDD, VSS UVDD, UVSS	–100	100	mA
I_{ASUP}	Analog supply current	AVDD, AVSS	–20	20	mA
I_{HSUP}	SM supply current @ $T_j = 105^\circ\text{C}$, duty factor = 0.71 ¹⁾	HVDD1, HVSS1 HVDD2, HVSS2	–380	380	mA
V_{in}	Input voltage	U ports, XTAL, RESETQ, TEST	$UV_{SS}-0.5$	$UV_{DD}+0.7$	V
		P0 ports VREF	$UV_{SS}-0.5$	$AV_{DD}+0.7$	V
		H ports	$HV_{SS}-0.5$	$HV_{DD}+0.7$	V
I_{in}	Input current	all inputs	0	2	mA
I_o	Output current	U ports	–5	5	mA
		H ports	–60	60	mA
t_{oshsl}	Duration of short circuit in Port SLOW mode to UVSS or UVDD	U ports except U3.2 in DP mode		indefinite	s
T_j	Junction temperature under bias		–45	115	$^\circ\text{C}$
T_s	Storage temperature		–45	125	$^\circ\text{C}$
P_{max}	Maximum power dissipation			0.8	W

¹⁾ This condition represents the worst case load with regard to the intended application

3.2. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Keep $UV_{DD} = AV_{DD}$ during all power-up and power-down sequences.

Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction.

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions” of this specification is not implied, may result in unpredictable behavior of the device and may reduce reliability and lifetime.

Table 3–2: All voltages listed are referenced to ground ($UV_{SS} = HV_{SSn} = AV_{SS} = 0V$), except where noted. All ground pins except VSS must be connected to a low-resistive ground plane close to the IC.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage Port supply voltage Analog supply voltage	VDD UVDD AVDD	4.5	5	5.5	V
HV_{DD}	SM supply voltage 1 SM supply voltage 2	HVDD1 HVDD2	4.75	5	5.25	V
ΔV_{DD}	Voltage difference between VDD and AVDD resp. UVDD	VDD, AVDD UVDD	–0.2		0.2	V
dAV_{DD}	AVDD ripple, peak to peak	AVDD			200	mV
f_{XTAL}	XTAL clock frequency	XTAL1	4		12	MHz
	XTAL clock frequency using ERM	XTAL1	4		10	MHz
T_j	Junction temperature		–40		110	°C
V_{il}	Low input voltage	U ports H ports P0 ports TEST			$0.51 \cdot V_{DD}$	V
V_{ih}	High input voltage	U ports H ports P0 ports TEST	$0.86 \cdot V_{DD}$			V
RV_{il}	Reset active input voltage	RESETQ			0.9	V
WRV_{il}	Reset active input voltage during power-saving modes and Wake Reset	RESETQ			0.6	V
RV_{im}	Reset inactive and Alarm active input voltage	RESETQ	1.6		2.1	V
RV_{ih}	Reset inactive and Alarm inactive input voltage	RESETQ	2.9			V
WRV_{ih}	Reset inactive during power-saving modes	RESETQ	$UV_{DD} - 0.4V$			V
V_{REFi}	ADC reference input voltage	VREF	2.56		AV_{DD}	V
$P0V_i$	P0 ADC input port input voltage	P0 ports	0		V_{REFi}	V

3.3. Characteristics

Listed are only those characteristics that differ from chapter 3.3 of document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD). All not differing characteristics, that are not listed here, apply, but in a T_{CASE} temperature range extended to -40 to $+105$ °C

Table 3–3: $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0$ V, 4.5 V $< V_{DD} = AV_{DD} = UV_{DD} < 5.5$ V, 4.75 V $< HV_{DD1} = HV_{DD2} < 5.25$ V, $T_{CASE} = -40$ °C to $+105$ °C, $f_{XTAL} = 10$ MHz

Symbol	Parameter	Pin Name	Min.	Typ. ¹⁾	Max.	Unit	Test Conditions
Package							
R _{thjc}	Thermal resistance from junction to case			12.1		K/W	measured on Micronas typical 2-layer board, 1s1p, described in document “Integrated Circuits - Thermal Characterization of Packages” (6200-266-1E) (modified JESD-51.3)
R _{thja}	Thermal resistance from junction to ambient			41.0		K/W	
Supply Currents (CMOS levels on all inputs, no loads on outputs, difference between any two VDDs within ±0.2 V)							
I _{DDF}	VDD FAST mode supply current	VDD		16	20	mA	
I _{DDS}	VDD SLOW mode supply current	VDD		1.5	2.0	mA	all modules off ²⁾ ³⁾ , all hardware options set to their reset values
I _{DDD}	VDD DEEP SLOW mode supply current	VDD		0.6	0.9	mA	all modules off ²⁾ ³⁾ , all hardware options set to their reset values
I _{DDI}	VDD IDLE mode supply current	VDD		45	100	μA	f _{xtal} = 4 MHz ³⁾
				120	190	μA	f _{xtal} = 10 MHz ³⁾
				10	30	μA	internal RC oscill.
I _{DDW}	VDD WAKE mode supply current	VDD	0	1	25	μA	
UI _{DDa}	UVDD active supply current	UVDD			0.3	mA	no output activity, LCD module on
AI _{DDa}	AVDD active supply current	AVDD		0.2	0.4	mA	ADC on, ERM off
				1	2	mA	ERM on, f _X TAL = 8.4 MHz
AI _{DDq}	Quiescent supply current	AVDD	0	1	10	μA	ADC and ERM off
UI _{DDq}		UVDD	0	1	10	μA	no output activity, LCD module off
HI _{DDq}		sum of all HVDDn	0	1	20	μA	no output activity, SM module off
¹⁾ Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical recommended operating conditions applied, and are not 100% tested).							

²⁾ Value may be exceeded with unusual hardware option setting

³⁾ Measured with external clock. Add 100 μ A at 4 MHz, 115 μ A at 10 MHz for operation on typical quartz with SR3.XTAL = 0 (Oscillator RUN mode).

3.4. Recommended Crystal Characteristics

See chapter 3.4 of document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

4. CPU, RAM, ROM and Banking

phys.addr.		Alternative log.addr.	Native log.addr.
000000	2K RAM	0000	000000
000800	Reserved		
001900			
001A00			
001B00	CAN0-RAM		
001C00	CAN-Regs		
001D00	Ext. I/O		
001E00	I/O-Reg1		
001F00	I/O-Reg0		
002000		Bank 0	
008000	64 KB ROM	7FFF 8000	Bank 0
010000		FFFF 8000	00FFFF 010000
012000		Bank 2	
		FFFF 8000	Bank 1
		Bank 3	
		FFFF 8000	01FFFF 020000
		Bank 4	
		FFFF 8000	Bank 2
		Bank 5	
		FFFF 8000	02FFFF 030000
		Bank 6	Bank 3
		Bank 15	Bank 7
080000		FFFF 8000	07FFFF 080000
082000	mirrored ROM	Bank 16	Bank 8
		FFFF 8000	
FFFFFF			

Fig. 4–1: Address Map

5. Core Logic

5.1. Control Register CR

The control register CR serves to configure the ways by which certain system resources are accessed during operation. The main purpose is to obtain a variable system configuration during IC test.

Upon each high transition on the RESETQ pin, internal hardware reads data from the address location 00FFF3h and stores it to the CR. The state of the TEST pin at that time specifies which program storage source is accessed for this read:

Table 5–1: Control byte source

TEST	Control byte source
0 or NC	internal ROM (standard for stand-alone operation)
1	external, via multifunction pins in bus mode (for test purposes only)

The system will thus start up according to the configuration defined in address location 00FFF3h, automatically copied to register CR.

CR Control Register							
	7	6	5	4	3	2	1 0
r/w	RESLNG	TSTTOG	x	MFM	TSTROM	IROM	IRAM ICPU
Value of 00FFF3h							
Res							

RESLNG Reset Pulse Length

r/w1: Pulse length is $16/F_{XTAL}$
r/w0: Pulse length is $4096/F_{XTAL}$

This bit specifies the length of the reset pulse which is output at pin RESETQ following an internal reset. If pin TEST is 1 the first reset after power on is short. The following resets are as programmed by RESLNG. If pin TEST is 0, all resets are long.

TSTTOG TEST Pin Toggle (Table 5–2)

This bit is used for test purposes only. If TSTTOG is true in IC active mode, pin TEST can toggle the multifunction pins between bus mode and normal mode.

MFM Multifunction Pin Mode (Table 5–2)

Table 5–2: TSTTOG and MFM usage in ROM parts

TSTTOG	MFM	TEST pin	Multifunction Pins
0	0	x	bus mode
1	0	0	bus mode
		1	normal mode
x	1	x	normal mode

TSTROM TestROM (Table 5–3)

IROM Internal ROM (Table 5–3)

Table 5–3: TSTROM and IROM usage in ROM parts

TSTROM	IROM	selected program storage
1	1	internal ROM
0		internal test ROM
x	0	external via multifunction pins in bus mode

IRAM Internal RAM
r/w1: Enable internal RAM.
r/w0: Disable internal RAM.

ICPU Internal CPU
r/w1: Enable internal CPU.
r/w0: Disable internal CPU.

Table 5–4: Some commonly used settings for address location 00FFF3h. A copy is automatically transferred to the CR when exiting reset.

Code	TEST Pin	Operation Mode
FFh	0	Stand-alone with internal ROM
ABh	1	External program storage connected to multifunction pins in bus mode

6. Interrupt Controller (IR)

Listed are only those registers that differ from document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

6.1. Interrupt Assignment

(cf. chapter 10.3 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

Table 6–1: INT-MUX 1 = HW Option addr. FFC0H

bit 1	bit 0	selects
0	0	CC0 COMP
0	1	Timer 2
1	0	V _{SS}
1	1	Timer 1

Table 6–2: INT-MUX 2 = HW Option addr. FFC0H

bit 3	bit 2	selects
0	0	V _{SS}
0	1	P06 COMP
1	0	SPI 0
1	1	Timer 1

Table 6–3: INT-MUX 3 = HW Option addr. FFC0H

bit 5	bit 4	selects
0	0	PINT3-IN
0	1	V _{SS}
1	0	V _{SS}
1	1	CC1 COMP

Table 6–4: INT-MUX 4 = HW Option addr. FFC0H

bit 7	bit 6	selects
0	0	V _{SS}
0	1	SPI 0
1	0	V _{SS}
1	1	PINT3-IN

Table 6–5: INT-MUX 5 = HW Option addr. FFC1H

bit 1	bit 0	selects
0	0	Timer 2
0	1	V _{SS}
1	0	V _{SS}
1	1	V _{SS}

Table 6–6: INT-MUX 6 = HW Option addr. FFC1H

bit 3	bit 2	selects
0	0	Timer 2
0	1	V _{SS}
1	0	V _{SS}
1	1	PINT2-IN

Table 6–7: INT-MUX 7 = HW Option addr. FFC1H

bit 5	bit 4	selects
0	0	CC0OR
0	1	V _{SS}
1	0	IR-RTC
1	1	IR-WAPI

Table 6–8: INT-MUX 9= HW Option addr. FFC2H

bit 1	bit 0	selects
0	0	V _{SS}
0	1	V _{SS}
1	0	IR-RTC
1	1	IR-WAPI

7. Hardware Options

7.1. Functional Description

Hardware Options are available in several areas to adapt the IC function to the host system requirements:

- clock signal selection for most of the peripheral modules from f_{osc} to $f_{osc}/2^{17}$ plus some internal signals (see “Table 25-2: Clock Option Selection Code” in Chapter “25. Hardware Options” of document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD)).
- interrupt source selection for interrupt inputs 0, 1, 5, 6, 7, 10, 13, 14 and 15
- Special out signal selection for some U and H ports
- Rx/Tx polarity selection for SPI and UART modules
- U Port Slow mode selection

In ROM parts hardware options are not software-programmable.

The data in address locations 00FFA0H through 00FFC3H were used to define their respective, hard-wired hardware options during mask production and can only be altered by changing a production mask for this IC.

For verification purposes, it is recommended to have an application code in ROM that runs with flash parts as well - which is automatically the case if flash parts have been used for software development and tests before. This implies reading of locations 00FFA0h through 00FFC3h directly after reset, to activate the hardware options' settings in flash and EMU parts as well.

7.2. Listing of Dedicated Addresses and Corresponding Hardware Options

Listed are only those registers that differ from document “CDC16xxF-E, Automotive Controller Family User Manual,

CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

Table 7–1: Hardware-Option-Dedicated Addresses

(cf. chapter 25.2 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

00FFA1 PWM0 Clock Options

x	x	x	Clock options f0 to f31 (all)				
---	---	---	-------------------------------	--	--	--	--

00FFA2 PWM0 Trigger Options

x	x	x	Clock options f0 to f31 (all)
The high pulse width of the trigger period must be greater than the high pulse width of the clock the PWM is provided with.			

00FFA3 PWM1 Clock Options

x	x	x	Clock options f0 to f31 (all)				
---	---	---	-------------------------------	--	--	--	--

00FFA4 PWM1 Trigger Options

x	x	x	Clock options f0 to f31 (all)
The high pulse width of the trigger period must be greater than the high pulse width of the clock the PWM is provided with.			

Table 7–1: Hardware-Option-Dedicated Addresses, continued

(cf. chapter 25.2 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

00FFAE SMM, SPI0 Clock Prescaler and SMM Clock Option

x	x0: direct 01: 1/ 1.5 11: 1/ 2.5	Clock options f0 to f31 (all)
---	--	-------------------------------

00FFB4 UART0 Input and Output

UART0 Tx 0: direct 1: inverted	UART0 Rx 0: direct 1: inverted	x	x	x	x	x	x
--------------------------------------	--------------------------------------	---	---	---	---	---	---

00FFC0 Interrupt Sources Multiplexer 1 to 4

<u>Mux4:</u> 00 V _{SS} 01 SPI 0 10 V _{SS} 11 PINT3-IN	<u>Mux3:</u> 00 PINT3-IN 01 V _{SS} 10 V _{SS} 11 CC1 COMP	<u>Mux2:</u> 00 V _{SS} 01 P06 COMP 10 SPI 0 11 Timer 1	<u>Mux1:</u> 00 CC0 COMP 01 Timer 2 10 V _{SS} 11 Timer 1
---	--	---	---

00FFC1 Interrupt Sources Multiplexer 5 to 8

<u>Mux8:</u> 00 CC1OR 01 PINT2-IN 10 IR-RTC 11 IR-WAPI	<u>Mux7:</u> 00 CC0OR 01 V _{SS} 10 IR-RTC 11 IR-WAPI	<u>Mux6:</u> 00 Timer 2 01 V _{SS} 10 V _{SS} 11 PINT2-IN	<u>Mux5:</u> 00 Timer 2 01 V _{SS} 10 V _{SS} 11 V _{SS}
--	---	---	--

00FFC2 Interrupt Sources Multiplexer 9 and Port Multiplexer

H-Port 1.1 0: SME 1: PWM2	x	H-Port 1.0 0: SME 1: PWM0	PINT3-IN 0: at U5.6 1: at U5.7	x	x	<u>Mux9:</u> 00 V _{SS} 01 V _{SS} 10 IR-RTC 11 IR-WAPI
---------------------------------	---	---------------------------------	--------------------------------------	---	---	---

8. Register Cross Reference Table

Table 8–1: CAN RAM, memory page 1B

Address (hex)	Mnemonic	Block
1B00 ... 1BFF	CAN0_RAM	CAN0-RAM

Table 8–2: CAN Registers, memory page 1C

Address (hex)	Mnemonic	Block
1C00	CAN0CTR	CAN0
1C01	CAN0STR	
1C02	CAN0ESTR	
1C03	CAN0IDX	
1C04	CAN0IDM	
1C05		
1C06		
1C07		
1C08	CAN0BT1	
1C09	CAN0BT2	
1C0A	CAN0BT3	
1C0B	CAN0ICR	
1C0C	CAN0OCR	
1C0D	CAN0TEC	
1C0E	CAN0REC	
1C0F	CAN0ESM	
1C10	CAN0CTIM	
1C11		

Table 8–3: I/O Registers, memory page 1E

Address (hex)	Mnemonic	Block
1E64	PAR0	Patch Module
1E65	PAR1	
1E66	PAR2	
1E67	PDR	
1E68	PER0	
1E70	WUS	Power Saving Module
1E71		
1E74	SSR	
1E75		
1E76		
1E78	SSC	
1E79		
1E7A		
1E7C	RTC	
1E7D		
1E7E		
1E80	WPM0	
1E81	WPM2	
1E82	WPM4	
1E83	WPM6	
1E84	WPM8	
1E88	WSC	
1E90	OSC	
1E94	RTCC	
1E98	POL	
1E99		
1E9C	SMX	

Table 8–3: I/O Registers, memory page 1E, continued

Address (hex)	Mnemonic	Block
1EA0	MULCAND	Multiplier
1EA1	MULPLIER	
1EA2	MULPROD	
1EA3		

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1F1F	IRE	Interrupt Controller
1F20	IRC	
1F21	IRRET	
1F22	IRPRI10	
1F23	IRPRI32	
1F24	IRPRI54	
1F25	IRPRI76	
1F26	IRPRI98	
1F27	IRPRIBA	
1F28	IRPRIDC	
1F29	IRPRIFE	
1F2A	IRP	
1F2B	IRPM0	
1F2C	IRPP	
1F2D	AMAS	Audio Module
1F2E	AMF	
1F2F	AMDEC	
1F30	U2D	Universal Port 2
1F32	U2SEG10	
1F33	U2M10	
1F34	U2SEG32	
1F35	U2M32	
1F36	U2SEG54	
1F37	U2M54	
1F38	U2SEG76	
1F39	U2M76	
1F4E	TIM0	Timer 0
1F4F		
1F50	PWM0	PWM
1F51	PWM1	
1F52	PWM2	

Table 8–4: I/O Registers, memory page 1F

Address (hex)	Mnemonic	Block
1F00	CSW0	Core Logic
1F01	CR	
1F02	ERMC	ERM
1F08	SR0	Core Logic
1F09	SR1	
1F0A	SR2	
1F0B	SR3	
1F0C	DBG	Debug Register
1F0F	ABR	Memory Banking
1F10	SPI0D	SPI0
1F11	SPI0M	
1F14	CO0SEL	Core Logic
1F15	CO1SEL	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1F54	TIM1	Timer 1, 2
1F55	TIM2	
1F5A	SMVC	Stepper Motor Module
1F5B	SMVSIN	
1F5C	SMVCOS	
1F5D	SMVCMP	
1F60	CSW1	Core Logic
1F61	CSW2	
1F6C	CC0M	Capture Compare Module
1F6D	CC0I	
1F6E	CC0	
1F6F		
1F70	CC1M	
1F71	CC1I	
1F72	CC1	
1F73		
1F74	CC2M	
1F75	CC2I	
1F76	CC2	
1F77		
1F7C	CCC	
1F7D		
1F7E	P0PIN	Analog Input Port 0
1F80	H0NS	High Current Port 0
1F81	H0TRI	
1F82	H0D	
1F84	H1NS	High Current Port 1
1F85	H1TRI	
1F86	H1D	
1F88	H2NS	High Current Port 2
1F89	H2TRI	
1F8A	H2D	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1F90	H3NS	High Current Port 3
1F91	H3TRI	
1F92	H3D	
1F98	U1D	Universal Port 1
1F99	U1SEG10	
1F9A	U1SEG32	
1F9B	U1M30	
1F9C	U1SEG54	
1F9D	U1M54	
1F9E	U1SEG76	
1F9F	U1M76	
1FA0	UA0D	UART0
1FA1	UA0C	
1FA2	UA0BR0	
1FA3	UA0BR1	
1FA4	UA0IM	
1FA5	UA0CA	
1FA6	UA0IF	
1FA8	AD0	AD Converter
1FA9	AD1	
1FAC	U3D	Universal Port 3
1FAE	U3SEG10	
1FAF	U3M10	
1FB0	U3SEG32	
1FB1	U3M32	
1FB2	U3SEG54	
1FB3	U3M54	
1FB4	U3SEG76	
1FB5	U3M76	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1FB8	U4D	Universal Port 4
1FBA	U4SEG10	
1FBB	U4M10	
1FBC	U4SEG32	
1FBD	U4M32	
1FBE	U4SEG54	
1FBF	U4M54	
1FC0	U4SEG76	
1FC1	U4M76	
1FC4	U5D	Universal Port 5
1FC6	U5SEG10	
1FC7	U5M10	
1FC8	U5SEG32	
1FC9	U5M32	
1FCA	U5SEG54	
1FCB	U5M54	
1FCC	U5SEG76	
1FCD	U5M76	
1FD0	U6D	Universal Port 6
1FD2	U6SEG10	
1FD3	U6M10	
1FD4	U6SEG32	
1FD5	U6M32	
1FD6	U6SEG54	
1FD7	U6M54	
1FD8	U6SEG76	
1FD9	U6M76	
1FDC	U7D	Universal Port 7
1FDE	U7SEG10	
1FDF	U7M10	
1FE0	U7SEG32	
1FE1	U7M32	

Table 8–4: I/O Registers, memory page 1F, continued

Address (hex)	Mnemonic	Block
1FFD	TST3	TST
1FFE	TST1	
1FFF	TST2	

▪

8.1. Modified Registers

Listed are only those registers that differ from document “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD).

8.1.1. Standby Registers

(cf. chapter 6.3 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

SR0		Standby Register 0							
		7	6	5	4	3	2	1	0
r/w		SM	PWM1	PWM0	x	x	CAN0	CCC	SPI0
		0	0	0	x	x	0	0	0
		Res							

SR2		Standby Register 2							
		7	6	5	4	3	2	1	0
r/w		TIM2	x	PWM2	x	x	x	EXTIR	ABM
		0	x	0	x	x	x	0	0
		Res							

SR3		Standby Register 3							
		7	6	5	4	3	2	1	0
r/w		x	x	x	XTAL	WAID	FCLO	x	x
		x	x	x	1	0 ¹⁾	0	x	x
		Res							

¹⁾Reset with pin reset or VDD power on

8.1.2. Memory Patch Module

(cf. chapter 9.2 in “CDC16xxF-E, Automotive Controller Family User Manual, CDC1605F-E Automotive Controller Specification” (6251-606-1PD))

PER0		Patch Enable Register 0								
		7	6	5	4	3	2	1	0	Note
w		x	x	PSEL4	PSEL3	PSEL2	PSEL1	PSEL0	PMEN	
		x	x	0	0	0	0	0	0	Res

9. Differences

This chapter describes differences between this document and predecessor document “CDC1631F-E Automotive Controller”, June 11, 2003, 6251-617-1AI.

No.	Section	Description
1	1. Introduction	Revised introduction
		1.1. Features, Table 1–1: CDC16xxF Family Feature List, page 6: Temperature range, CDC1605F-E EMU: “T _{case} : –40 °C to +105 °C” changed into “T _{case} : 0 to +70 °C”.
2	3. Electrical Data	3.1. Absolute Maximum Ratings: Revised introduction
		3.2. Recommended Operating Conditions: Revised introduction
		3.3. Characteristics: Heading changed and reference added
		Table 3–3: Footnote 1 modified and some values changed (indicated by change bars).
3	4. CPU, RAM, ROM and Banking	Fig. 4–1: Address Map: “MCM PQFP100 Bottom Boot Config.” removed
4	5. Core Logic	5.1. Control Register CR: Description of RESLNG corrected
		Table 5–4: “or Flash” removed
5	6. Interrupt Controller (IR)	New
6	7. Hardware Options	7.1. Functional Description: “- interrupt source selection for interrupt inputs” 0, 1, 10 added
		7.2. Listing of Dedicated Addresses and Corresponding Hardware Options: Added
7	8. Register Cross Reference Table	New
8	9. Differences	New

10. Data Sheet History

1. Advance Information: "CDC1631F-E Automotive Controller", June 11, 2003, 6251-617-1AI. First release of the advance information. Originally created for the HW version CDC1631F-E1.
2. Preliminary Data Sheet: "CDC1631F-E Automotive Controller", Aug. 2, 2004, 6251-617-1PD. First release of the preliminary data sheet. Originally created for the HW version CDC1631F-E3.

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

Printed in Germany
Order No. 6251-617-1PD

All information and data contained in this data sheet are without any commitment, are not to be considered as an offer for conclusion of a contract, nor shall they be construed as to create any liability. Any new issue of this data sheet invalidates previous issues. Product availability and delivery are exclusively subject to our respective order confirmation form; the same applies to orders based on development samples delivered. By this publication, Micronas GmbH does not assume responsibility for patent infringements or other rights of third parties which may result from its use.

Further, Micronas GmbH reserves the right to revise this publication and to make changes to its content, at any time, without obligation to notify any person or entity of such revisions or changes.

No part of this publication may be reproduced, photocopied, stored on a retrieval system, or transmitted without the express written consent of Micronas GmbH.