## **DISCRETE SEMICONDUCTORS**

# DATA SHEET

# **BSD22**MOSFET N-channel depletion switching transistor

Product specification
File under Discrete Semiconductors, SC07

December 1997





# **MOSFET N-channel depletion switching transistor**

BSD22

#### **DESCRIPTION**

Symmetrical insulated-gate silicon MOS field-effect transistor of the n-channel depletion mode type. The transistor is sealed in a SOT143 envelope and features a low ON-resistance and low capacitances. The transistor is protected against excessive input voltages by integrated back-to-back diodes between gate and substrate.

#### Applications:

- analog and/or digital switch
- · switch driver
- convertor
- chopper

#### **PINNING**

1 = substrate (b)

2 = source

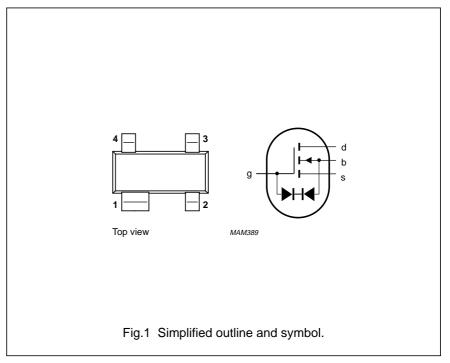
3 = drain

4 = gate

#### Note

 Drain and source are interchangeable

#### Marking code: M32



#### **QUICK REFERENCE DATA**

Drain-source voltage	$V_{DS}$	max.	20	V	
Cata aguras voltage	V	may	+ 15	V	
Gate-source voltage	$V_{GS}$	max.	<b>- 40</b>	V	
Drain current (DC)	I <sub>D</sub>	max.	50	mA	
Total power dissipation up to T <sub>amb</sub> = 25 °C	$P_{tot}$	max.	230	mW	
Junction temperature	$T_j$	max.	125	°C	
Drain-source ON-resistance					
$V_{GS} = 10 \text{ V}; V_{SB} = 0; I_D = 1 \text{ mA}$	$R_{DSon}$	max.	30	Ω	
Feed-back capacitance					
$V_{GS} = V_{BS} = -5 \text{ V}; V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}$	$C_{rss}$	typ.	0.6	pF	

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RATINGS				
Limiting values in accordance with the Absolute Maxir	mum System (IEC	134)		
Drain-source voltage	$V_{DS}$	max.	20	V
Source-drain voltage	$V_{SD}$	max.	20	V
Drain-substrate voltage	$V_{DB}$	max.	25	V
Source-substrate voltage	$V_{SB}$	max.	25	V
Gate-substrate voltage	$V_{GB}$	max.	± 15	V
Gate-source voltage	$V_{GS}$	max.	+ 15 - 40	V V
Drain current (DC)	$I_{D}$	max.	50	mA
Total power dissipation up to $T_{amb} = 25  {}^{\circ}C^{(1)}$	$P_{tot}$	max.	230	mW
Storage temperature range	$T_{stg}$	-65	to + 150	°C
Junction temperature	$T_j$	max.	125	°C

#### THERMAL RESISTANCE

From junction to ambient in free air<sup>(1)</sup>  $R_{th j-a} = 430$  K/W

#### Note

1. Device mounted on a ceramic subtrate of 8 mm  $\times$  10 mm  $\times$  0.7 mm.

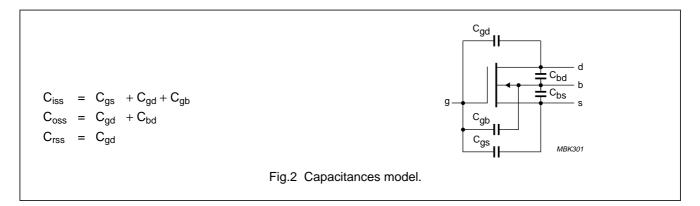
#### CHARACTERISTICS

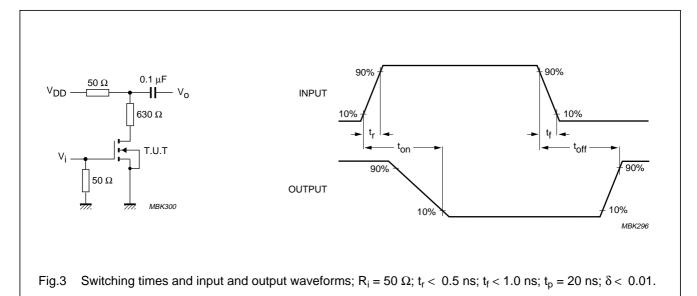
T <sub>amb</sub> = 25 °C unless otherwise specified				
Drain-source breakdown voltage				
$V_{GS} = V_{BS} = -5 \text{ V}; I_S = 10 \text{ nA}$	$V_{(BR)DSX}$	min.	20	V
Source-drain breakdown voltage				
$V_{GD} = V_{BD} = -5 \text{ V}; I_D = 10 \text{ nA}$	$V_{(BR)SDX}$	min.	20	V
Drain-substrate breakdown voltage				
$V_{GB} = 0$ ; $I_D = 10$ nA; open source	$V_{(BR)DBO}$	min.	25	V
Source-substrate breakdown voltage				
$V_{GB} = 0$ ; $I_S = 10$ nA; open drain	$V_{(BR)SBO}$	min.	25	V
Drain-source leakage current				
$V_{GS} = V_{BS} = -5 \text{ V}; V_{DS} = 10 \text{ V}$	I <sub>DSoff</sub>	typ.	1.0	nA
Source-drain leakage current				
$V_{GD} = V_{BD} = 5 \text{ V}; V_{SD} = 10 \text{ V}$	I <sub>SDoff</sub>	typ.	1.0	nA
Gate-substrate leakage current				
$V_{DB} = V_{SB} = 0$ ; $V_{GB} = \pm 15 \text{ V}$	$I_{GBS}$	max.	10	nA
Forward transconductance at f = 1 kHz				
$V_{DS} = 10 \text{ V}; V_{SB} = 0; I_D = 20 \text{ mA}$	<b>a</b>	min.	10	mS
	9 <sub>fs</sub>	typ.	15	mS
Gate-source cut-off voltage				
$V_{DS} = 10 \text{ V}; V_{SB} = 0;$				
$I_D = 10 \mu A$	$-V_{(P)GS}$	max.	2.0	V

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Drain-source ON-resistance				
$I_D = 1 \text{ mA}; V_{SB} = 0;$		f	05	0
$V_{GS} = 5 V$	$R_{DSon}$	typ. max.	25 50	$\Omega$
V <sub>GS</sub> = 10 V	$R_{DSon}$	typ. max.	15 30	$\Omega$
Capacitances at f = 1 MHz				
$V_{GS} = V_{BS} = -5 \text{ V}; V_{DS} = 10 \text{ V}$				
Feed-back capacitance	$C_{rss}$	typ.	0.6	pF
Input capacitance	$C_iss$	typ.	1.5	pF
Output capacitance	$C_{oss}$	typ.	1.0	pF
Switching times (see Fig.3)				
$V_{DD} = 10 \text{ V}; V_i = -5 \text{ V to} + 5 \text{ V}$	t <sub>on</sub>	typ.	1.0	ns
	$t_{off}$	typ.	5.0	ns





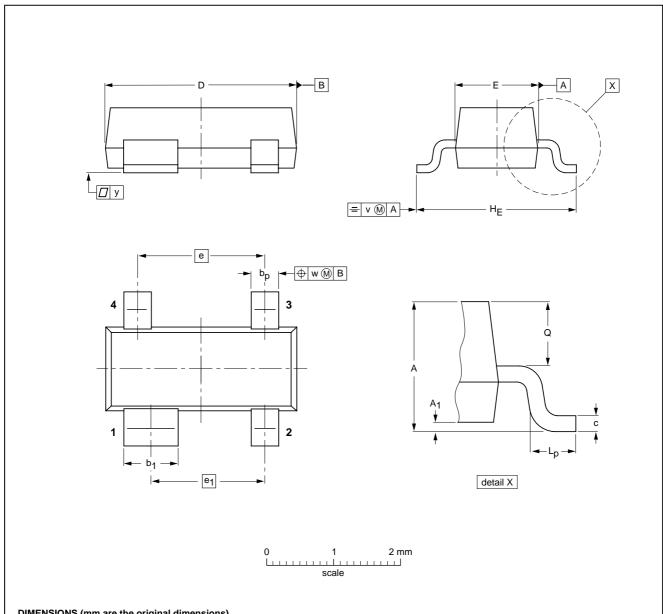
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#### **PACKAGE OUTLINE**

#### Plastic surface mounted package; 4 leads

SOT143B



#### **DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	bp	b <sub>1</sub>	С	D	E	е	e <sub>1</sub>	HE	L <sub>p</sub>	Q	v	w	у
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE		REFER	ENCES	EUROPEAN ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT143B					97-02-28	

Product specification Philips Semiconductors

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#### **DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	

#### Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

#### **Application information**

Where application information is given, it is advisory and does not form part of the specification.

#### LIFE SUPPORT APPLICATIONS

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