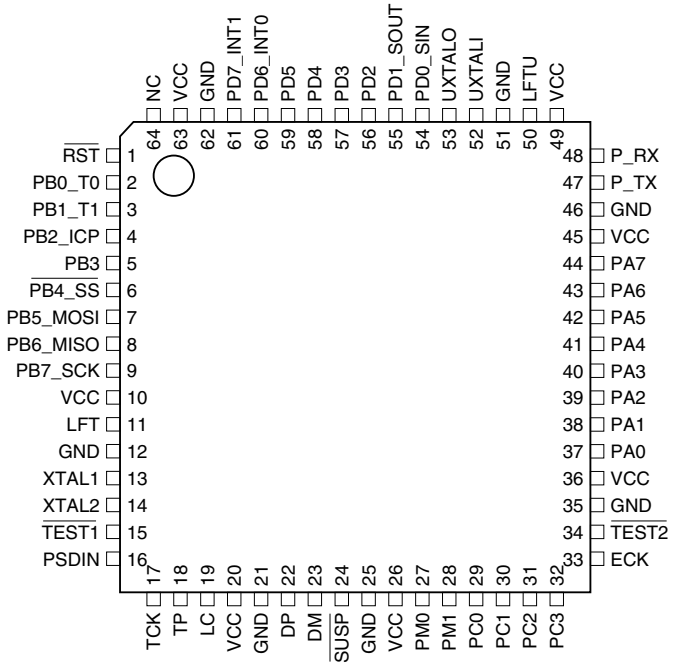
Features

- **AVR® Microcontroller**
- **Clock Generator Provides CPU Rates up to 24 MHz**
- **Programmable UART with 16-byte FIFOs at the Receiver Side (1), with a Maximum Rate of 921K Baud**
- **Programmable SPI Interface**
- **Full-speed USB Function Controller**
- **On-chip 2K Bytes SRAM (for Data)**
- **On-chip 2K Bytes Dual-port RAM for Segmentation and Reassembly of Packets Exchanged between the USB and the UART Interfaces**
- **8K x 16-bit In-system SRAM for Program Code**
- **On-chip Bootstrap ROM for Program Uploading to the Internal Program SRAM, Either from the USB or the SPI**
- **One USB Control Endpoint**
- **Five USB Programmable Endpoints (up to 64 Bytes) with Double-buffered FIFOs for Back-to-back Transfers**
- **One 8-bit Timer/Counter**
- **One 16-bit Timer/Counter**
- **External and Internal Interrupt Sources**
- **Programmable Watchdog Timer**
- **Independent UART BRG Oscillator**
- **64-pin TQFP Package**
- **3.3V Operation**

Figure 1. Pin Configuration



AVR®-based Bridge between Full-speed USB and Fast Serial Asynchronous Interfaces

AT76C711

Rev. 1643AS–10/00

Note: This is a summary document. A complete document is available on our web site at *www.atmel.com*.

Description

The Atmel AT76C711 is a compound USB device designed to provide a high-speed USB interface to devices that need to communicate with a base station through fast serial links, like UARTs and IrDA interfaces. It is based on the AVR-enhanced RISC architecture and consists of a USB function interface with a devoted DMA controller for fast transfers of data between the endpoint FIFOs and the DPRAM, a 2 KB internal RAM, a Synchronous Peripheral Interface (SPI), a UART, supporting a maximum rate of 921K baud, an 8K x 16-bit in-system SRAM for microcode storage, which is loaded from the SPI controller, 2K bytes dual-port RAM (DPRAM) and a programmable DMA controller for packet transfers between the UART and the DPRAM, without microcontroller intervention. An IrDA controller is also provided, attached to a second UART module and is able to communicate with an IrDA transceiver with a maximum rate of 1.2 Mbps. A hardwired Device Firmware Upgrade (DFU) protocol handler is implemented for programming an external AT45BDxxx serial Flash during the production phase. An internal bootstrap ROM contains the executable program for uploading the application code from an external serial Flash to the on-chip program SRAM. Alternatively, microcode can be stored in the program SRAM using the slave program mode while the chip is in the reset state. The USB and peripheral device controller function should be implemented in the microcontroller's firmware.

The device is suitable for applications where minimization of power dissipation is required, since there are no power-consumable transactions with external parallel devices.

The USB H/W block consists of a USB transceiver, the SIE, endpoint controllers and an interface to the microcontroller. The USB H/W interfaces to the USB host at the packet level. The microcontroller firmware handles the higher-level USB protocol layers that are not processed by the USB H/W and in addition, it performs the peripheral control functions.

A typical application of AT76C711 and its functional diagram are shown in Figures 2 and 3.

Applications

AT76C711 can be used in applications where peripherals supporting fast serial asynchronous or synchronous transfer of data have to communicate with a host or other peripherals through a high-speed serial link, like USB.

Typical areas of AT76C711 usage are:

- Connection of Network Interface Cards (NICs) to a host system
- Wireless communications
- Bridging of microcontrollers with different types of serial interfaces
- USB to UART bridge
- USB to IrDA bridge
- IrDA to UART bridge
- Packet adaptation of network protocol packets to USB requirements

Block Diagram

Figure 1. Block Diagram

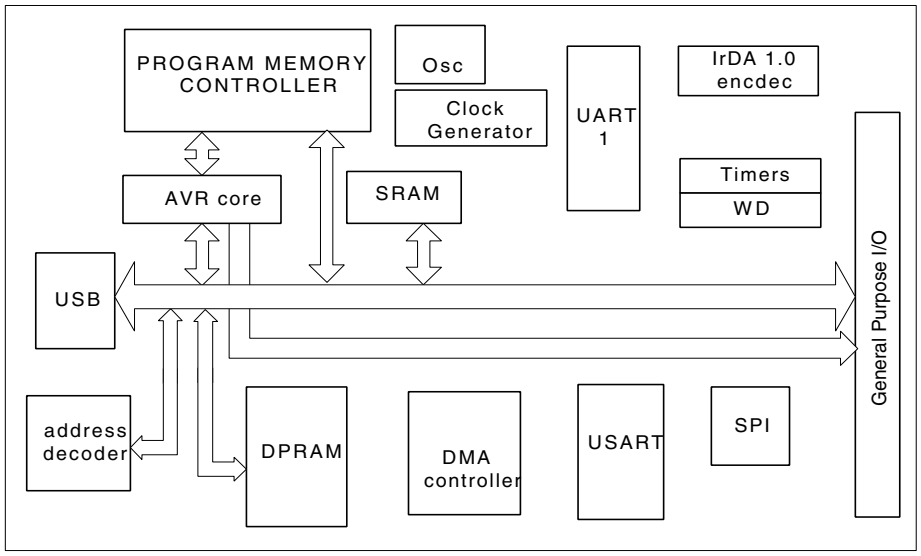


Figure 2. Typical AT76C711 Application

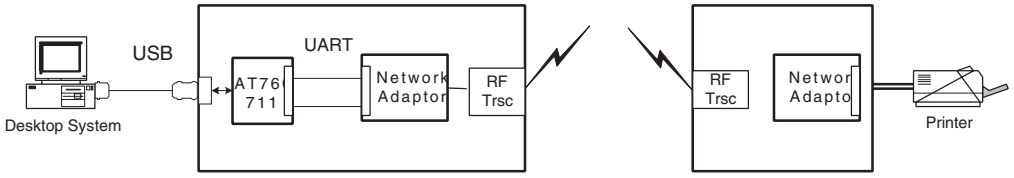
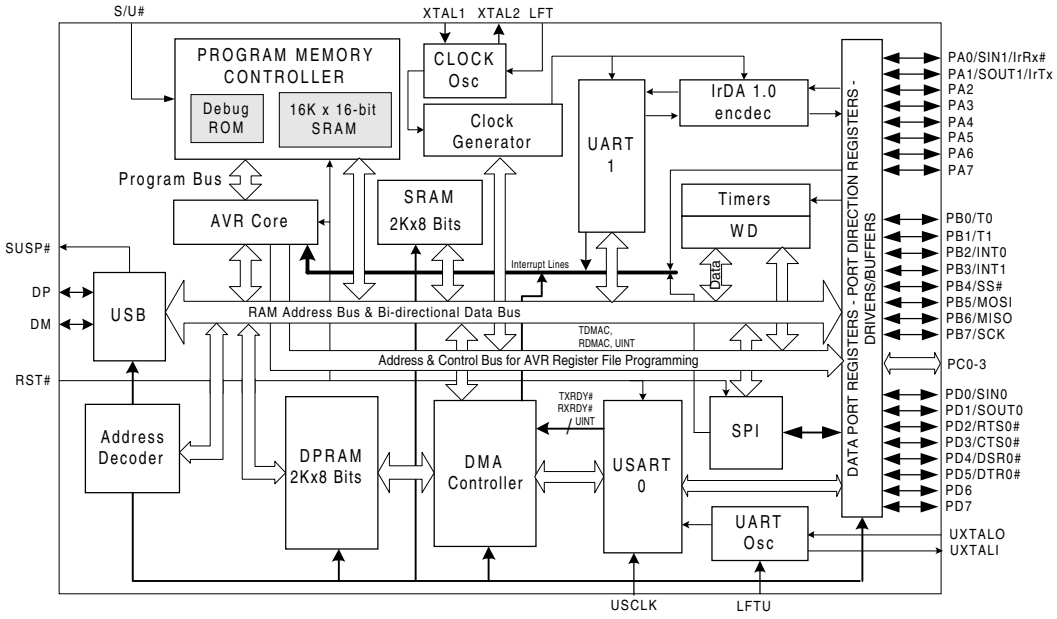


Figure 3. Functional Diagram



Pin Summary

Pin Assignment

Type: I = Input O = Output
OD = Output, open drain B = Bi-directional
V = Power supply, ground

Table 1. Pin Assignment in Alphabetical Order

Pin #	Signal	Type
23	DM	B
22	DP	B
33	ECK	I
19	LC	I
14	LFT	I
50	LFTU	I
*	GND	V
64	NC	
48	P_IRX	I
47	P_ITX	O
37	PA0	B
38	PA1	B
39	PA2	B
40	PA3	B
41	PA4	B
42	PA5	B
43	PA6	B

Pin #	Signal	Type
44	PA7	B
2	PB0_T0	B
3	PB1_T1	B
4	PB2_ICP	B
5	PB3	B
6	$\overline{\text{PB4\_SS}}$	B
7	PB5_MOSI	B
8	PB6_MISO	B
9	PB7_SCK	B
29	PC0	B
30	PC1	B
31	PC2	B
32	PC3	B
54	PD0_SIN	B
55	PD1_SOUT	B
56	PD2	B
57	PD3	B

Pin #	Signal	Type
58	PD4	B
59	PD5	B
60	PD6_INT0	B
61	PD7_INT1	B
16	PSDIN	I
1	$\overline{\text{RST}}$	I
27, 28	PM0, PM1	I
24	$\overline{\text{SUSP}}$	O
17	TCK	I
15	$\overline{\text{TEST1}}$	I
34	$\overline{\text{TEST2}}$	I
18	TP	I
**	VCC	V
51	UXTALI	I
52	UXTALO	O
11	XTAL1	I
12	XTAL2	O

Notes: 1. (*) GND: 12, 21, 25, 35, 46, 51, 62
2. (*) VCC: 10, 20, 24, 36, 45, 49, 63

Table 2. Pin Assignment in Numerical Order

Pin #	Signal	Type
1	$\overline{\text{RST}}$	I
2	PB0_T0	B
3	PB1_T1	B
4	PB2_ICP	B
5	PB3	B
6	$\overline{\text{PB4\_SS}}$	B
7	PB5_MOSI	B
8	PB6_MISO	B
9	PB7_SCK	B
10	VCC	V
11	LFT	I
12	GND	V
13	XTAL1	I
14	XTAL2	O
15	$\overline{\text{TEST1}}$	I
16	PSDIN	I
17	TCK	I
18	TP	I
19	LC	I
20	VCC	V
21	GND	V
22	DP	B

Pin #	Signal	Type
23	DM	B
24	$\overline{\text{SUSP}}$	O
25	GND	V
26	VCC	V
27	PM0	I
28	PM1	I
29	PC0	B
30	PC1	B
31	PC2	B
32	PC3	B
33	ECK	I
34	$\overline{\text{TEST2}}$	I
35	GND	V
36	VCC	V
37	PA0	B
38	PA1	B
39	PA2	B
40	PA3	B
41	PA4	B
42	PA5	B
43	PA6	B
44	PA7	B

Pin #	Signal	Type
45	VCC	V
46	GND	V
47	P_ITX	O
48	P_IRX	I
49	VCC	V
50	LFTU	I
51	GND	V
52	UXTALI	I
53	UXTALO	O
54	PD0_SIN	B
55	PD1_SOUT	B
56	PD2	B
57	PD3	B
58	PD4	B
59	PD5	B
60	PD6_INT0	B
61	PD7_INT1	B
62	GND	V
63	VCC	V
64	NC	V

Signal Description

Table 3. Signal Description

Name	Type	Description
Program Memory Controller Signals		
PM0, PM1	I	See Figure 4.
PSDIN	I	Program Serial Data In: In slave program mode, this signal carries the serial program data that are samples with the positive edge of TCK.
TP	I	When $\overline{RST}$ is active (low), a high level of this signal, for at least two TCK pulses, forces the program address generator.
LC	I	Load Complete: A transition from low to high denotes the completion of program data transfer from the external device. The AVR will start executing instructions from the internal SRAM as soon as the $\overline{RST}$ goes high.
TCK	I	A clock signal for sampling PSDIN input.
Port Signals		
PA[0:7]	B	Port A, PB0 through PB7. 8-bit bi-directional port.
PA[0:7]	B	Port B, PB0 through PB7. 8-bit bi-directional port. PB0, PB1, PB2, PB4 through PB7 are dual functions as shown below: **Port** **Alternate Function** PB0 Timer/Counter0 clock input PB1 Timer/Counter1 clock input PB2 (ICP) Input Capture Pin for Timer/Counter1 PB4 (SS#) SPI slave port select input PB5 (MOSI) SPI slave port select input PB6 (MISO) SPI master data in, slave data out PB7 (SCK) SPI master clock out, slave clock in
PC[0:3]	B	Port C, PC0 through PC3. 4-bit output port.
PD[0:7]	B	Port D, PD0 through PD7. 8-bit bi-directional I/O port. PD0, PD1 also serve as the data lines for the asynchronous serial port as listed below: **Port** **Alternate Function** PD0 (SIN) Serial Data In (I): This pin provides the serial receive data input to 16550 UART. The SIN signal will be a logic “1” during reset, idle (no data). During the local loopback mode, the SIN input pin is disabled and SOUT data is internally connected to the UART SIN input. PD1 (SOUT) Serial Data Out (O): This pin provides the serial transmit data from the 16550 UART. The SOUT signal will be a logic “1” during reset, idle (no data). PD6 (INT0) External Interrupt0 source PD7 (INT1) External Interrupt1 source
USB Serial Interface		
DP	B	Upstream Plus USB I/O. DP and DM form the differential signal pin pair connected to the host controller or an upstream hub.
DM	B	Upstream Minus USB I/O
$\overline{SUSP}$	O	Suspend. This output pin is deactivated (high) during normal operation. It is used to signal the host microcontroller that AT76C711 has received USB suspend signaling. This pin will stay asserted while AT76C722 is in the suspend mode. This pin is deactivated whenever a USB resume signaling is detected on DP and DM.

Table 3. Signal Description (Continued)

Name	Type	Description
Test Signals		
$\overline{\text{TEST1}}$	I	Test signal for clocks (used in production phase only – normally tied to high)
$\overline{\text{TEST2}}$	I	Test signal for monitoring internal signal levels using the four data ports (used in production phase only – normally tied to high)
ECK	I	Clock pulse for activating various test modes when $\overline{\text{TEST2}}$ is active
IrDA Interface		
P_ITX	O	Infrared Data Out: This pin provides the serial transmit data from the IrDA codec to external IR Data Transceiver. This function is activated when the IrDA interface is enabled from PERIPHEN I/O Register.
P_IRX	I	Infrared Data In: This pin provides the serial receive data input from the external IR Data Transceiver to IrDA codec. This function is activated when the IrDA interface is enabled from PERIPHEN I/O Register.
Other Signals		
GND	V	Ground
VCC	V	3.3V power supply
$\overline{\text{RST}}$	I	Reset. A low on this pin for two machine cycles, while the oscillator is running, resets the device.
XTAL1	I	Oscillator Input. Input to the inverting oscillating amplifier. A 12 MHz clock oscillator should be applied.
XTAL2	O	Oscillator Output. Output of the inverting oscillator amplifier.
LFT	I	Master clock PLL LFT pin
UXTALI	I	UART BRG Oscillator Input. Input to the UART oscillator amplifier.
UXTALO	O	UART BRG Oscillator Output. Output of the UART oscillator amplifier.
LFTU	I	UART clock PLL LFT pin

Note: Any signal with a # indicates that it is an active low signal.

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-803-000
FAX (44) 1355-242-743

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

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