50 MHz to 2200 MHz Quadrature Modulator

Preliminary Technical Data

ADL5385

FEATURES

Output frequency range: 50 MHz to 2200 MHz
Modulation bandwidth: dc to 700 MHz
1 dB output compression: +9 dBm @ 350 MHz
Noise floor: –158 dBm/Hz
Sideband Suppression: -40 dBc @ 350 MHz
Single supply: 4.75 V to 5.5 V
24-lead exposed-paddle LFCSP package

APPLICATIONS

Radiolink Infrastructure
Cable Modem Termination Systems
Wireless Infrastructure Systems
Wireless LAN/wireless local loop
LMDS/broadband wireless access systems

FUNCTIONAL BLOCK DIAGRAM

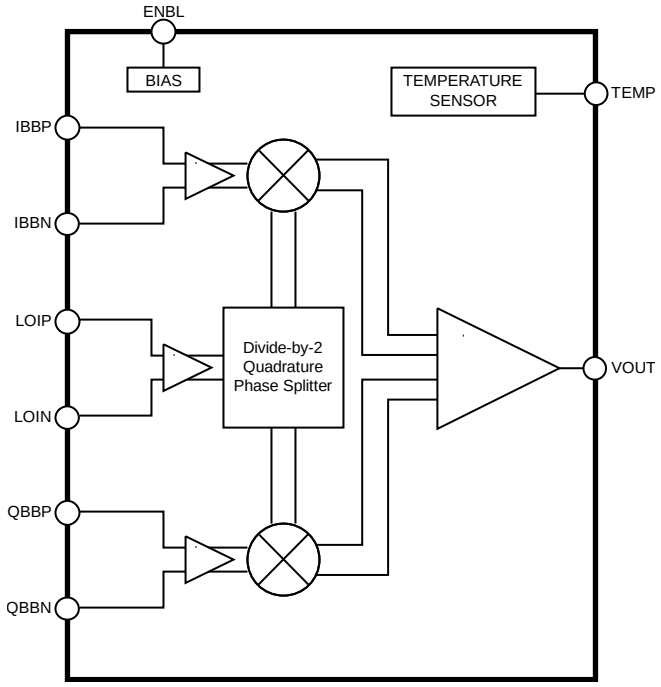

Figure 1 Block Diagram

PRODUCT DESCRIPTION

The ADL5385 is a silicon, monolithic, quadrature modulator that is designed for use from 50 MHz to 2200 MHz. Its excellent phase accuracy and amplitude balance enable high performance IF or direct RF modulation for communication systems.

The single-ended two-times-LO input signal is buffered, and then split into in-phase and quadrature signals at one-times-LO. These two LO signals are further buffered and then mixed with the corresponding I channel and Q channel baseband signals in two Gilbert cell mixers. The mixers' outputs are then summed together in the output amplifier. The output amplifier is designed to drive 50 Ω loads.

The ADL5385 can be used as a IF or direct-to-RF modulator in digital communication systems. The wide baseband input bandwidth allows for baseband drive or drive from a complex IF. Typical applications are in Radiolink Transmitters, Cable Modem Termination systems and Broadband Wireless Access Systems.

The ADL5385 is fabricated using Analog Devices' advanced Silicon Germanium bipolar process and is available in a 24-Lead Pb-free LFCSP with exposed paddle. Performance is specified over a –40°C to +85°C temperature range. A Pb-free evaluation board is available.

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SPECIFICATIONS

Table 1. V_S = 5 V; Ambient Temperature = 25°C; LO = -7 dBm; I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias; baseband frequency = 1 MHz; LO source and RF output load impedances are 50 Ω, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
Output Frequency Range		50		2200	MHz
External LO Frequency Range	External LO frequency is twice output frequency	100		4400	MHz
Output Frequency = 50 MHz					
Output Power	Single (lower) Sideband Output		6		dBm
Output P1 dB			10		dBm
Carrier Feedthrough	unadjusted (nominal drive level)		-50		dBm
Sideband Suppression	unadjusted (nominal drive level)		-50		dBc
Second Baseband Harmonic	(F_{LO} - (2 × F_{BB}))		-50		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB}))		-50		dBc
Output IP3	F1= 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = -5 dBm per tone		24		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-158		dBm/Hz
	20 MHz offset from LO, Output Power = -5 dBm		-158		dBm/Hz
Output Return Loss			10		dB
Output Frequency = 140 MHz					
Output Power	Single (lower) Sideband Output		6		dBm
Output P1 dB			10		dBm
Carrier Feedthrough	unadjusted (nominal drive level)		-46		dBm
Sideband Suppression	unadjusted (nominal drive level)		-50		dBc
Second Baseband Harmonic	(F_{LO} - (2 × F_{BB}))		-50		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB}))		-50		dBc
Output IP3	F1= 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = -5 dBm per tone		24		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-158		dBm/Hz
	20 MHz offset from LO, Output Power = -5 dBm		-158		dBm/Hz
Output Return Loss			10		dB
Output Frequency = 350 MHz					
Output Power	Single (lower) Sideband Output		6		dBm
Output P1 dB			10		dBm
Carrier Feedthrough	unadjusted (nominal drive level)		-41		dBm
Sideband Suppression	unadjusted (nominal drive level)		-40		dBc
Second Baseband Harmonic	(F_{LO} - (2 × F_{BB}))		-50		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB}))		-50		dBc
Output IP3	F1= 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = -5 dBm per tone		24		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-158		dBm/Hz
	20 MHz offset from LO, Output Power = -5 dBm		-158		dBm/Hz
Output Return Loss			10		dB
Output Frequency = 860 MHz					
Output Power	Single (lower) Sideband Output		4.5		dBm
Output P1 dB			9		dBm
Carrier Feedthrough	unadjusted (nominal drive level)		-37		dBm
Sideband Suppression	unadjusted (nominal drive level)		-35		dBc
Second Baseband Harmonic	(F_{LO} - (2 × F_{BB}))		-50		dBc
Third Baseband Harmonic	(F_{LO} + (3 × F_{BB}))		-50		dBc
Output IP3	F1= 3.5 MHz, F2 = 4.5 MHz, P_{OUT} = -5 dBm per tone		24		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-158		dBm/Hz
	20 MHz offset from LO, Output Power = -5 dBm		-158		dBm/Hz
Output Return Loss			10		dB

Parameter	Conditions	Min	Typ	Max	Unit
LO INPUTS	Pins LOIP and LOIN				
LO Drive Level	Characterization performed at typical level		–7		dBm
Input Impedance			50		Ω
Input Return Loss	350 MHz		-10		dB
BASEBAND INPUTS	Pins IBBP, IBBN, QBBP, QBBN				
I and Q Input Bias Level			500		mV
Bandwidth (3 dB)			700		MHz
TEMPERATURE OUTPUT	TEMP				
Output Voltage	T_A = 27.15°C, 300K, R_L = 1 MΩ		1.5		V
Temperature Slope	–40°C ≤ T_A ≤ +85°C, R_L = 1 MΩ		4.7		mV/°C
POWER SUPPLIES	Pins VPS1 and VPS2				
Voltage		4.75		5.5	V
Supply Current			210		mA

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

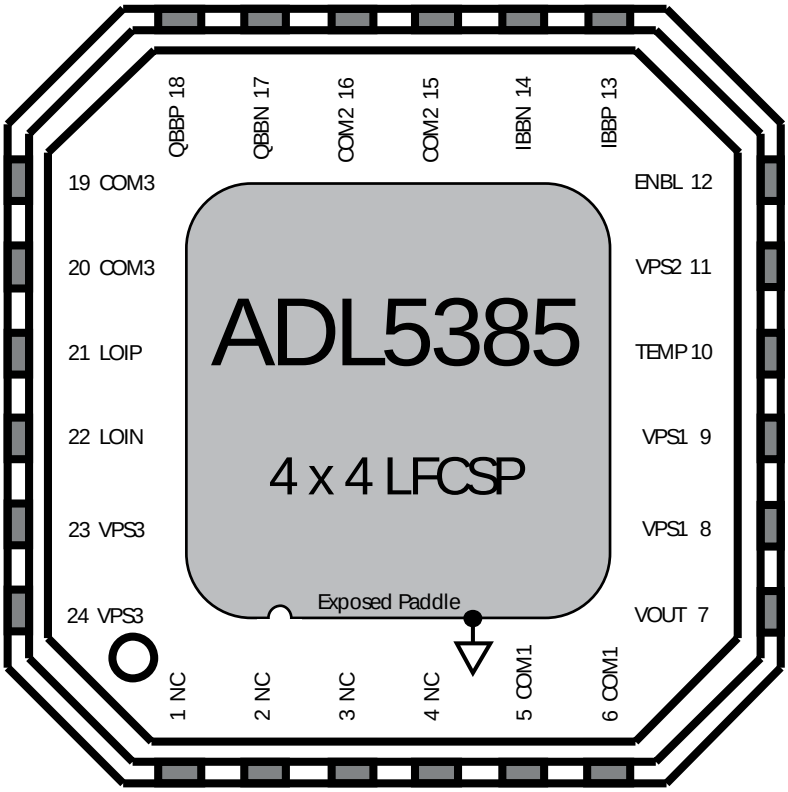

Figure 2 ADL5385 Pinout

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description	Equivalent Circuit
1,2,3,4	NC	No Connection. These pins can be left open or tied to ground.	
5,6,15,16, 19,20	COM1, COM2, COM3	Common Pins. COM1, COM2, and COM3 should all be connected to a ground plane via a low impedance path.	
7	VOUT	Device Output. Single-ended, 50 Ω internally biased RF/IF output. Pin must be ac-coupled to the load.	
8,9,11,23,24	VPS1, VPS2, VPS3	Power Supply Pins. Decouple each pin with a 0.1uF capacitor. Pins 8 and 9 can share a single capacitor as can pins 23 and 24	
10	TEMP	Temperature Sensor Output	
12	ENBL	Chip Enable. Set to 0V to enter sleep mode. Set to supply voltage to activate device.	
13,14,17,18	IBBP, IBBN, QBBN, QBBP	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs should be dc-biased to approximately 500 mV dc, and should be driven from a low impedance source. Nominal characterized ac signal swing is 700 mV p-p on each pin (150 mV to 850 mV). This results in a differential drive of 1.4 V p-p with a 500 mV dc bias. These inputs are not self-biased and must be externally biased.	
21	LOIP	Single-Ended two-times Local Oscillator Input. Internally dc-biased . LOIP should be ac-coupled.	
22	LOIN	Common for LO Input. AC couple through a low impdeance path to ground.	

BASIC CONNECTIONS

Refer to the evaluation board schematic for the basic connections for operating the AD5385 (Figure 2). A single power supply of between 4.75 V and 5.5 V is applied to pins VPS1 and VPS2 and VPS3. All VPS pins must be connected to the same potential. Each pin should be decoupled with a 0.1 uF capacitor. These capacitors should be located as close as possible to the device. Pins 8 and 9 can share a single capacitor as can pins 23 and 24. The voltage applied to Pin 12 (ENBL) determines whether the part is in a sleep mode or active mode. When this pin is grounded the internal biasing circuitry is disabled and the part draws minimal supply current. When this pin is tied to the supply voltage, the bias circuitry is activated and the part is in active mode. Pins COM1, COM2, and COM3 should all be tied to the same ground plane through low impedance paths. The exposed paddle on the under side of the package should be soldered to a low impedance ground plane. If multiple ground planes exist on the circuit board, these should be stitched together with multiple vias to enhance thermal and electrical performance.

The baseband inputs QBBP, QBBN, IBBP and IBBN must be driven from a differential source. The nominal drive level of 1.4 Vpp differential (700 mVpp on each pin) should be biased at 500 mV.

A Single –ended Local Oscillator should be applied to the LOIP pin through an ac-coupling capacitor. The recommended LO drive power is -7 dBm. The LO return pin, LOIN, should be ac-coupled to ground though a low impedance path.

The RF output is available at pin 7, VOUT. This pin should also be ac-coupled. Both LOIP and VOUT have nominal broadband input and output impedances of 50 Ω and do not need further external matching.

Pin 10, TEMP, provides a output voltage that is proportional to ambient temperature. At 25 degC, the output voltage on this pin is 1.5 V. The temperature coefficient of this pin is 4.71 mV/°C.

EVALUATION BOARD

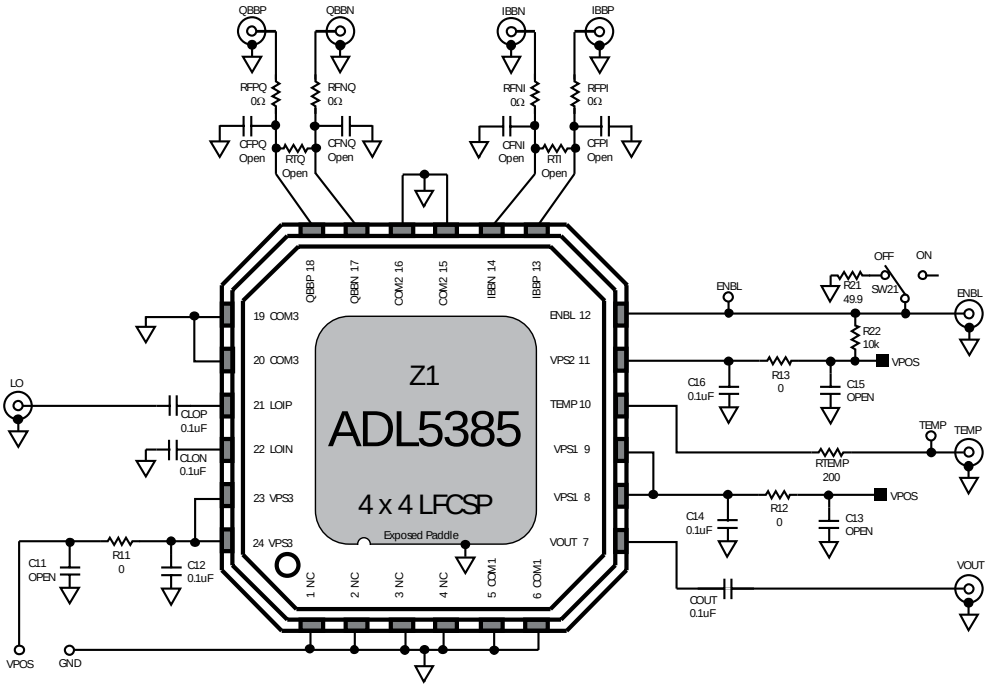

Figure 3. Evaluation Board Schematic

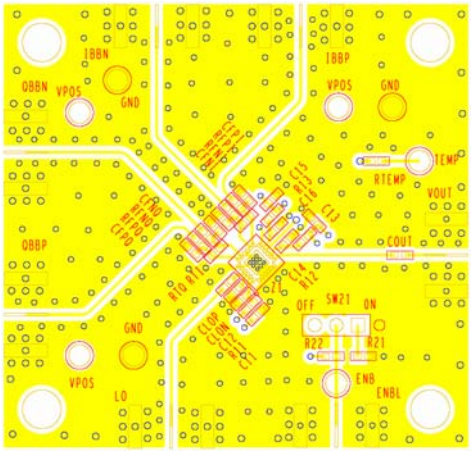

Figure 3. Layout of Evaluation Board, Top Layer

A populated ADL5385 evaluation board is available. The ADL5385 has an exposed paddle underneath the package, which is soldered to the board. The evaluation board is designed without any components on the underside of the board so that heat may be applied to the underside for easy removal and replacement of the ADL5385.

Table 3. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Power Supply and Ground Clip Leads	Not applicable
SW21	Chip Enable Select. SW21 sets the voltage on the ENBL pin. OFF = 0 V (disabled) ON = 5V (enabled)	SW21 = ON
RFNQ, CFNQ, RTQ, CFPQ, RFPQ, RFNI, CFNI, RTI, CFPI, RFPI	Baseband Input Filters: These components can be used to implement a low-pass filter for the baseband signals.	RFNQ, RFPQ, RFNI RFPI = 0 Ω (0402) RTQ, RTI = Open (0402) CFNQ,CFPQ,CFNI,CFPI = Open (0402)

OUTLINE DIMENSIONS

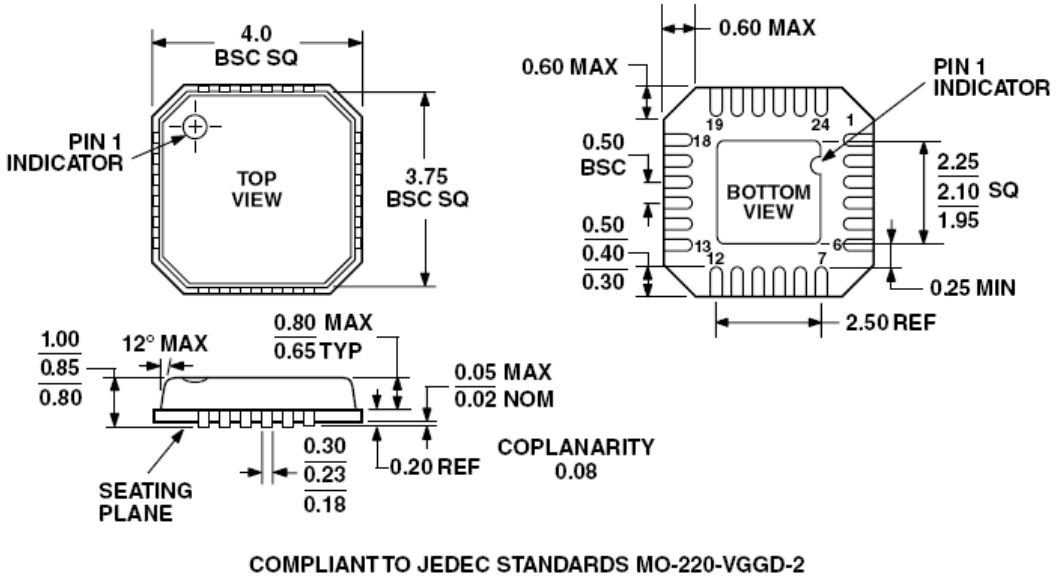

Figure 4. 24-Lead LFCSP with exposed paddle. Dimensions shown in millimeters

TABLE 4. ORDERING GUIDE

Model	Temperature Range (°C)	Package Description	Package Option
ADL5385ACPZ-R7[1]	–40 to +85	7" Tape and Reel	
ADL5385ACPZ-WP	–40 to +85	Waffle Pack	
ADL5385-EVAL		Evaluation Board	

[1] Z indicates Pb-free

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