

1.1 Scope.

This specification covers the requirements for a high speed 12-bit resolution bipolar current output D/A converter with double buffered latch and high stability buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
- 1	AD567SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-28.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to Power Ground	0 to +18V
V_{EE} to Power Ground	0 to -18V
Voltage on DAC Output (Pin 2)	-3V to +12V
Digital Inputs (Pins 10-15, 17-28) to Power Ground	-1.0V to +7.0V
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Power Dissipation	1000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C}/\text{W}$
 $\theta_{JA} = 60^\circ\text{C}/\text{W}$

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition ¹	Units
Relative Accuracy	RA	−1	1/2	1/2	3/4	All Bits with Positive Errors On. All Bits with Negative Errors On.	± LSB max
Differential Nonlinearity	DNL	−1	3/4	3/4	1	Major Carry Errors	± LSB max
Gain Error ²	A _E	−1	0.25	0.25		All Bits On	± % FSR max
Gain Temperature Coefficient	TCA _E	−1	30		30	All Bits On	± ppm/°C max
Unipolar Offset Error	V _{OS}	−1	0.05	0.05		All Bits Off	± % FSR max
Temperature Coefficient Unipolar Offset	TCV _{OS}	−1	2		2	All Bits Off	± ppm/°C max
Bipolar Zero Error ³	B _{PZE}	−1	0.15	0.15		MSB On, All Other Bits Off Bipolar	± % FSR max
B/P Zero Temperature Coefficient	TCB _{BZE}	−1	10		10	MSB On, All Other Bits Off Bipolar	± ppm/°C max
Reference Input Resistance	R _{IN}	−1	15 25				kΩ min kΩ max
Output Resistance	R _{OUT}	−1	6 10			Exclusive of Span Resistor	kΩ min kΩ min
Reference Output Voltage	V _{REF}	−1	9.9 10.10	9.9 10.10	9.9 10.10	Bipolar, 0.1mA External Load V _{CC} = +12V, V _{EE} = −12V ⁴	V min V max
Compliance Voltage	V _{CPL}	−1	1.5 10.0				− V min V max
Output Current Settling Time	t _{SL}	−1	500			See Figure 1	ns max
Output Current	I _{OUT}	−1	1.6 2.4 0.8 1.2	1.6 2.4 0.8 1.2		Unipolar All Bits On V _{IH} + 5.0V Bipolar All Bits On V _{IH} + 5.0V	− mA min − mA max − mA min − mA max
Power Supply Rejection Ratio	PSRR	−1	10 25	10 25		+ 11.4V ≤ V _{CC} ≤ + 16.5V − 16.5V ≤ V _{EE} ≤ − 11.4V	ppm of FSR/ % max
Power Supply Current	I _{CC} I _{EE}	−1 −1	5 25	5 25		V _{CC} = + 16.5V, V _{EE} = − 16.5V All Bits Low	mA max − mA max
Power Dissipation	P _D	−1	495	495		V _{CC} = + 16.5V, V _{EE} = − 16.5V All Bits Low	mW max
Digital Input High Voltage	V _{IH}	−1	2.0 5.5	2.0			V min V max
Digital Input Low Voltage	V _{IL}	−1	0.8	0.8			V max
Digital Input High Current	I _{IH}	−1	300	300		V _{IH} = 5.5V	μA max
Digital Input Low Current	I _{IL}	−1	100	100		V _{IL} = 0.0V	μA max
Write Pulse Width	t _{WR}	−1	100			See Note 5	ns min
Data Setup Time	t _{OW}	−1	50			See Note 5	ns min
Data Hold Time	t _{DH}	−1	10			See Note 5	ns min
CS Valid to End of $\overline{WR}$	t _{CW}	−1	100			See Note 5	ns min
Address Valid End of $\overline{WR}$	t _{AW}	−1	100			See Note 5	ns min
Latch Functionality	A _{Ed}	−1	1	1	1	See Notes 6 and 7	± LSB max
Latch Functionality	V _{OSA}	−1	1	1	1	See Note 6	± LSB max

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

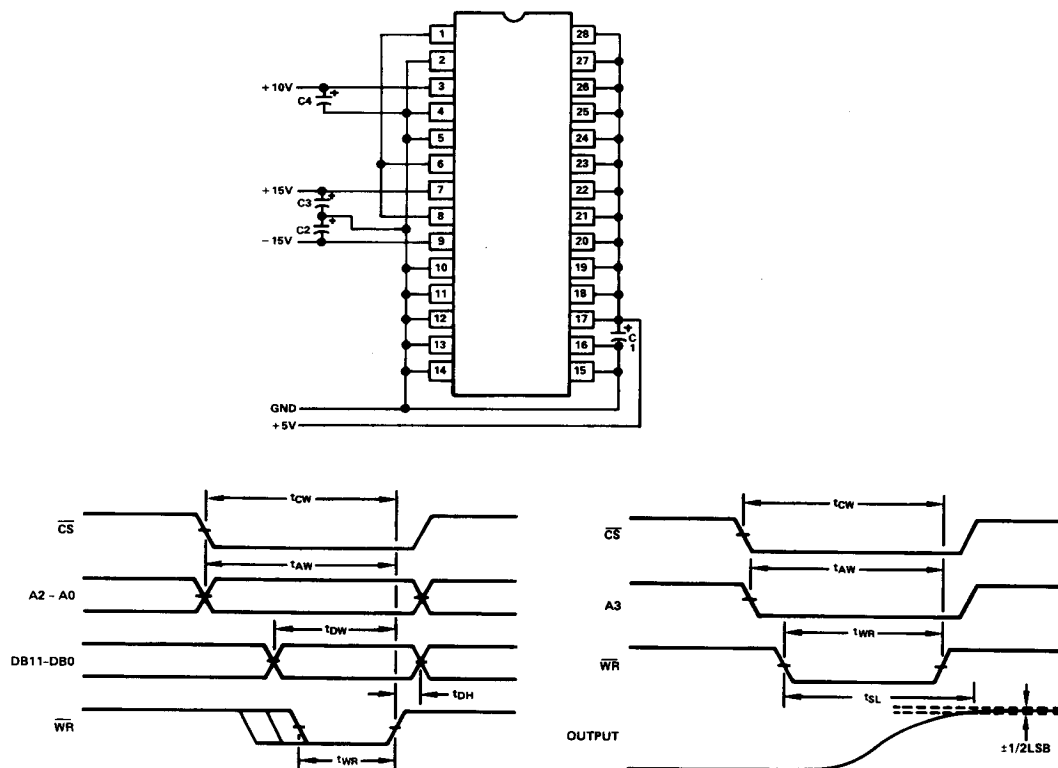


Figure 1.

Table 2. Truth Table

CS	WR	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No Operation
X	1	X	X	X	X	No Operation
0	0	1	1	1	0	Enable 4 LSBs of First Rank
0	0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	0	All Latches Transparent

"X" = Don't Care