2.7 V to 5.5 V, <100 µA, 14 Bit *nano*DAC™ D/A, Tiny SC70 Package

Preliminary Technical Data

AD5641

FEATURES

6-lead SC70 package
Power-down to <100 nA @ 3 V
Single 14-bit DAC
- B Version: ±4 LSB INL , A Version: ±8 LSB INL
Micropower operation: max 100 µA @ 5 V
2.7 V to 5.5 V power supply
Guaranteed monotonic by design
Power-on-reset to 0 V with brownout detection
3 power-down functions
Low power serial interface with Schmitt-triggered inputs
On-chip output buffer amplifier, rail-to-rail operation
SYNC interrupt facility

APPLICATIONS

Voltage Level Setting
Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators

FUNCTIONAL BLOCK DIAGRAM

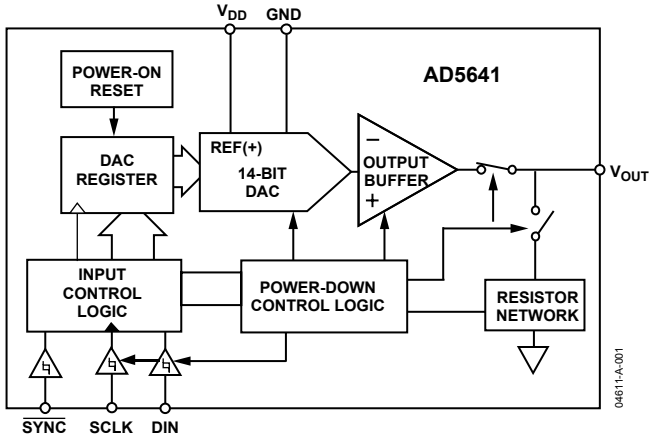

Figure 1

RELATED DEVICES

Part Number	Description
AD5601/11/21	2.7 V to 5.5 V, <100 µA, 8/10/12Bit ***nano*DAC™** D/A, SPI Interface, SC70 Package

GENERAL DESCRIPTION

The AD5641, a member of the ***nano*DAC™** family, is a single 14-bit buffered voltage out DAC that operates from a single 2.7 V to +5.5 V supply consuming <100 µA at 5 V, and comes in a tiny SC70 package. Its on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5641 utilizes a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards.

The reference for AD5641 is derived from the power supply inputs and thus gives the widest dynamic output range. The part incorporates a power-on-reset circuit that ensures the DAC output powers up to 0 V and remains there until a valid write takes place to the device. The part contains a power-down feature that reduces the current consumption of the device to <100 nA at 3 V and provides software selectable output loads while in power-down mode. The part is put into power-down mode over the serial interface. The low power consumption of this part in normal operation makes it ideally suited to portable battery operated equipment. The combination of small package and low power make these devices idea for level setting requirements such as generating bias or control voltages in space constrained and power sensitive applications.

The AD5641 is designed with new technology and comes in a tiny space saving SC70 package.

Rev. PrB

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PRODUCT HIGHLIGHTS

1. Available in 6-lead SC70.
2. Low power, single-supply operation. This part operates from a single 2.7 V to 5.5 V supply and typically consumes 0.2 mW at 3 V and 0.5 mW at 5 V, making it ideal for battery-powered applications.
3. The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a typical slew rate of 0.5 V/μs.
4. Reference derived from the power supply.
5. High speed serial interface with clock speeds up to 30 MHz.
6. Designed for very low power consumption. The interface only powers up during a write cycle.
7. Power-down capability. When powered down, the DAC typically consumes <100 nA at 3 V.
8. Brown out detection on power-on-reset.

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REVISION HISTORY

Revision PrB: Preliminary Version

AD5641—SPECIFICATIONS

Table 1. V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE					
Resolution	14			Bits	
Relative Accuracy[2]			±4	LSB	B Grade
			±8	LSB	A Grade
Differential Nonlinearity[2]			±1	LSB	Guaranteed Monotonic by Design.
Zero Code Error		±0.2		LSB	All 0s Loaded to DAC Register.
Offset Error		±0.125		% of FSR	
Full-Scale Error		±0.01		LSB	All 1s Loaded to DAC Register.
Gain Error		±0.04		% of FSR	
Zero Code Error Drift		5.0		µV/°C	
Gain Temperature Coefficient		2.0		ppm of FSR/°C	
Output CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Output Voltage Settling Time		8	18	µs	Code ¼ to ¾
Slew Rate		0.5		V/µs	
Capacitive Load Stability		470		pF	$R_L = \infty$
		1000		pF	RL = 2 kΩ
Output Noise Spectral Density		120		nV/Hz	DAC code=TBD , 10 kHz
Noise		TBD			DAC code=TBD 0.1-10Hz Bandwidth
Digital-to-Analog Glitch Impulse		10		nV-s	1 LSB Change Around Major Carry.
Digital Feedthrough		0.5		nV-s	
DC Output Impedance		1			
Short Circuit Current		20		mA	V_{DD} = +3/5 V
LOGIC INPUTS					
Input Current			±1	µA	
V_{INL}, Input Low Voltage	0.8			V	V_{DD} = +5 V
V_{INL}, Input Low Voltage	0.6			V	V_{DD} = +2.7 V
V_{INH}, Input High Voltage			1.8	V	V_{DD} = +5 V
V_{INH}, Input High Voltage			1.4	V	V_{DD} = +2.7 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All Digital Inputs at Zero or V_{DD}
I_{DD} (Normal Mode)					DAC Active and Excluding Load Current
V_{DD} = +4.5 V to +5.5 V			100	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = +2.7 V to +3.6 V			70	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)					
V_{DD} = +4.5 V to +5.5 V		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = +2.7 V to +3.6 V		0.05	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY					
I_{OUT}/I_{DD}		TBD		%	I_{LOAD} = 2 mA. V_{DD} = +5 V

[1] Temperature ranges are as follows: B Version: –40°C to +125°C, typical at 25°C.
[2] Linearity calculated using a reduced code range 120-16179.
[3] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

Table 2. V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 2.

Parameter	Limit[4]	Unit	Test Conditions/Comments
t_1[5]	33	ns min	SCLK Cycle Time
t_2	13	ns min	SCLK High Time
t_3	12	ns min	SCLK Low Time
t_4	13	ns min	$\overline{SYNC}$ to SCLK Falling Edge Setup Time
t_5	5	ns min	Data Setup Time
t_6	4.5	ns min	Data Hold Time
t_7	0	ns min	SCLK Falling Edge to SYNC Rising Edge
t_8	33	ns min	Minimum SYNC High Time
t_9	13	ns min	$\overline{SYNC}$ Rising Edge to next SCLK Fall Ignore

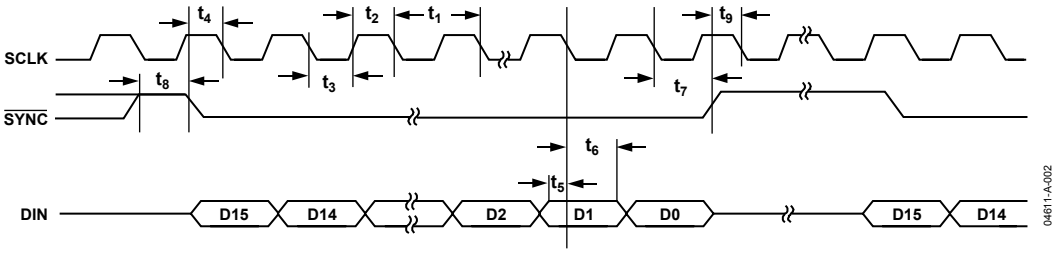

Figure 2. Timing Diagram

[4] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[5] Maximum SCLK frequency is 30 MHz.

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted

Parameter	Rating
V_{DD} to GND	–0.3 V to + 7.0 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +160°C
Maximum Junction Temperature	150°C
SC70 Package	
θ_{JA} Thermal Impedance	332°C/W
θ_{JA} Thermal Impedance	120°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	2.0 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Model	Temperature Range	Description	Package Options
AD5641BKS	-40°C to 125°C	±4.0 LSB INL	KS-6
AD5641AKS	-40°C to 125°C	±8.0 LSB INL	KS-6

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

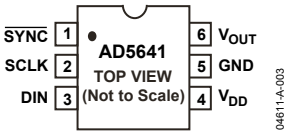

Figure 3. AD5641-1 SC70 (Top View)

Table 4. Pin Function Descriptions

Mnemonic	Function
V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and V_{DD} should be decoupled to GND.
V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
$\overline{SYNC}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 16th clock cycle unless $\overline{SYNC}$ is taken high before this edge in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC.
SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
D_{IN}	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
GND	Ground Reference Point for All Circuitry on the Part.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 2.

Differential Nonlinearity

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 3.

Zero-Code Error

Zero-code error is a measure of the output error when zero code (0000Hex) is loaded to the DAC register. Ideally the output should be 0 V. The zero-code error is always positive in the AD5641 because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 6.

Full-Scale Error

Full-scale error is a measure of the output error when full-scale code (FFFF Hex) is loaded to the DAC register. Ideally the output should be VDD – 1 LSB. Full-scale error is expressed in percent of full-scale range. A plot of full-scale error vs. temperature can be seen in Figure 6.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error

Total Unadjusted Error (TUE) is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot can be seen in Figure 4.

Zero-Code Error Drift

This is a measure of the change in zero-code error with a change in temperature. It is expressed in μV/°C.

Gain Error Drift

This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition (7FFF Hex to 8000 Hex). See Figure 19.

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

TYPICAL PERFORMANCE CHARACTERISTICS

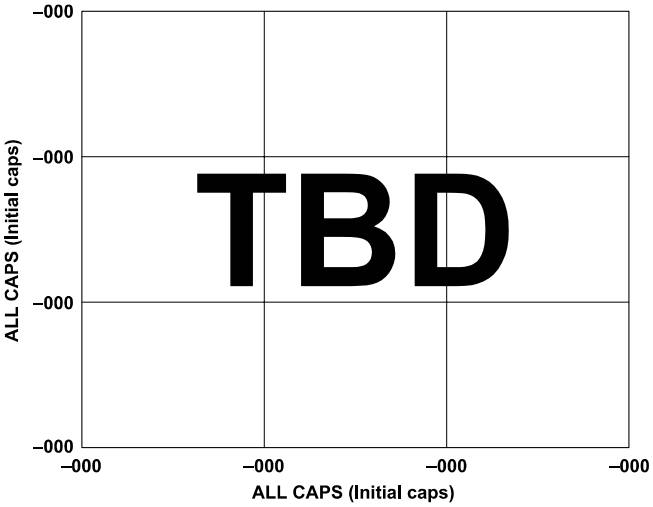

Figure 4. Typical INL Plot

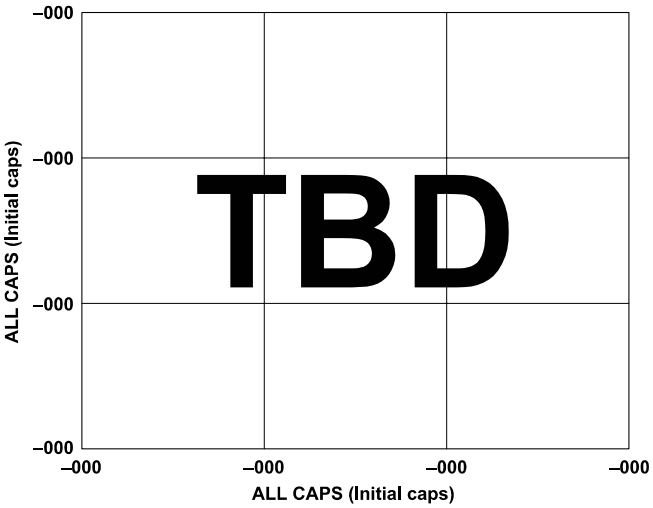

Figure 5. Total Unadjusted Error Plto.

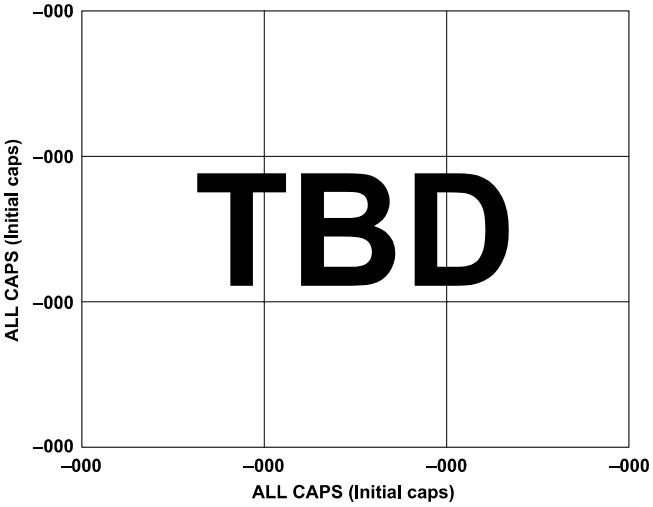

Figure 6. Zero Scale Error and Full Scale Error vs. Temperature

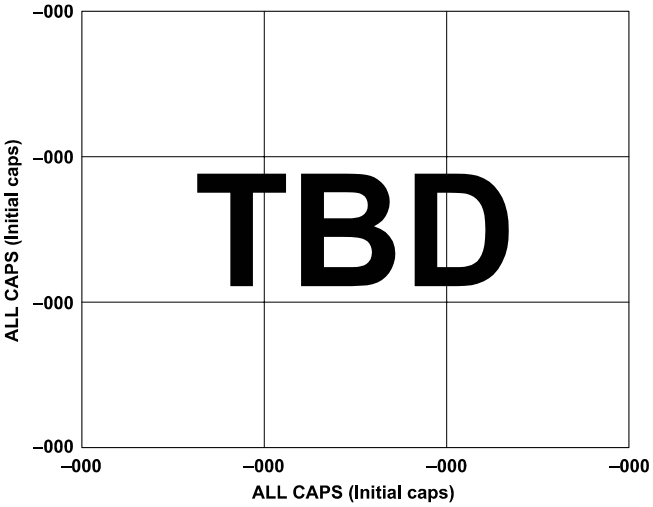

Figure 7. Typical DNL Plot

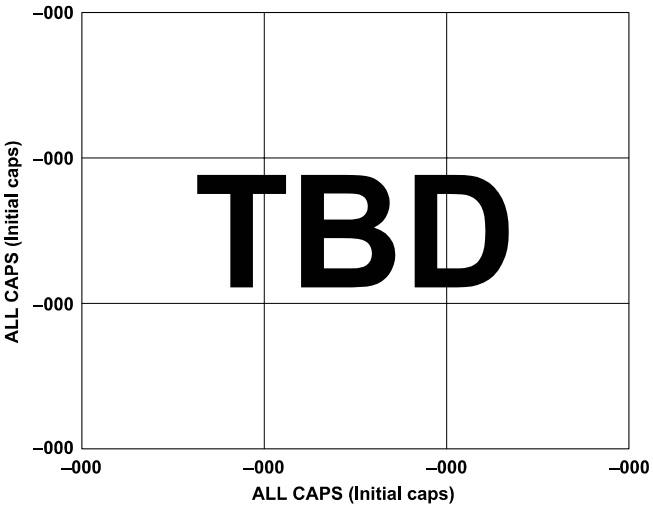

Figure 8. INL and DNL vs Supply

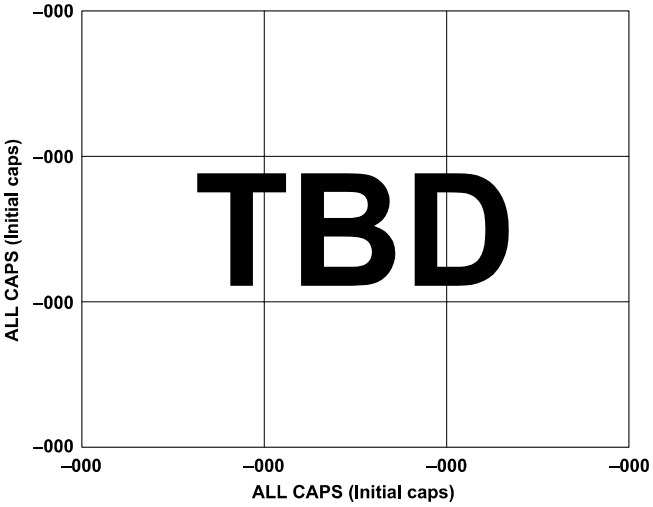

Figure 9. I_{DD} Histogram @ V_{DD} = 3 V/5 V

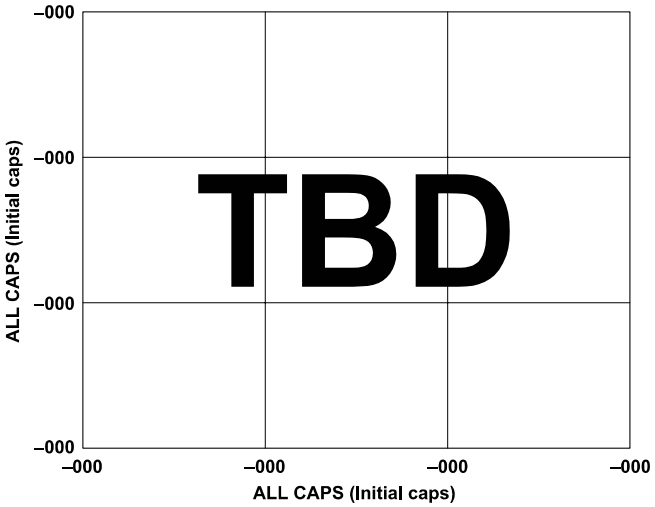

Figure 10. Source and Sink Current Capability

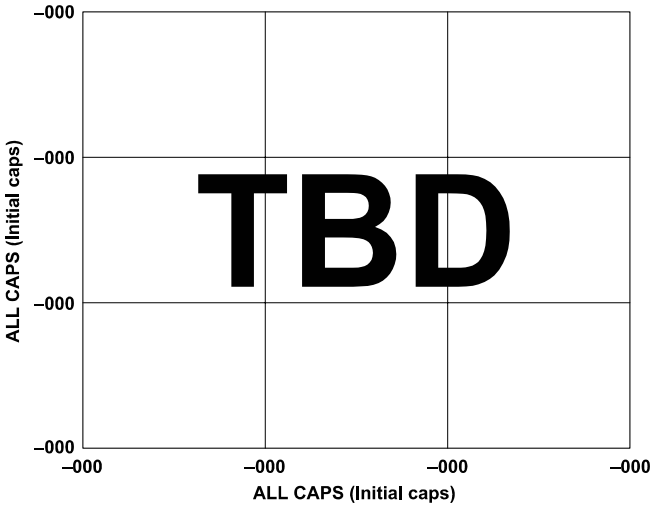

Figure 13. Supply Current vs Code.

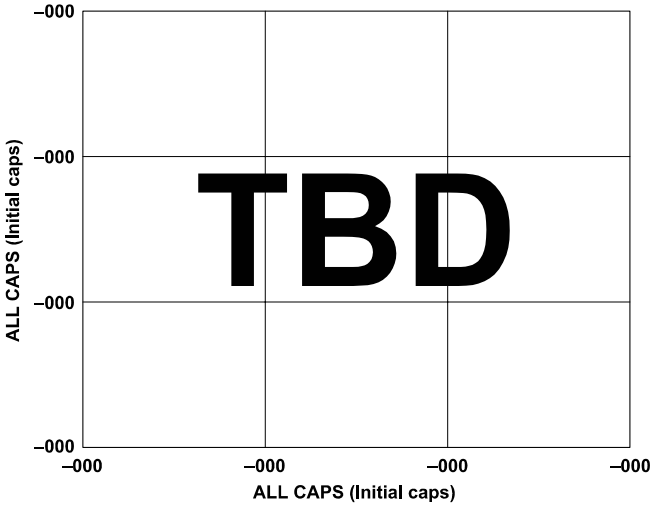

Figure 11. Supply Current vs. Temperature

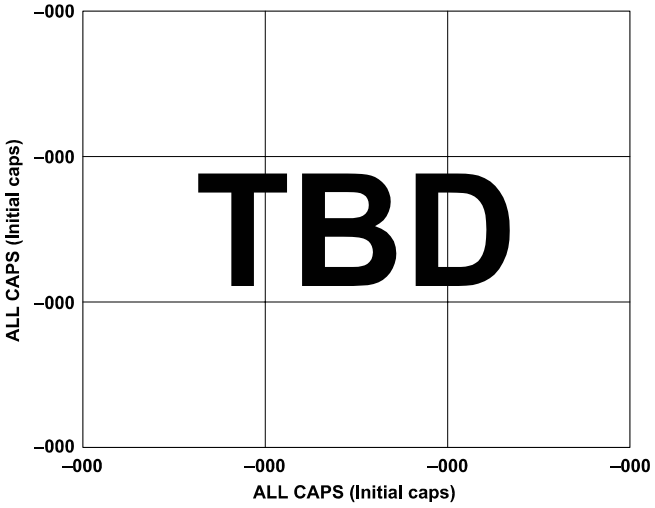

Figure 14. Supply Current vs. Supply Voltage

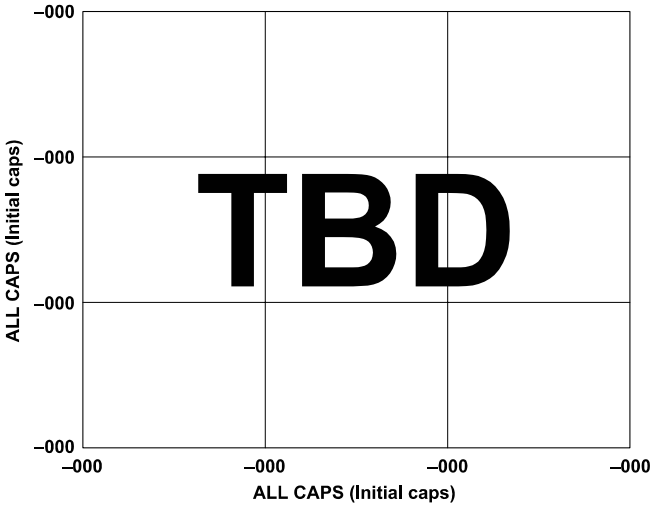

Figure 12. Full Scale Settling Time

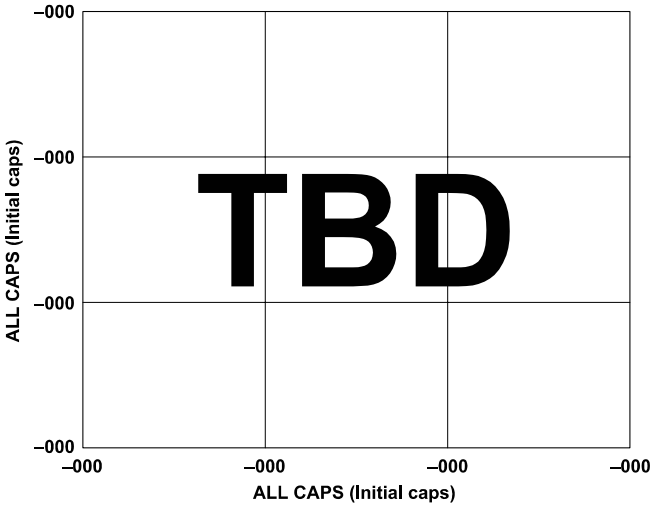

Figure 15. Half Scale Settling Time

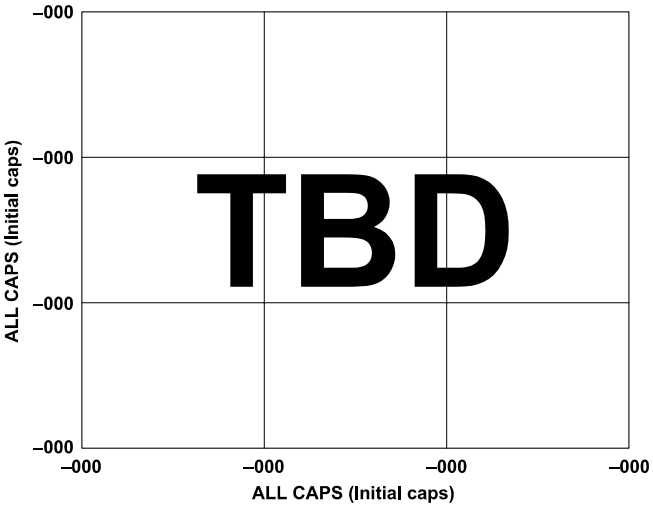

Figure 16. Power on Reset to 0 V

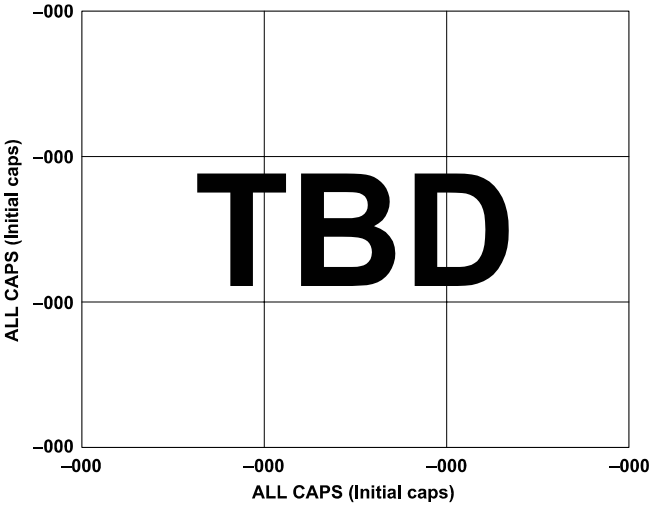

Figure 17. Digital to Analog Glitch Impulse

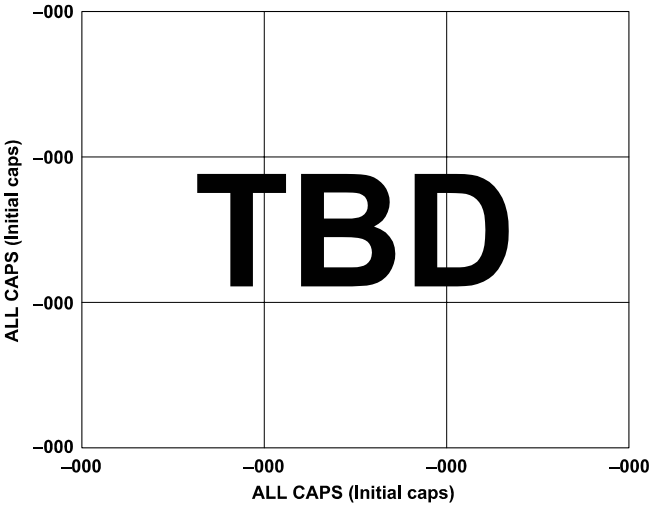

Figure 18. Output Spectral Density 100k Bandwidth

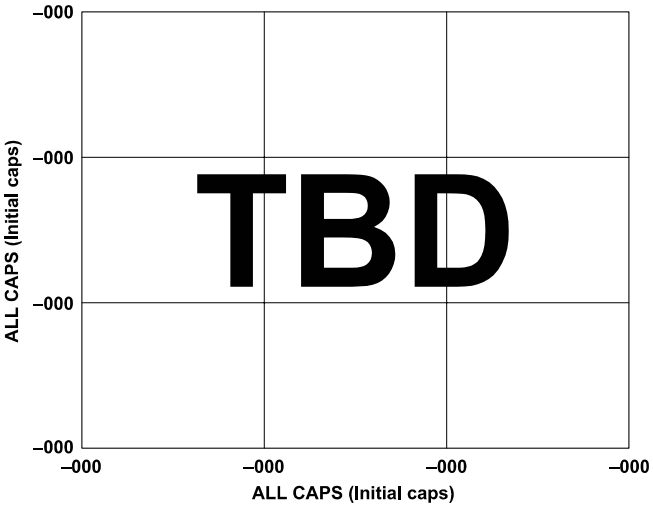

Figure 19. Exiting Power-Down

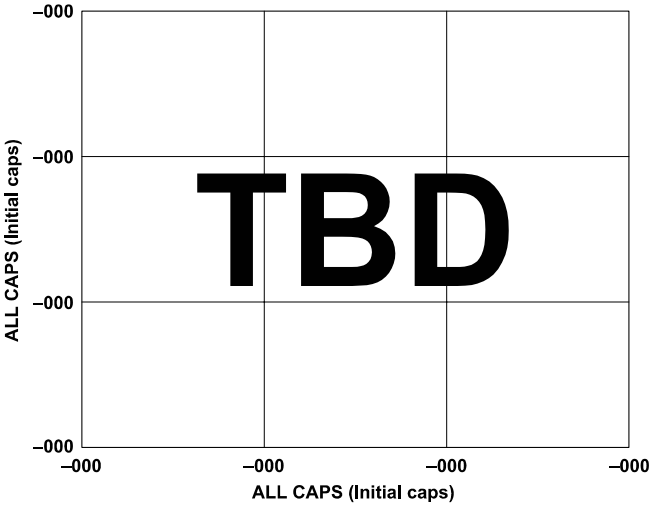

Figure 20. Harmonic Distortion on Digitally Generated Waveform.

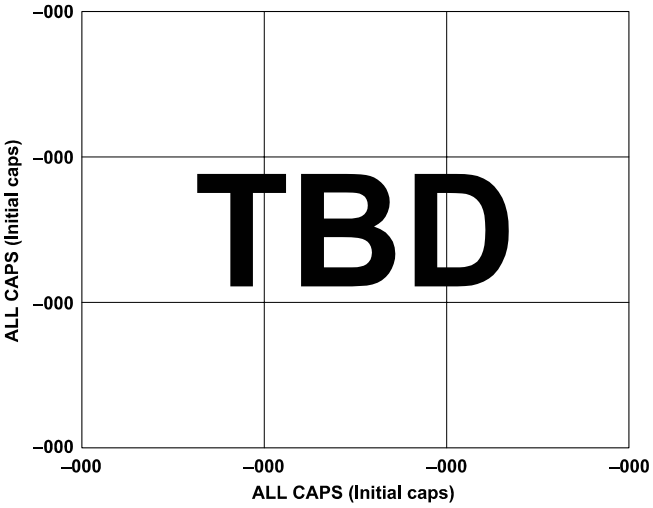

Figure 21. 0.1 Hz to 10 Hz Noise Plot

GENERAL DESCRIPTION

D/A SECTION

The AD5641 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 22 shows a block diagram of the DAC architecture.

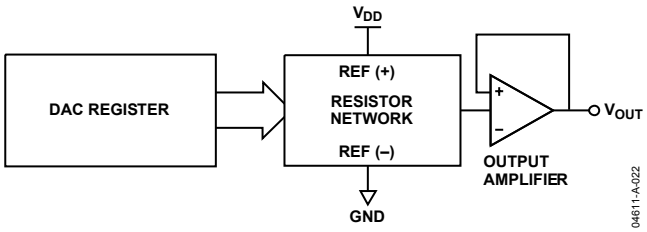

Figure 22. DAC Architecture

Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{DD} \cdot \left(\frac{D}{16384} \right)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 16384.

RESISTOR STRING

The resistor string section is shown in Figure 21. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 9 and Figure 10. The slew rate is 0.5 V/μs with a half-scale settling time of 8 μs with the output unloaded.

SERIAL INTERFACE

The AD5641 has a three-wire serial interface (SYNC, SCLK and DIN), which is compatible with SPI, QSPI and MICROWIRE interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the SYNC line low. Data from the DIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5641compatible with high speed DSPs. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (i.e., a change in DAC register contents and/or a change in the mode of operation). At this stage, the SYNC line may be kept low or be brought high. In either case, it must be brought high for a minimum of 33 ns before the next write sequence so that a falling edge of SYNC can initiate the next write sequence. Since the SYNC buffer draws more current when V_{IN} = 1.8 V than it does when V_{IN} = 0.8 V, SYNC should be idled low between write sequences for even lower power operation of the part, as mentioned above; however, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 23). The first two bits are control bits that control which mode of operation the part is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next sixteen bits are the data bits. These are transferred to the DAC register on the 16th falling edge of SCLK.

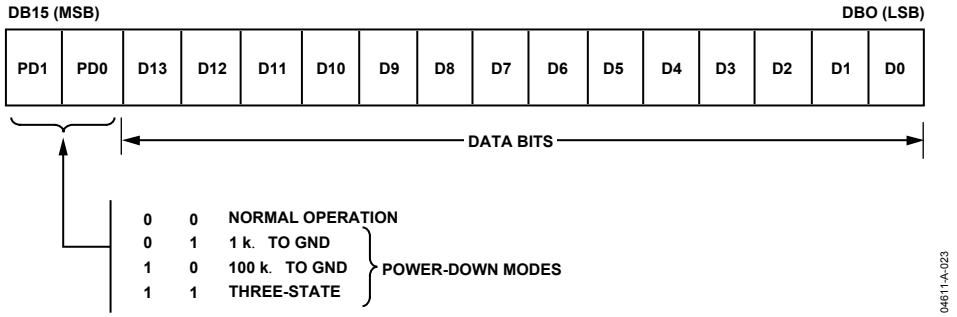

Figure 23. Input Register Contents

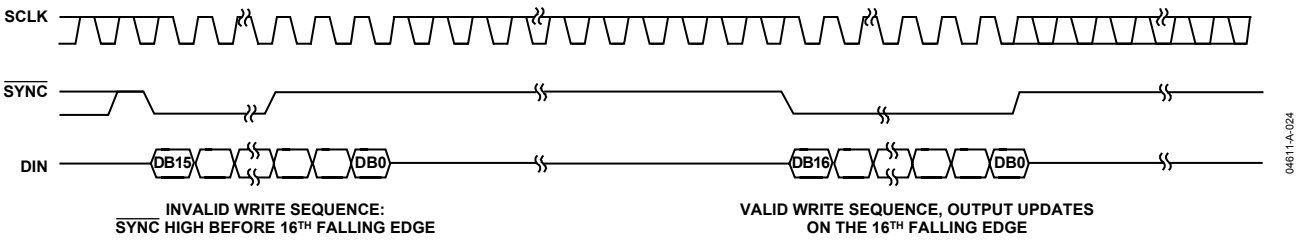

Figure 24. SYNC Interrupt Facility

SYNC INTERRUPT

In a normal write sequence, the SYNC line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if SYNC is brought high before the 16th falling edge this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents or a change in the operating mode occurs—see Figure 24.

POWER-ON-RESET

The AD5641 contains a power-on-reset circuit that controls the output voltage during power-up. The DAC register is filled with zeros and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

POWER-DOWN MODES

The AD5641 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB17 and DB16) in the control register. Table 5 shows how the state of the bits corresponds to the mode of operation of the device.

Table 5. Modes of Operation for the AD5641

DB15	DB14	Operating Mode
0	0	Normal Operation Power-Down Mode
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-State

When both bits are set to 0, the part works normally with its normal power consumption of 100 μA max at 5 V. However, for the three power-down modes, the supply current falls to <100 nA at 3 V). Not only does the supply current fall but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor or a 100 kΩ resistor, or is left open-circuited (three-state). Figure 25 shows the output stage.

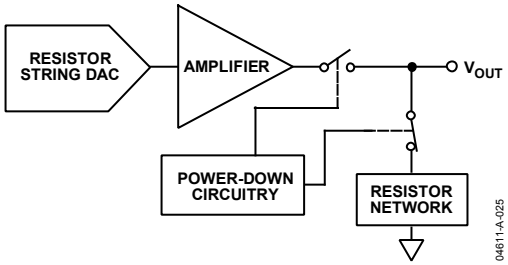

Figure 25. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs for V_{DD} = 3 V. See Figure 18 for a plot.

MICROPROCESSOR INTERFACING

AD5641 to ADSP-2101/ADSP-2103 Interface

Figure 26 shows a serial interface between the AD5641 and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set up to operate in SPORT transmit alternate framing mode. The ADSP-2101/ADSP-2103 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled.

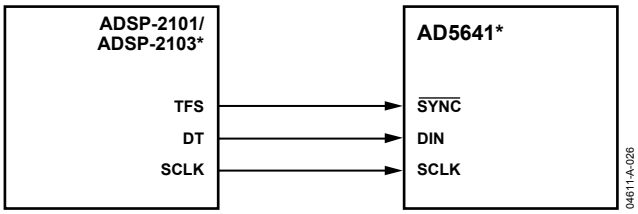

Figure 26. AD5641 to ADSP-2101/ADSP-2103 Interface

AD5641 to 68HC11/68L11 Interface

Figure 27 shows a serial interface between the AD5641 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5641, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that its CPOL bit is a 0 and its CPHA bit is a 1. When data is being transmitted to the DAC, the SYNC line is taken low (PC7). When the 68HC11/68L11 is configured as above, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to load data to the AD5641, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

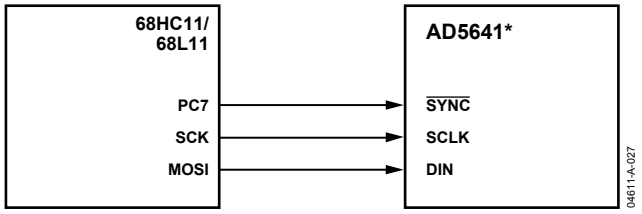

Figure 27. AD5641 to 68HC11/68L11 Interface

AD5641 to Blackfin® ADSP-BF53X Interface

Figure 28 shows a serial interface between the AD5641 and the Blackfin ADSP-53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5641, the setup for the interface is as follows: DT0PRI drives the SDIN pin of the AD5641, while TSCLK0 drives the SCLK of the part. The SYNC is driven from TFS0.

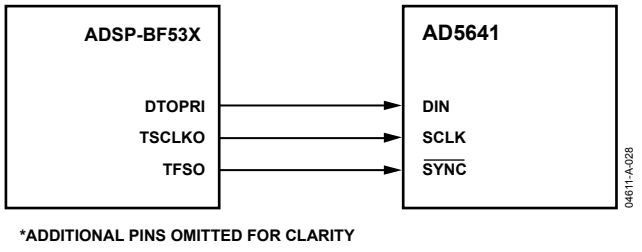

Figure 28. AD5641 to Blackfin ADSP-BF53X Interface

AD5641 to 80C51/80L51 Interface

Figure 29 shows a serial interface between the AD5641 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TXD of the 80C51/80L51 drives SCLK of the AD5641, while RXD drives the serial data line of the part. The SYNC signal is again derived from a bit programmable pin on the port. In this case, port line P3.3 is used. When data is to be transmitted to the AD5641, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5641 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

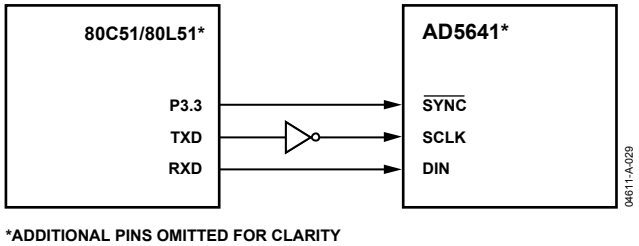

Figure 29. AD5641 to 80C51/80L51 Interface

AD5641 to MICROWIRE Interface

Figure 28 shows an interface between the AD5641 and any MICROWIRE compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5641 on the rising edge of the SK.

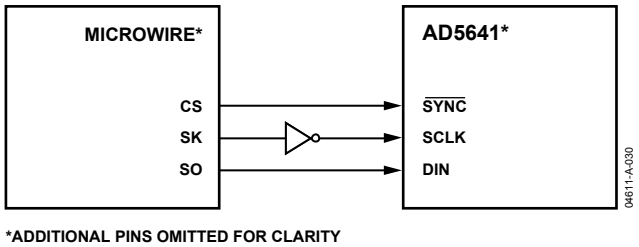

Figure 30. AD5641 to MICROWIRE Interface

APPLICATIONS

CHOOSING A REFERENCE AS POWER SUPPLY FOR AD5641

The AD5641 comes in a tiny SC70 package with less than 100 µA supply current. Because of this, the choice of reference depends on the application requirement. For space saving applications, the ADR425 is available in an SC70 package and has excellent drift at 3ppm/°C. It also provides very good noise performance at 3.4 µV p-p in the 0.1 Hz to 10 Hz range.

Because the supply current required by the AD5641 is extremely low, it is ideal for low supply applications. The ADR293 voltage reference is recommended in this case. This requires 15 µA of quiescent current and can therefore drive multiple DACs in the one system if required.

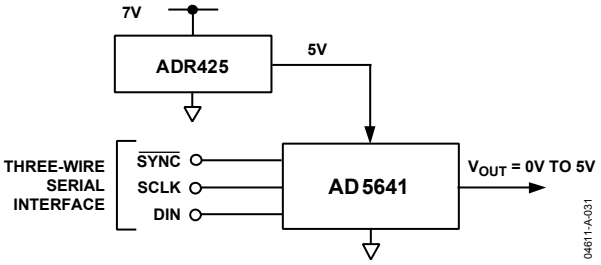

Figure 31. ADR425 as Power Supply to AD5641

Examples of some recommended precision references for use as supply to the AD5641 are shown in Table 6.

Table 6. Precision References for Use with AD5641

Part No.	Initial Accuracy (mV max)	Temperature Drift (ppm/°C max)	0.1–10 Hz Noise (µV p-p typ)
ADR435	±6	3	3.4
ADR425	±6	3	3.4
ADR02	±5	3	15
ADR395	±6	25	5

BIPOLAR OPERATION USING THE AD5641

The AD5641 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 32. The circuit in Figure 32 will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \cdot \left(\frac{D}{16384} \right) \cdot \left(\frac{R1+R2}{R1} \right) - V_{DD} \cdot \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0–16384). With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ:

$$V_O = \left(\frac{10 \cdot D}{16384} \right) - 5\text{V}$$

This is an output voltage range of ±5 V with 0000Hex corresponding to a –5 V output and 3FFF Hex corresponding to a +5 V output.

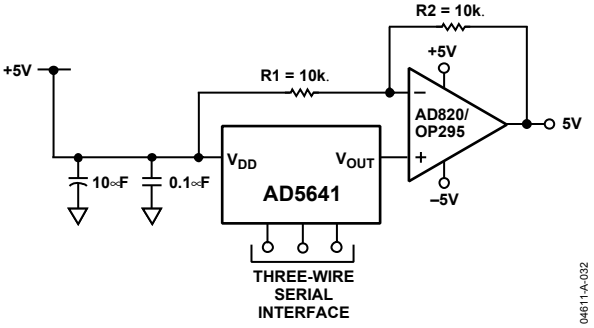

Figure 32. Bipolar Operation with the AD5641

USING AD5641 WITH AN OPTO-ISOLATED INTERFACE

In process-control applications in industrial environments, it is often necessary to use an opto-isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur in the area where the DAC is functioning. Opto-isolators provide isolation in excess of 3 kV. Because the AD5641 uses a 3-wire serial logic interface, it requires only three opto-isolators to provide the required isolation (see Figure 33). The power supply to the part also needs to be isolated. This is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5641.

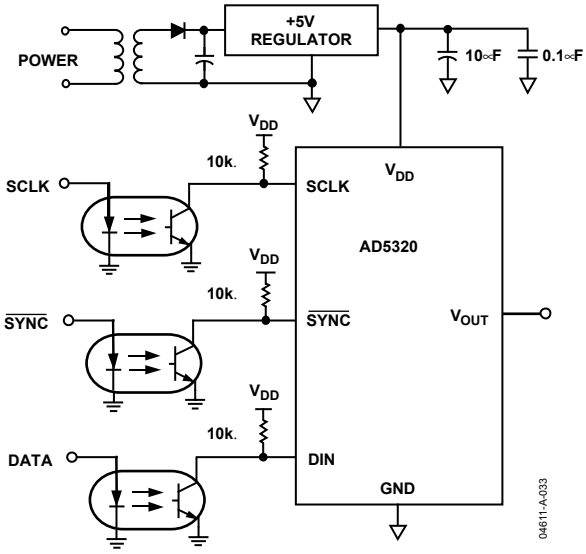

Figure 33. AD5641 with an Opto-Isolated Interface

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5641 should have separate analog and digital sections, each having its own area of the board. If the AD5641 is in a system where other devices require an AGND to DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5641.

The power supply to the AD5641 should be bypassed with 10 μF and 0.1 μF capacitors. The capacitors should be physically as close as possible to the device with the 0.1 μF capacitor ideally right up against the device. The 10 μF capacitors are the tantalum bead type. It is important that the 0.1 μF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), e.g., common ceramic types of capacitors. This 0.1 μF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

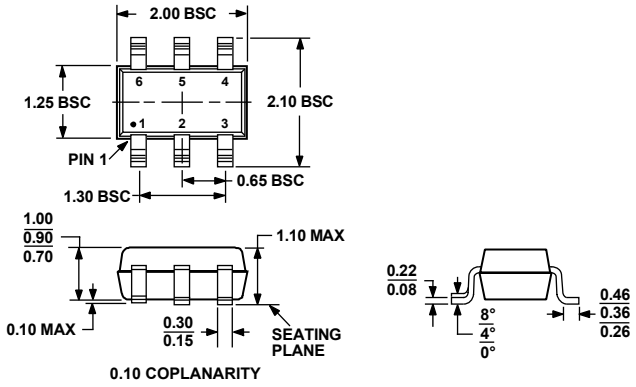

Figure 34. 6-Lead Plastic Surface Mount Package [SC70]
(KS-6)
Dimensions shown in millimeters

C04611–0–4/04(PrB)