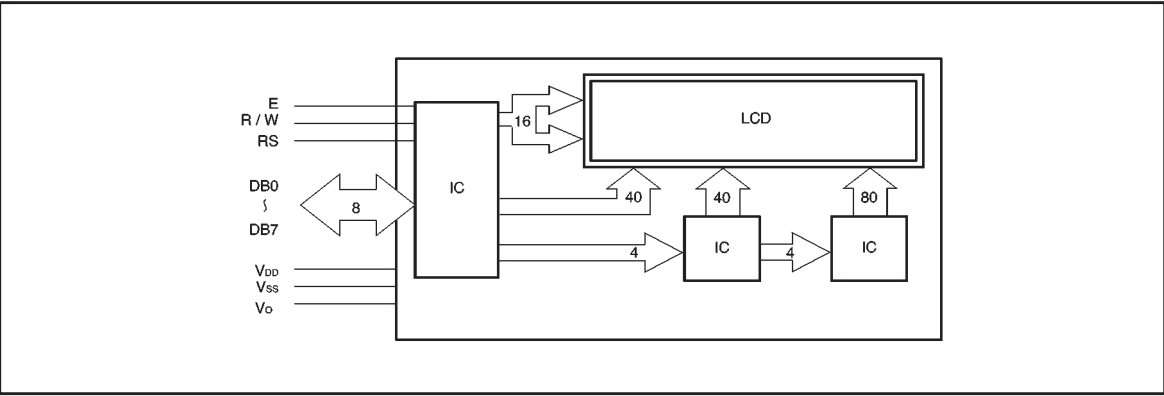


●Block diagram



●Pin assignments

Pin no.	Signal	Pin no.	Signal
1	V _{SS}	8	DB1
2	V _{DD}	9	DB2
3	V _O	10	DB3
4	RS	11	DB4
5	R / W	12	DB5
6	E	13	DB6
7	DB0	14	DB7

●Power supply example

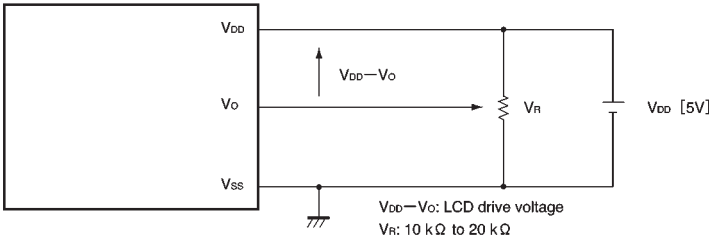


Fig.1

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic power supply voltage	V _{DD} -V _{SS}	0	—	6.5	V
LCD drive voltage	V _{DD} -V _O	0	—	6.5	V
Input voltage	V _{IN}	V _{SS}	—	V _{DD}	V
Operating temperature	T _{opr}	0	—	50	°C
Storage temperature	T _{stg}	-20	—	70	°C

●Electrical characteristics (V_{DD} = 5.0 V ± 0.25 V, Ta = 25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage	V _{IH}	2.2	—	V _{DD}	V	
Input low level voltage	V _{IL}	—	—	0.6	V	
Output high level voltage	V _{OH}	2.4	—	—	V	— I _{OH} = 0.205mA
Output low level voltage	V _{OL}	—	—	0.4	V	I _{OL} = 1.2mA
Power supply current	I _{DD}	—	2	4	mA	V _{DD} = 5V

●Optical characteristics (Ta = 25 °C, ϕ = 0 °)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Rise time	t _r	—	100	250	ms	θ = 10°, ϕ = 0°
Fall time	t _d	—	150	250	ms	θ = 10°, ϕ = 0°
Contrast ratio	K	—	3	—	—	θ = 10°, ϕ = 0°
Viewing angle	θ ₁	—	—	10	deg	ϕ = 0°, K ≥ 1.4
	θ ₂	40	—	—	deg	ϕ = 0°, K ≥ 1.4
	ϕ	±30	—	—	deg	θ ₁ = 20°, K ≥ 1.4

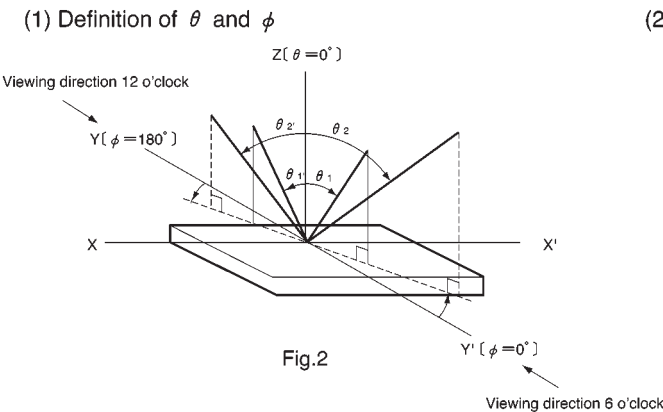


Fig.2

(2) Definition of viewing angles θ₁ and θ₂

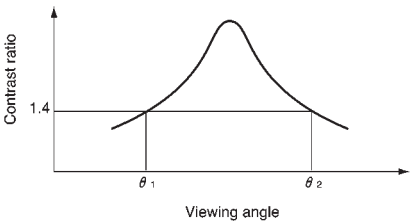


Fig.3

(3) Definition of contrast ratio“K”

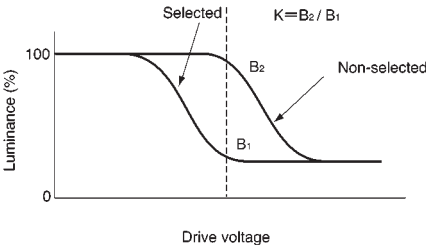


Fig.4

(4) Definition of optical response

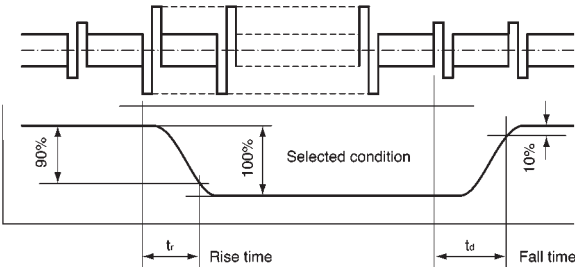


Fig.5

●Timing chart
(1) Writing

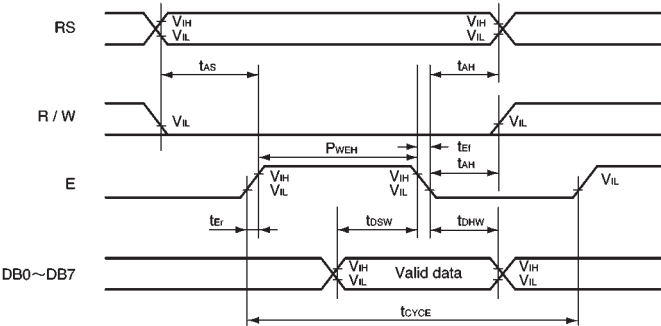


Fig. 6

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Enable cycle time	t_{CYCE}	500	—	—	ns	Fig.6
Enable pulse time	P_{WEH}	230	—	—	ns	Fig.6
Enable rise and fall time	t_{ER}, t_{EH}	—	—	20	ns	Fig.6
Address setup time	t_{AS}	40	—	—	ns	Fig.6
Address hold time	t_{AH}	10	—	—	ns	Fig.6
Data setup time	t_{DSW}	80	—	—	ns	Fig.6
Data hold time	t_{DHW}	10	—	—	ns	Fig.6

(2) Reading

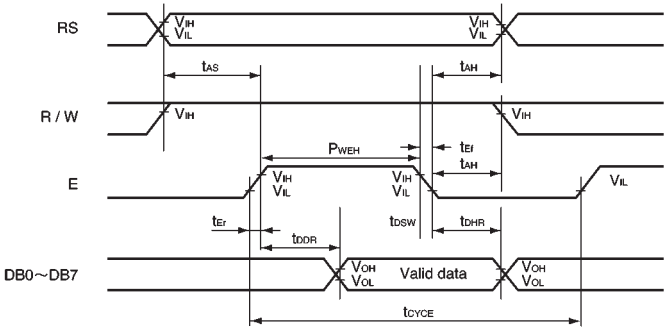


Fig. 7

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Enable cycle time	t _{CYCE}	500	—	—	ns	Fig.7
Enable pulse time	P _{WEH}	230	—	—	ns	Fig.7
Enable rise and fall time	t _{er} , t _{ef}	—	—	20	ns	Fig.7
Address setup time	t _{AS}	40	—	—	ns	Fig.7
Address hold time	t _{AH}	10	—	—	ns	Fig.7
Data delay time	t _{DDR}	—	—	160	ns	Fig.7
Data hold time	t _{DHR}	5	—	—	ns	Fig.7

● Pin functions

Symbol	Level	Input / output	Function
V _{SS}	—	—	GND : 0V
V _{DD}	—	—	5V
V _O	—	—	
RS	H / L	Input	Register selection signal. 0: Instruction register (writing) Busy flag, address counter (reading) 1: Data register (reading / writing)
R / W	H / L	Input	Reading (R) and writing (W) selection signal. “0” : Writing MPU → LCD module “1” : Reading MPU ← LCD module
E	H,H→L	Input	Data reading and writing start signal.
DB0 } DB3	H / L	Input / output	The lower 4 line data buses are bi-directional and used for data transfer between the MPU and the module. They are not used during 4-bit operation.
DB4 } DB7	H / L	Input / output	The upper 4 line data buses are bi-directional and used for data transfer between the MPU and the module. DB7 can also be used as a busy flag.

Note: In order to be able to interface with 4-bit or 8-bit MPUs, the module supports data transfer with two transmissions of 4 bits at a time or one transmission of 8 bits at once.

- (1) When the interface data length is 4 bits, data is transferred along DB4 through DB7 buses and DB0 through DB3 buses are not used. Data transfer is completed after two transfers of 4 bit data. First the upper nibble (contents of DB4 through DB7 during 8-bit interfacing) is transferred and then the lower nibble (contents of DB0 through DB3 during 8-bit interfacing) is transferred.
- (2) When the interface data length is 8 bits, the data DB0 through DB7 is transferred along the eight data buses.

● Instructions

Instruction	Code										Description	Execution time	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		f _{CP} =250kHz	
Clear display	0	0	0	0	0	0	0	0	0	1	Clears display and sets address 0 of DD RAM to address counter.	1.64ms	
Home cursor	0	0	0	0	0	0	0	0	1	*	Sets address 0 of DD RAM to address counter and returns a shifted display to original position. The contents of DD RAM are unchanged.	1.64ms	
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies whether or not to shift display. This operation occurs when reading or writing data.	40 μs	
Display on / off control	0	0	0	0	0	0	1	D	C	B	Turns display on or off [D], turns cursor on or off [C], or blinks the character at the cursor position [B].	40 μs	
Cursor / display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor or shifts display without changing the DD RAM.	40 μs	
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length [DL], number of lines displayed [N], and character font [F].	40 μs	
CG RAM address set	0	0	0	1	A _{CG}					Sets the CG RAM address. Data received after this is CG RAM data.		40 μs	
DD RAM address set	0	0	1	A _{DD}					Sets the DD RAM address. Data received after this is DD RAM data.		40 μs		
Read busy flag address	0	1	BF	AC					Reads the busy flag signifying internal operations in progress and reads the contents of the address counter.		0 μs		
Write data to CG or DD RAM	1	0	Write Data					Data is written from the DD RAM or CG RAM.		46 μs			
Read data from CG or DD RAM	1	1	Read Data					Data is read to DD RAM or CG RAM.		46 μs			
	I / D = 1: Increment I / D = 0: Decrement S = 1: Accompanies display shift S / C = 1: Display shift S / C = 0: Cursor movement R / L = 1: Right shift R / L = 0: Left shift DL = 1: 8 bit DL = 0: 4 bit N = 1: 2 lines N = 0: 1 line F = 1: 5 × 10 dots F = 0: 5 × 7 dots BF = 1: Internal operation in progress BF = 0: Instructions can be received										DD RAM: Display data RAM CG RAM: Character generator RAM A _{CG} : CG RAM address A _{DD} : DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM.		Execution times will vary with frequency.

(Note) * = Invalid

●Character code and corresponding character pattern

Higher 4 bit Lower 4 bit		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (1)		0	G	P	`	P		—	9	E	α	p	
XXXX0001	(2)	.	1	A	Q	a	q	.	7	+	4	a	q	
XXXX0010	(3)	"	2	B	R	b	r	"	4	W	×	p	θ	
XXXX0011	(4)	#	3	C	S	c	s	#	7	+	E	ε	∞	
XXXX0100	(5)	\$	4	D	T	d	t	\$	1	+	+	μ	α	
XXXX0101	(6)	%	5	E	U	e	u	%	+	+	1	ε	0	
XXXX0110	(7)	&	6	F	V	f	v	&	0	+	3	p	Σ	
XXXX0111	(8)	'	7	G	W	g	w	'	+	×	3	g	π	
XXXX1000	(1)	(	8	H	X	h	x	(	0	×	U	r	×	
XXXX1001	(2)	)	9	I	Y	i	y	)	+	7	U	·	γ	
XXXX1010	(3)	*	#	J	Z	j	z	*	3	0	k	j	*	
XXXX1011	(4)	+	#	K	C	k	c	+	+	9	h	×	π	
XXXX1100	(5)	.	<	L	*	l	l	.	3	7	5	+	π	
XXXX1101	(6)	—	=	M	O	m	o	—	3	×	^	+	÷	
XXXX1110	(7)	.	>	N	^	n	÷	.	3	h	+	·	·	
XXXX1111	(8)	/	7	O	_	o	÷	.	W	Y	7	0		

● Reset function

When you turn the power supply on using the internal re-set circuit, the module automatically returns to its initial (reset) settings. At the initial settings, the following instructions are carried out.

(1) Clear display

The busy flag remains in the busy condition ($BF = 1$) until initialization is completed. This takes 15 ms.

(2) Function set

DL = 1: 8-bit interface data length

N = 1

F = 0: 5 × 7 dot matrix

(3) Display on/off control

D = 0: Display off

C = 0: Cursor off

B = 0: Blinking off

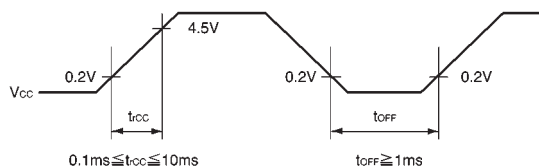
(4) Entry mode set

1/D = 1: +1 (increment)

S = 0: No shift

(5) Select DD RAM

Depending on the power supply's rise and fall times when it is turned on, there may be times when the initialization cannot be completed. Therefore, be aware of the following timing relationship.



t_{OFF} regulates the power supply breaks, or on and off times.

Note) When the above power supply conditions are not met, the internal re-set circuit will not operate properly.