



STSJ2NM60

N-CHANNEL 600V - 2.8Ω - 2A PowerSO-8 Zener-Protected MDmesh™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STSJ2NM60	600 V	< 3.2 Ω	2 A

- TYPICAL R_{DS(on)} = 2.8 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- IMPROVED ESD CAPABILITY
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

DESCRIPTION

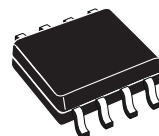
The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

APPLICATIONS

The MDmesh™ family is very suitable for increase the power density of high voltage converters allowing system miniaturization and higher efficiencies.

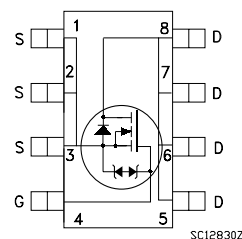
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	2	A
	Drain Current (continuous) at T _A = 25°C (1)	0.37	A
	Drain Current (continuous) at T _C = 100°C	1.26	A
I _{DM} (2)	Drain Current (pulsed)	8	A
P _{TOT}	Total Dissipation at T _C = 25°C	70	W
P _{TOT}	Total Dissipation at T _A = 25°C (1)	3	W
	Derating Factor (1)	0.02	W/°C
dv/dt (3)	Peak Diode Recovery voltage slope	15	V/ns
T _{stg}	Storage Temperature	- 65 to 150	°C
T _j	Max. Operating Junction Temperature		



PowerSO-8

INTERNAL SCHEMATIC DIAGRAM



DRAIN CONTACT ALSO ON THE BACKSIDE

STSJ2NM60

THERMAL DATA

Rthj-c	Thermal Resistance Junction-case Max	1.78	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (1)	42	°C/W
T _j	Max. Operating Junction Temperature	150	°C
T _{stg}	Storage Temperature	– 65 to 150	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	600			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±5	μA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 1 A		2.8	3.2	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (4)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 2 A		1.4		S
C _{iss}	Input Capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		160		pF
C _{oss}	Output Capacitance			67		pF
C _{rss}	Reverse Transfer Capacitance			4		pF
R _G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3.5		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 300\text{ V}$, $I_D = 1\text{ A}$		13		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		8		ns
Q_g	Total Gate Charge	$V_{DD} = 480\text{ V}$, $I_D = 2\text{ A}$,		6	8.4	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		1.8		nC
Q_{gd}	Gate-Drain Charge			3.3		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-Voltage Rise Time	$V_{DD} = 480\text{ V}$, $I_D = 2\text{ A}$,		12		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$		25		ns
t_c	Cross-Over Time	(see test circuit, Figure 3)		30		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				2	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				8	A
$V_{SD(4)}$	Forward On Voltage	$I_{SD} = 2\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 2$, $di/dt = 100\text{ A}/\mu\text{s}$,		516		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100\text{ V}$, $T_j = 25^\circ\text{C}$		516		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		2		A
t_{rr}	Reverse Recovery Time	$I_{SD} = 2$, $di/dt = 100\text{ A}/\mu\text{s}$,		808		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 100\text{ V}$, $T_j = 150^\circ\text{C}$		890		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		2.2		A

Note: 1. When mounted on 1inch² FR4 Board, 2oz of Cu, $t \leq 10\text{ sec}$.

2. Pulse width limited by safe operating area

3. $I_{SD} < 3.3\text{ A}$, $di/dt < 400\text{ A}/\mu\text{s}$, $V_{DD} < V_{(BR)DSS}$, $T_j < T_{jMAX}$

4. Pulsed: Pulse duration = 400 μs , duty cycle 1.5 %

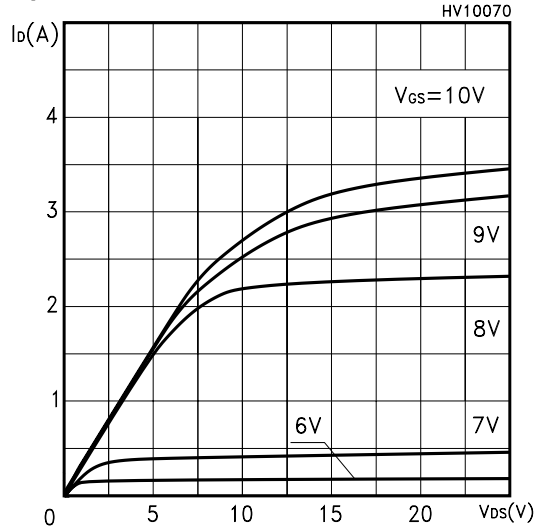
GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{ mA}$ (Open Drain)	30			V

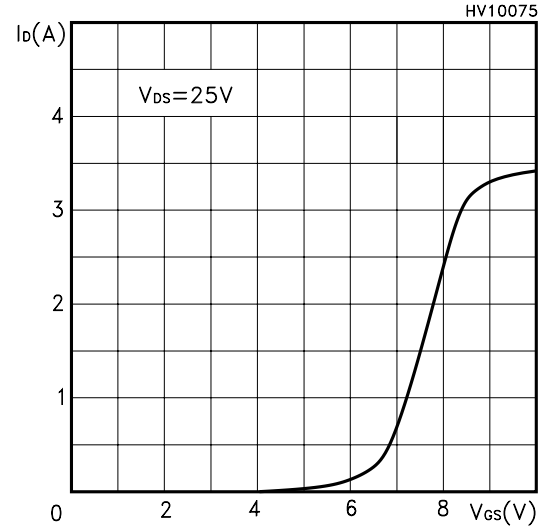
PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

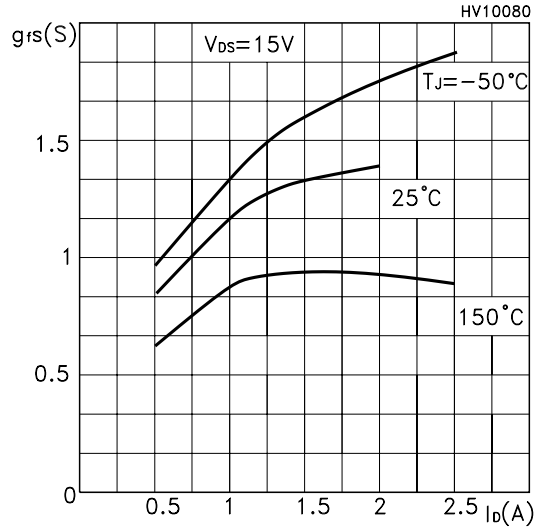
Output Characteristics



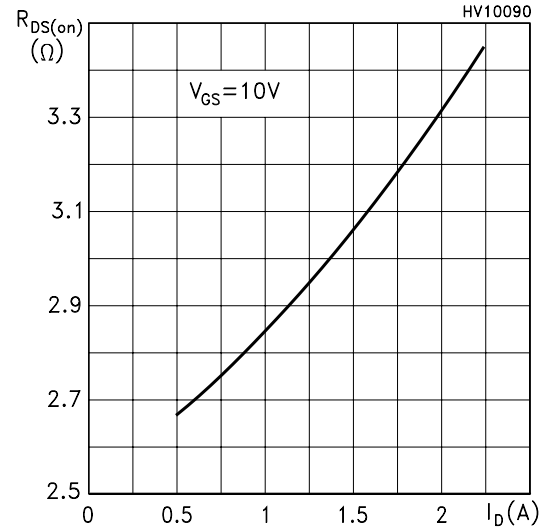
Transfer Characteristics



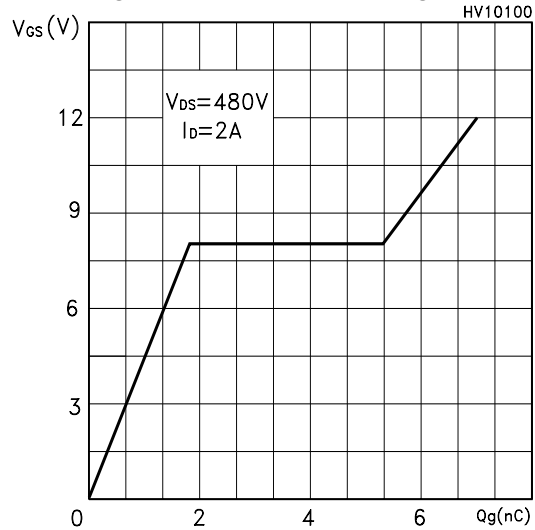
Transconductance



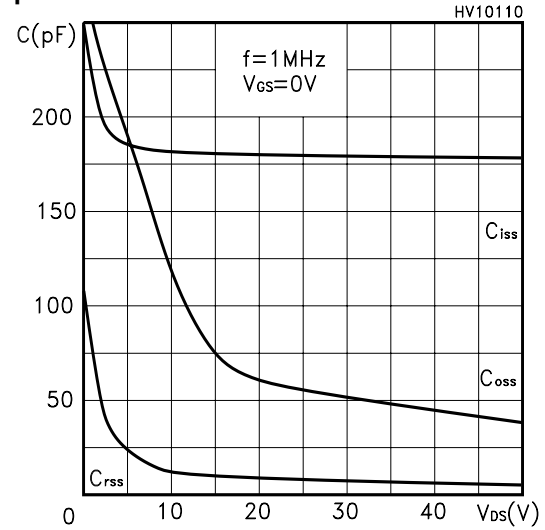
Static Drain-source On Resistance



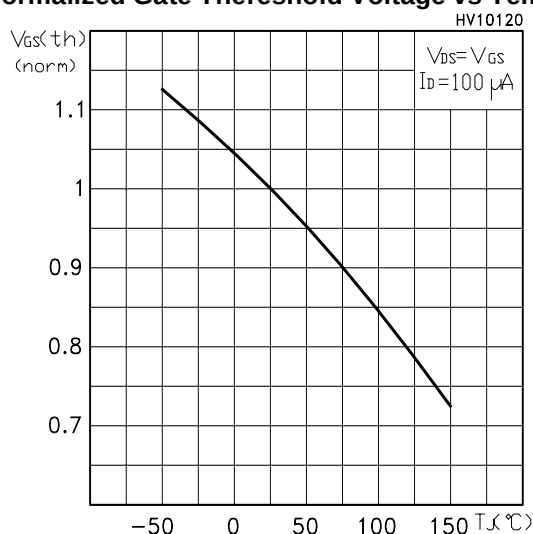
Gate Charge vs Gate-source Voltage



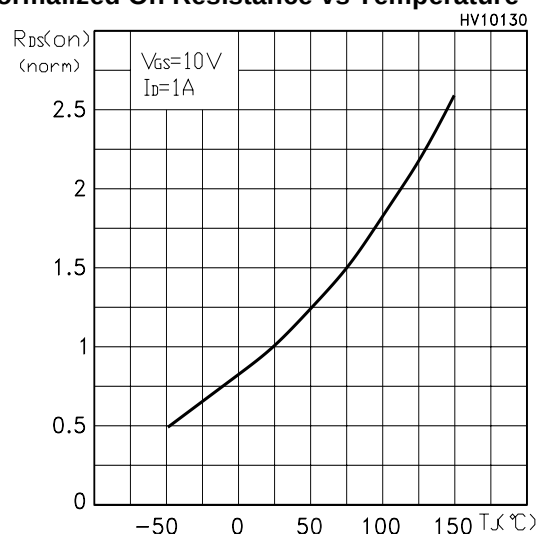
Capacitance Variations



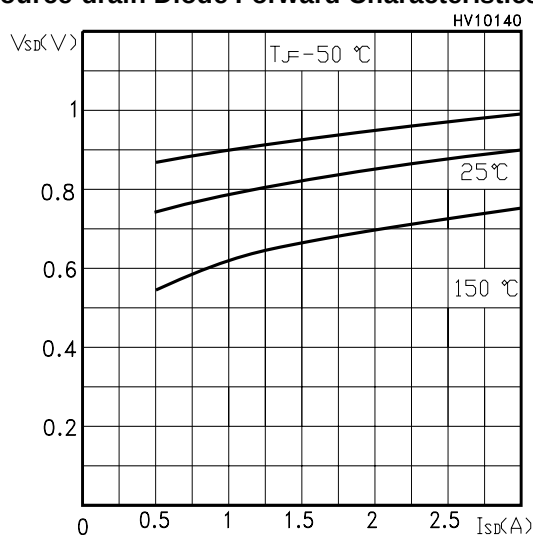
Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized BVDSS vs. Temperature

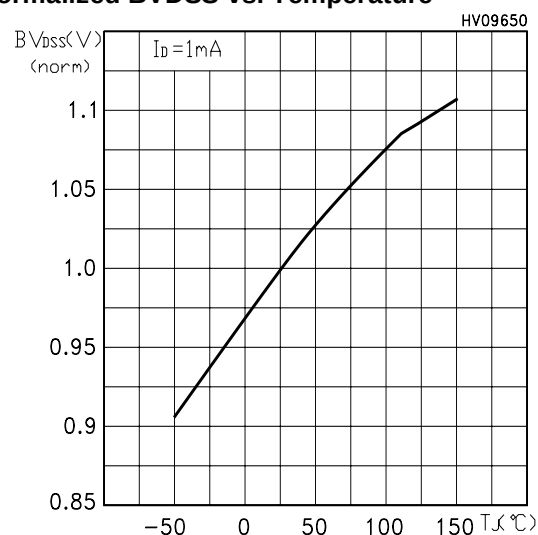


Fig. 1: Unclamped Inductive Load Test Circuit

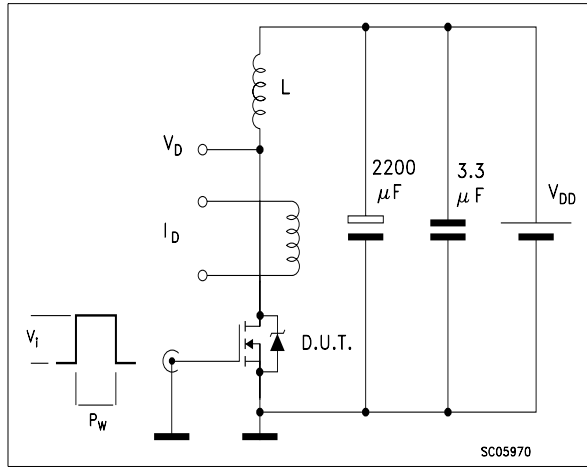


Fig. 2: Unclamped Inductive Waveform

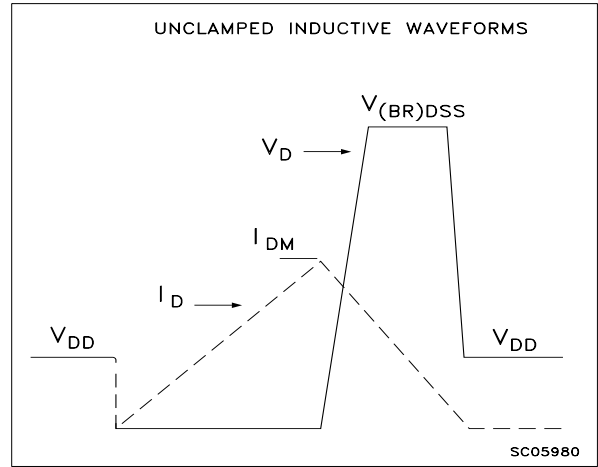


Fig. 3: Switching Times Test Circuit For Resistive Load

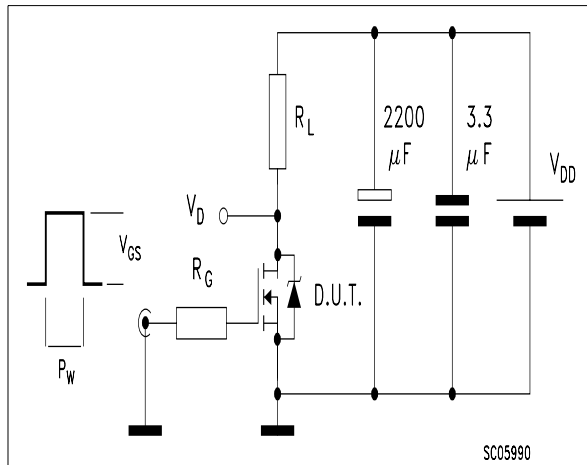


Fig. 4: Gate Charge test Circuit

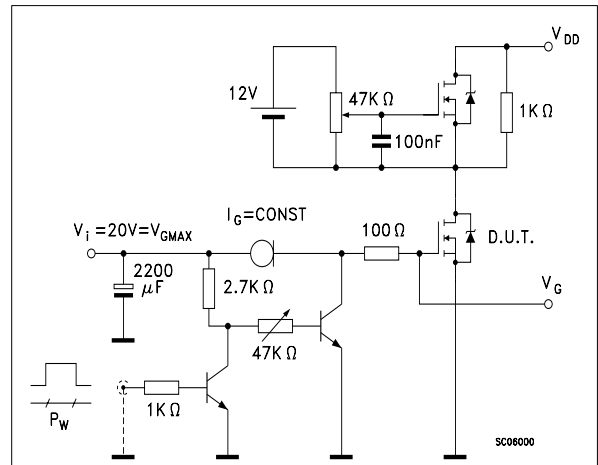
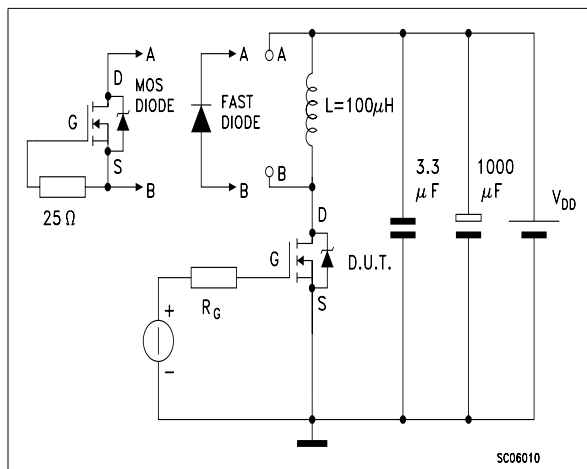
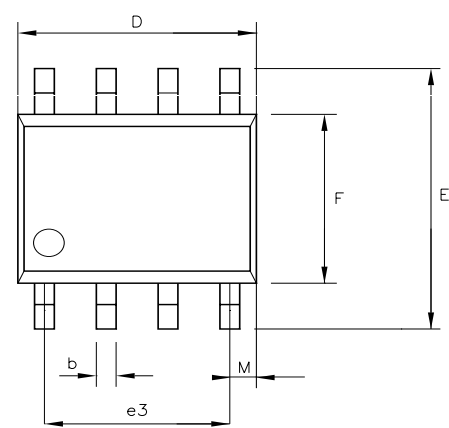


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

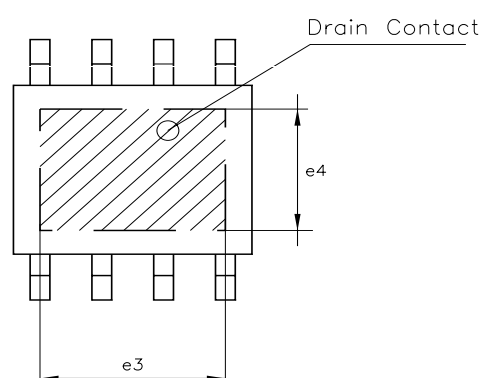


PowerSO-8™ MECHANICAL DATA

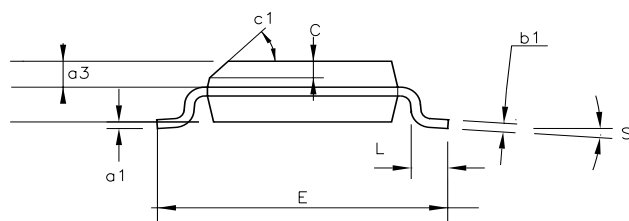
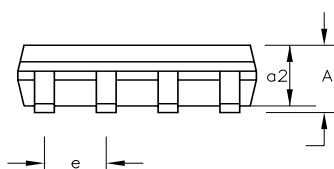
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45° (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
e4		2.79			0.110	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8° (max.)					



(Top View)



(Bottom View)



Powerso-8

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>