

Monolithic N-Channel JFET Dual

PRODUCT SUMMARY

$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
-1 to -6	-25	4.5	-1	20

FEATURES

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 90 dB

BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- High-Speed Performance
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

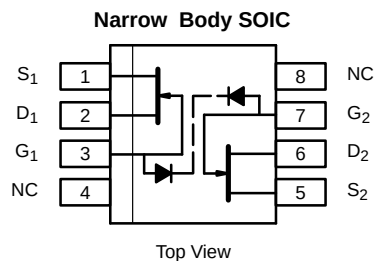
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

DESCRIPTION

The SST441 is a monolithic high-speed dual JFET mounted in a single SO-8 package. This JFET is an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

The SO-8 package is available with tape-and-reel options to support automated assembly (see Packaging Information).

For similar products in TO-71 packaging, see the U441 data sheet.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage -25 V
 Gate Current 50 mA
 Lead Temperature ($1/16$ " from case for 10 sec.) 300°C
 Storage Temperature -55 to 150°C

Operating Junction Temperature -55 to 150°C
 Power Dissipation : Per Side^a 300 mW
 Total^a 500 mW

Notes

a. Derate 2.4 mW/°C above 25°C

Applications information may also be obtained via FaxBack, request document #70595.

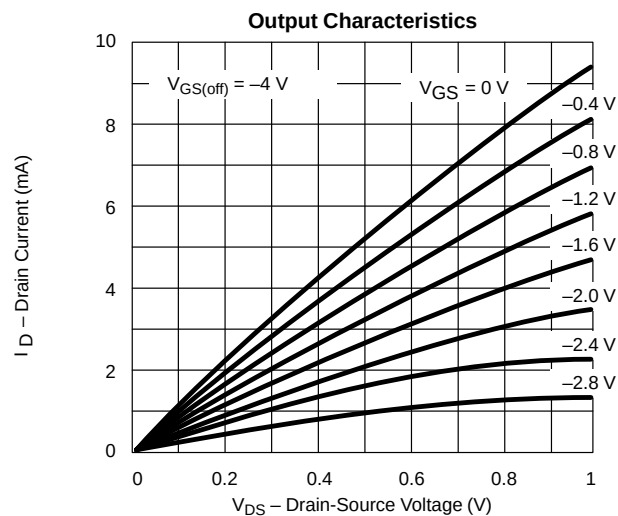
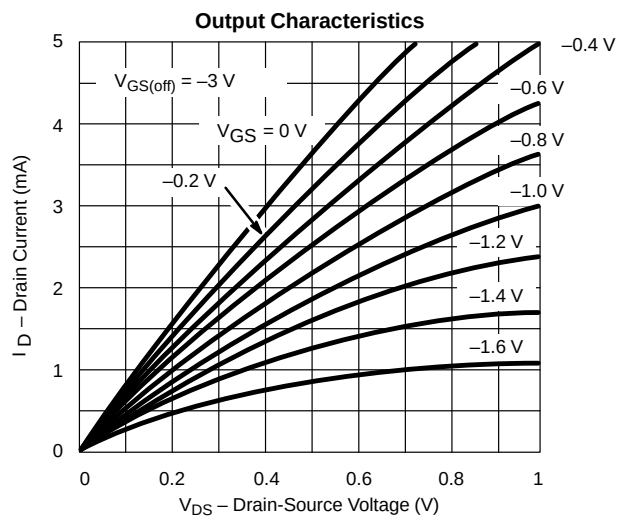
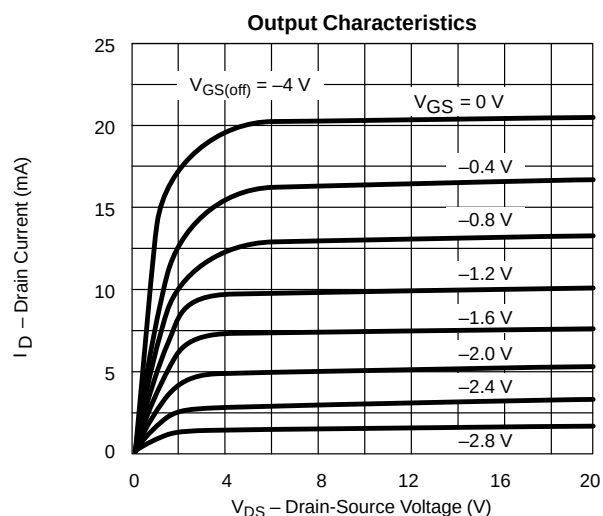
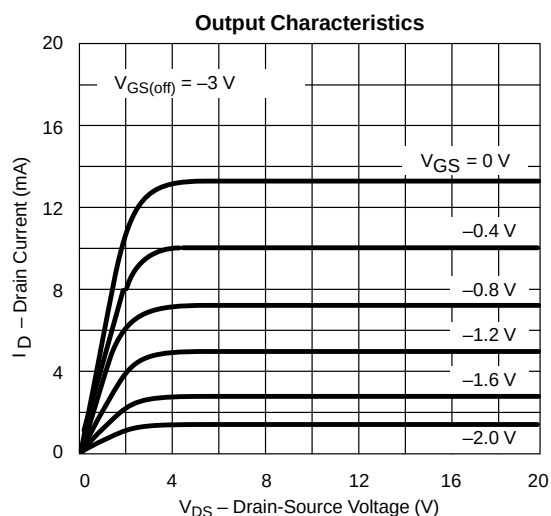
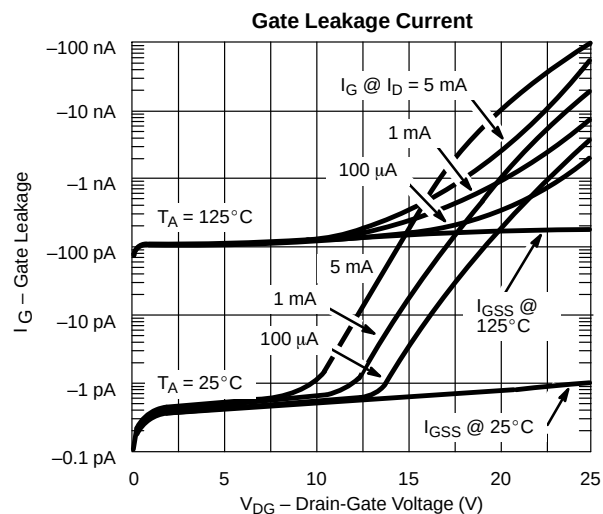
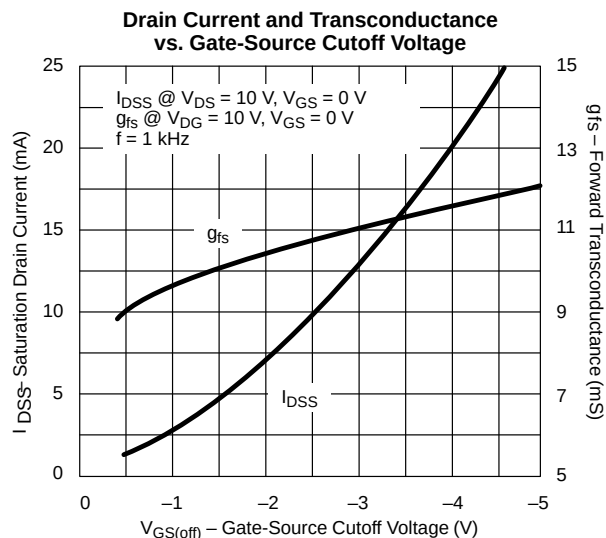


SPECIFICATIONS ^a						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ ^b	Max	
Static						
Gate-Source Breakdown Voltage	V _{(BR)GSS}	I _G = −1 μA, V _{DS} = 0 V	−25	−35		V
Gate-Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 nA	−1	−3.5	−6	
Saturation Drain Current ^c	I _{DSS}	V _{DS} = 10 V, V _{GS} = 0 V	6	15	30	mA
Gate Reverse Current	I _{GSS}	V _{GS} = −15 V, V _{DS} = 0 V		−1	−500	pA
		T _A = 125°C		−0.2		nA
Gate Operating Current	I _G	V _{DG} = 10 V, I _D = 5 mA		−1	−500	pA
		T _A = 125°C		−0.2		nA
Gate-Source Forward Voltage	V _{GS(F)}	I _G = 1 mA , V _{DS} = 0 V		0.7		V
Dynamic						
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 5 mA f = 1 kHz	4.5	6	9	mS
Common-Source Output Conductance	g _{os}			20	200	μS
Common-Source Forward Transconductance	g _{fs}	V _{DS} = 10 V, I _D = 5 mA f = 100 MHz		5.5		mS
Common-Source Output Conductance	g _{os}			30		μS
Common-Source Input Capacitance	C _{iss}	V _{DS} = 10 V, I _D = 5 mA f = 1 MHz		3.5		pF
Common-Source Reverse Transfer Capacitance	C _{rss}			1		
Equivalent Input Noise Voltage	e _n	V _{DS} = 10 V, I _D = 5 mA f = 10 kHz		4		nV/ √Hz
Matching						
Differential Gate-Source Voltage	V _{GS1} − V _{GS2}	V _{DG} = 10 V, I _D = 5 mA		7	20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	V _{DG} = 10 V, I _D = 5 mA T _A = −55 to 125°C		10		μV/°C
Saturation Drain Current Ratio ^d	$\frac{I_{DSS1}}{I_{DSS2}}$	V _{DS} = 10 V, V _{GS} = 0 V		0.98		
Transconductance Ratio ^d	$\frac{g_{fs1}}{g_{fs2}}$	V _{DS} = 10 V, I _D = 5 mA f = 1 kHz		0.98		
Common Mode Rejection Ratio	CMRR	V _{DG} = 10 to 15 V, I _D = 5 mA		90		dB

Notes

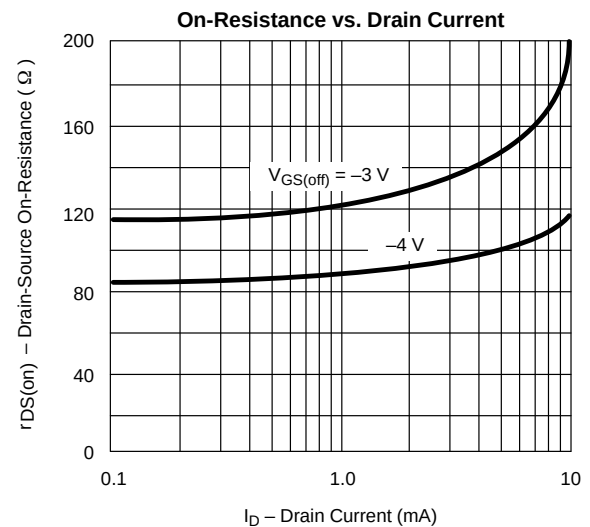
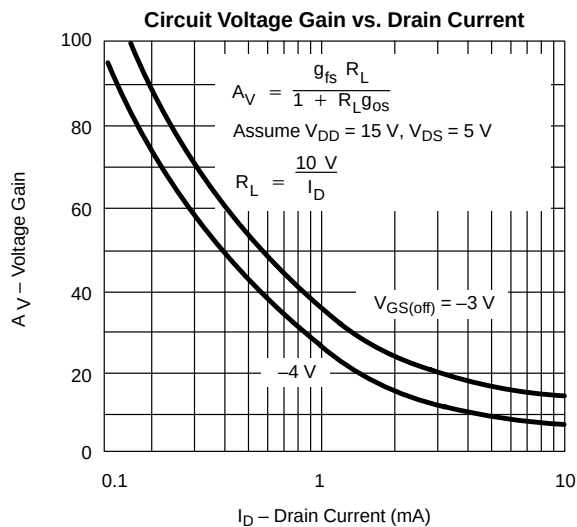
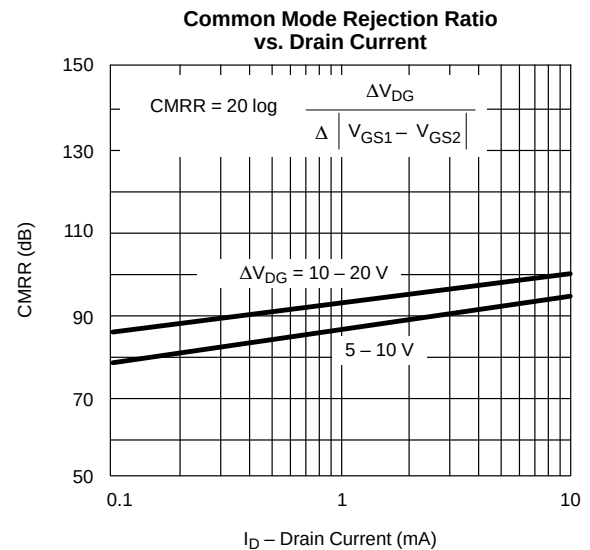
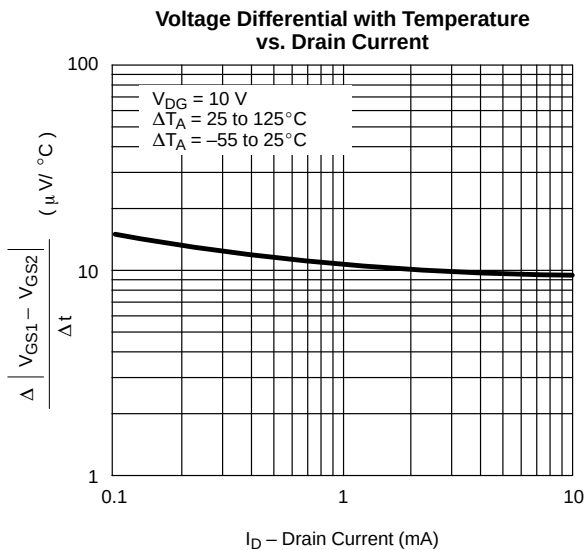
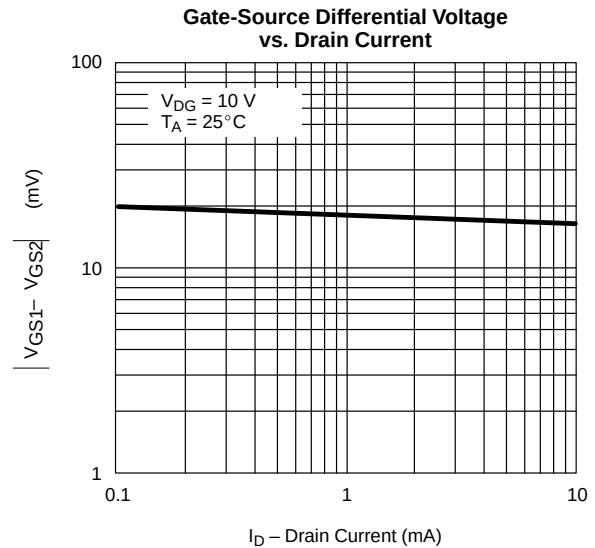
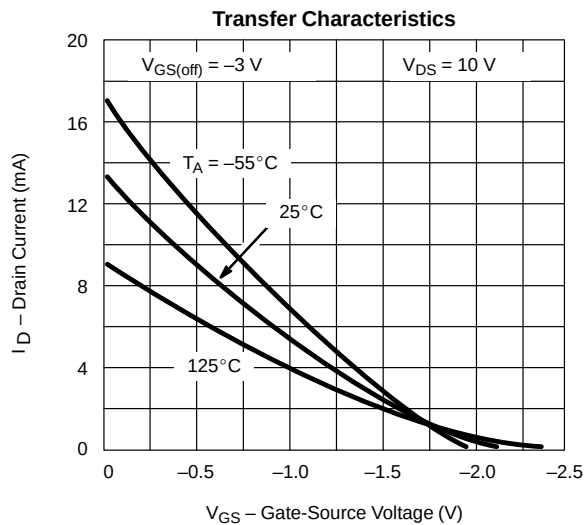
- a. $T_A = 25^\circ C$ unless otherwise noted.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.
d. Assumes smaller value in the numerator.

NNZ

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)




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