HN62W5016N Series

524288-word × 32-bit/1048576-word × 16-bit CMOS MASK Programmable ROM

HITACHI

Preliminary

Description

The HN62W5016N is a 16-Mbit CMOS mask-programmable ROM organized either as 524,288-word by 32-bit or as 1,048,576-word by 16-bit. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns is the most suitable to the system using a high speed micro-computer by 32-bit.

Features

- Low voltage operation: 3.3 V ± 0.3 V
- High Speed
  Normal access time: 120 ns/150 ns (max)
  Page access time: 40 ns/50 ns (max)
- Low power consumption
  Active: 360 mW (max)
  Standby: 0.72 mW (max)
  Power down mode: 36 µW (max)
- Double word-wide or word-wide data organization with DW/W
- 4 double-word page access on double word-wide mode
- 8 word page access on word-wide mode
- Three-state data output for or-tying
- LVTTL compatible

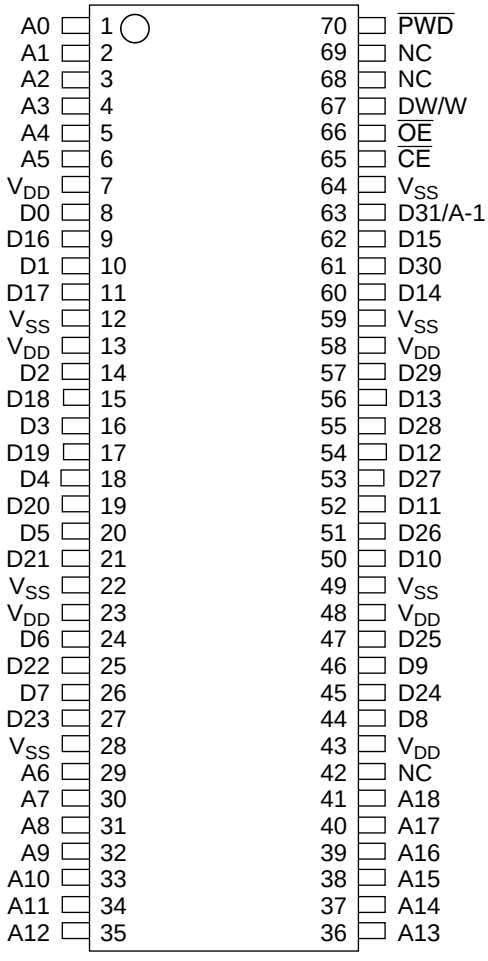
Ordering Information

Type No.	Access Time	Package
HN62W5016NF-12	120 ns	70 pin plastic SSOP (FP-70DS)
HN62W5016NF-15	150 ns	

Note: The specifications of this device are subject to change without notice. Please contact your hearest Hitachi's Sales Dept. regarding specifications.

Pin Arrangement

HN62W5016NF

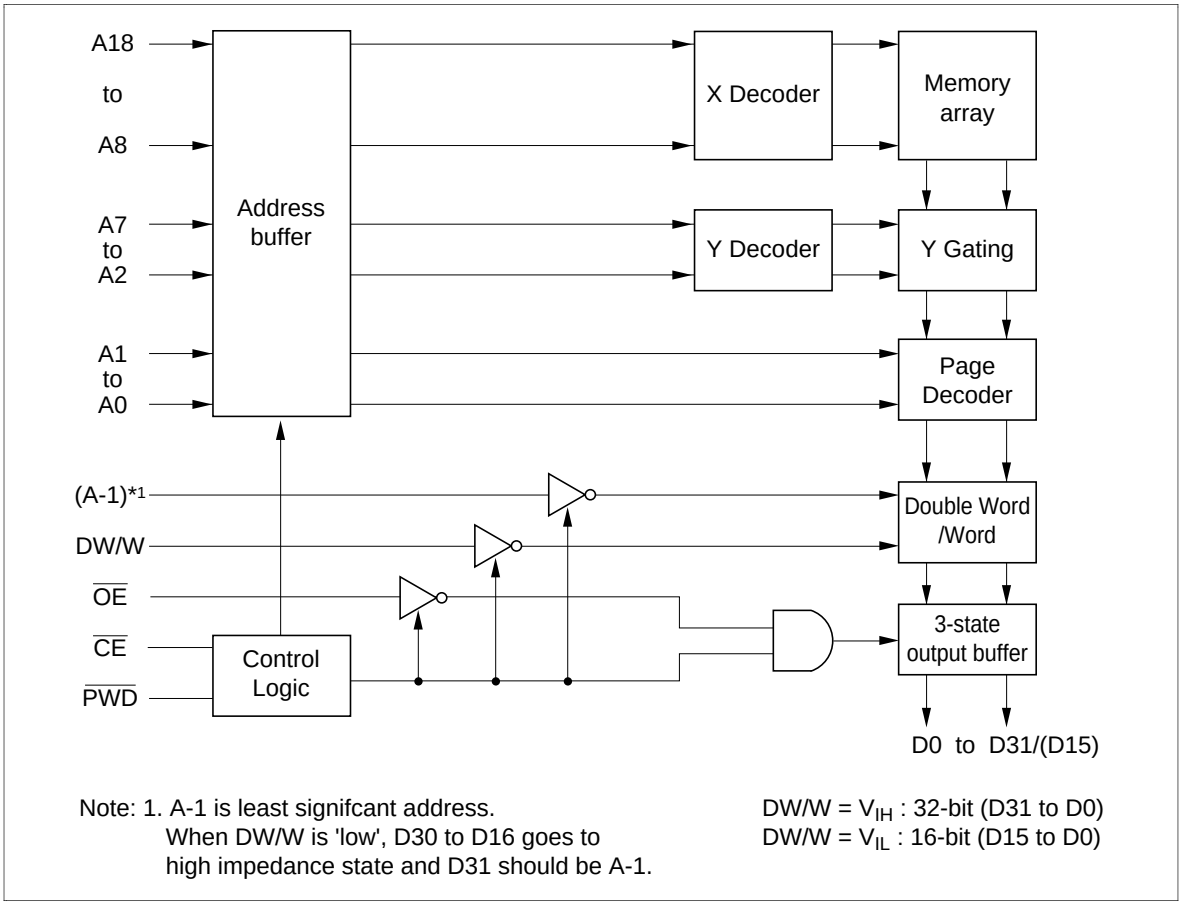


(Top view)

Pin Description

Pin name	Function
A2 to A18	Address inputs
A-1, A0 to A1	Page address inputs
D0 to D31	Data output
DW/W	32/16 bit (Double word/word) mode switch inputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PWD}$	Power down input
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



Note: 1. A-1 is least signifcant address.
When DW/W is 'low', D30 to D16 goes to high impedance state and D31 should be A-1.

DW/W = V_{IH} : 32-bit (D31 to D0)
DW/W = V_{IL} : 16-bit (D15 to D0)

Mode Selection

	Pin					Data output		Address input	
Mode	**$\overline{PWD}$**	**$\overline{CE}$**	**$\overline{OE}$**	**DW/W**	**D31/A-1**	**D0–D15**	**D16–D31**	**LSB**	**MSB**
Power down	L	×*1	×	×	×	High-Z*2	High-Z	—	—
Standby	H	H	×	×	×	High-Z	High-Z	—	—
Output disable	H	L	H	×	×	High-Z	High-Z	—	—
Read (32-bit)	H	L	L	H	Dout	D0 to D15	D16 to D31	A0	A18
Read (16-bit)	H	L	L	L	L	D0 to D15	High-Z	A-1	A18
Read (16-bit)	H	L	L	L	H	D16 to D31	High-Z	A-1	A18

Notes: 1. ×: Don't care.
2. High-Z: High impedance.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and outpu tvoltage	Vin, Vout	–0.3 to V_{DD} + 0.3	V	1
Operating temperatue range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Operating power supply current	I_{DD}	—	100	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = min
Standby power supply current	I_{SB1}	—	200	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD} - 0.2$ V
	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq 2.2$ V
Power down supply current	I_{PWD}	—	10	µA	V_{DD} = 3.6 V, $\overline{PWD} \leq 0.2$ V
Input leakage current	$\|I_{IL}\|$	—	10	µA	V_{IN} = 0 to V_{DD}
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{DD}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –2 mA
	V_{OL}	—	0.4	V	I_{OL} = 2 mA

Capacitance (V_{DD} = 3.3 ±0.3 V, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D31/A-1 pin is output.

AC Characteristics (V_{DD} = 3.3 ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

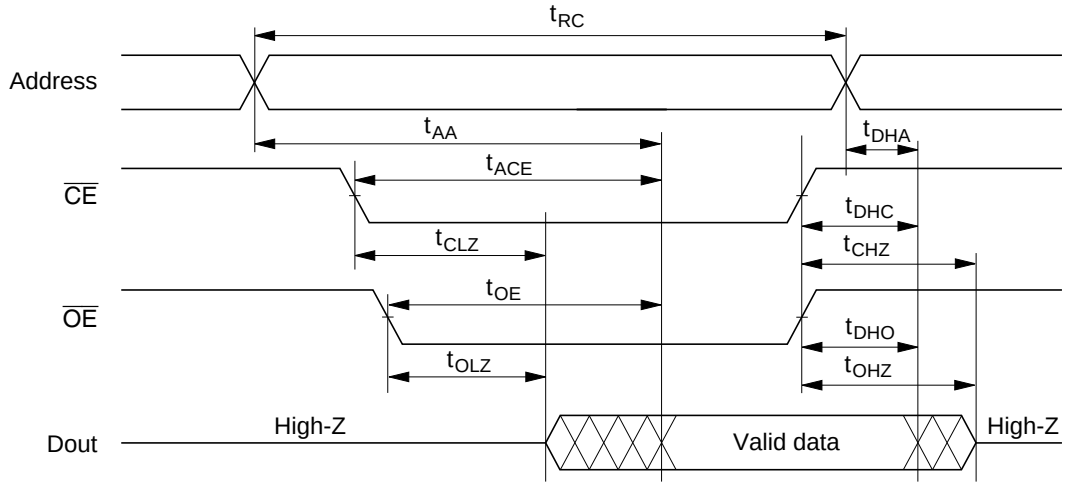
- Output load: 1TTL + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5 ns

		HN62W5016N-12		HN62W5016N-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Page read cycle time	t_{PC}	40	—	50	—	ns	
Address access	t_{AA}	—	120	—	150	ns	
Page access time	t_{PA}	—	40	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
DW/W access time	t_{DWW}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from DW/W	t_{DHD}	0	—	0	—	ns	
Output hold time from $\overline{PWD}$	t_{DHP}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	40	—	50	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	40	—	50	ns	1
DW/W to output in high-Z	t_{DHZ}	—	40	—	50	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
DW/W to output in low-Z	t_{DLZ}	5	—	5	—	ns	
Recovery time from $\overline{PWD}$	t_R	10	—	10	—	µs	

Note: 1. t_{CHZ}, t_{OHZ} and t_{DHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

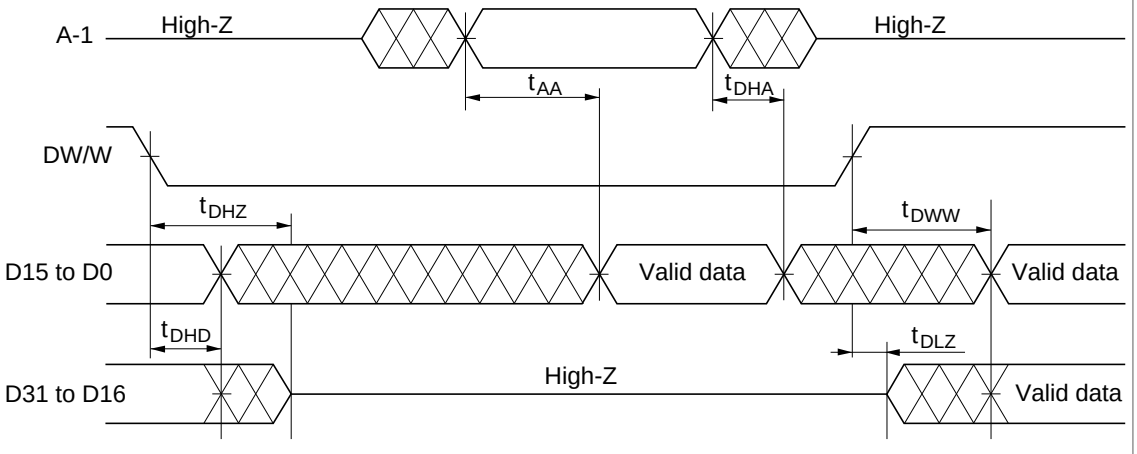
Timing Waveforms

Double Word Mode (DW/W = 'V_{IH}') **or Word Mode** (DW/W = 'V_{IL}')



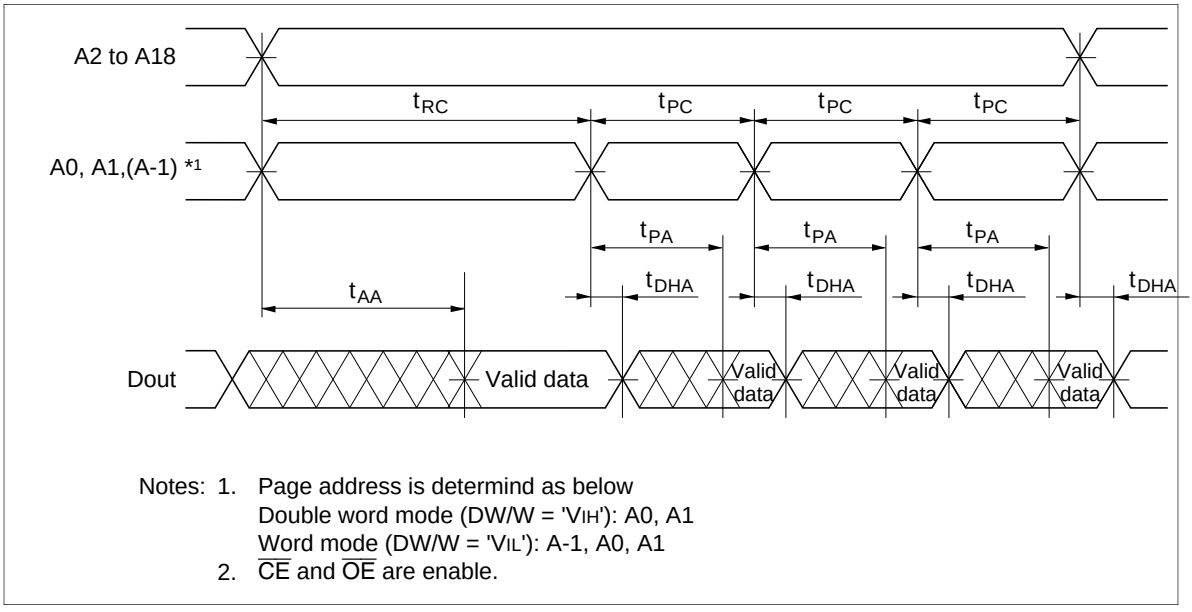
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Double Word Mode, Word Mode Switch



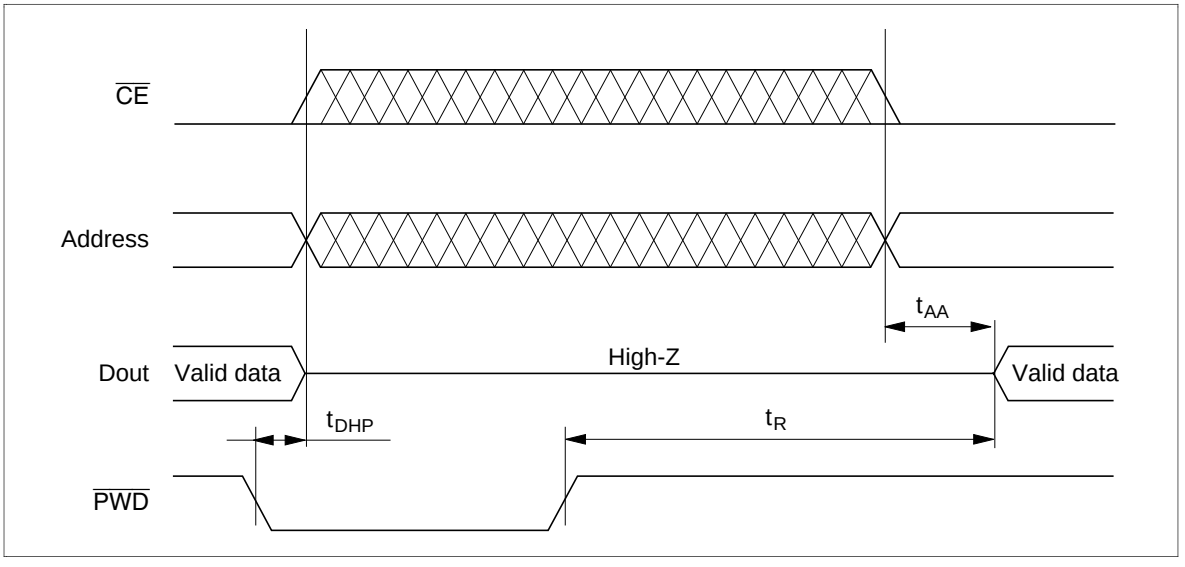
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A18 to A0 are valid.
2. D31/A-1 pin is in the output state when DW/W is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page Mode

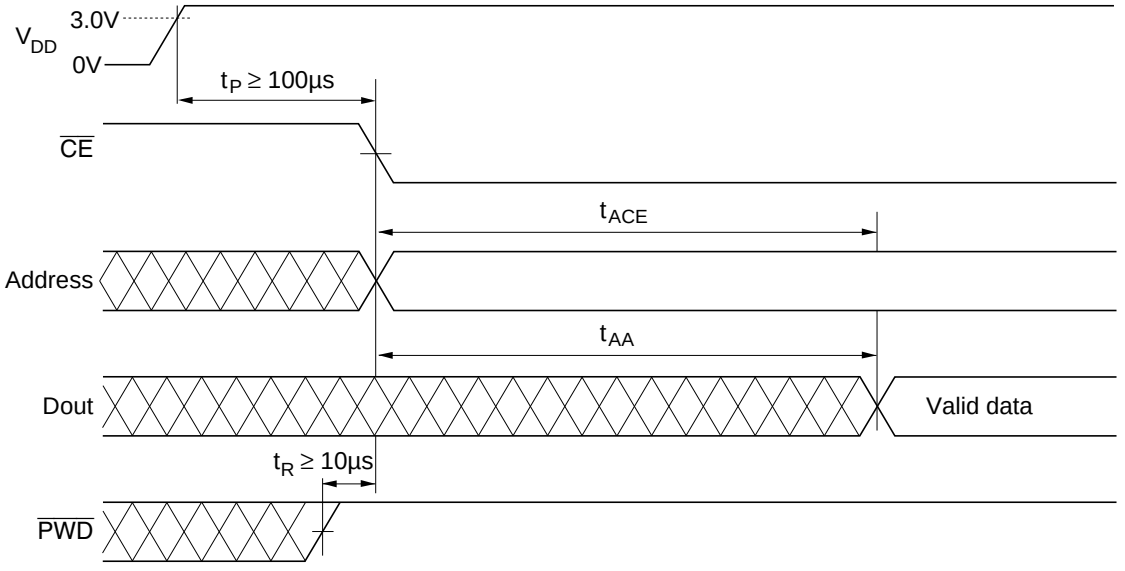


Notes: 1. Page address is determind as below
Double word mode (DW/W = 'V_{IH}'): A0, A1
Word mode (DW/W = 'V_{IL}'): A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are enable.

Power Down Mode



Power Up Sequence



Notes: 1. This device is used ATD(Address Transition Detector). Therefore, transfer either $\overline{CE}$ or address(A18 to A2) after power up to 3.0 V.
2. t_P, t_R: Determined by slower.

Package Dimensions

HN62W5016NF Series (FP-70DS) Unit: mm