
HM628128B Series

131,072-word $\times$ 8-bit High speed CMOS Static RAM

HITACHI

ADE-203-243B (Z)

Rev. 2.0

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Description

The Hitachi HM628128B is a CMOS static RAM organized 131,072-word $\times$ 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μ m Hi-CMOS shrink process technology. It offers low power standby power dissipation, therefore, it is suitable for battery backup systems. The device, packaged in a 525 mil SOP or a 8 mm $\times$ 20 mm TSOP or a 600 mil plastic DIP is available.

Features

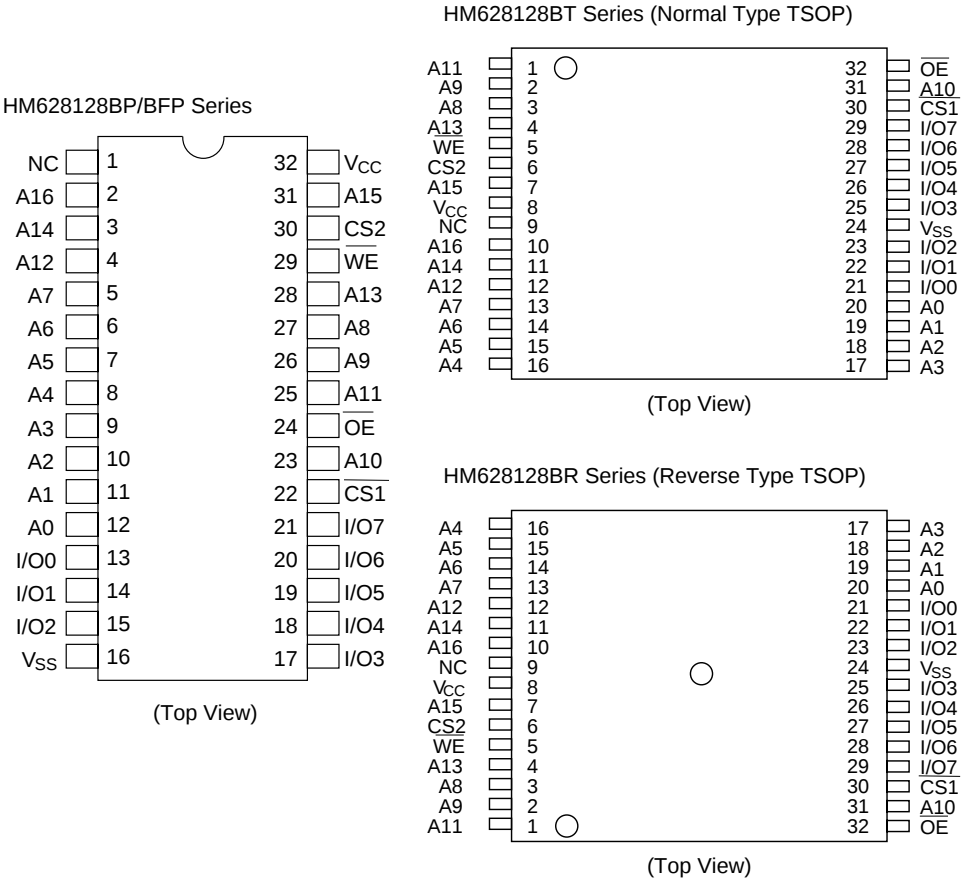
- High speed
 - Fast access time: 70/85ns (max)
- Low power
 - Standby: 10 μ W (typ) (L/L-SL version)
 - Operation: 50 mW/MHz (typ)
- Single 5 V supply
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Capability of battery backup operation (L/L-SL version)
 - 2 chip selection for battery backup

HM628128B Series

Ordering Information

Type No.	Access Time	Data Retention Current	Package
HM628128BLP-7	70 ns	50 μ A	600-mil 32-pin plastic DIP (DP-32)
HM628128BLP-8	85 ns	50 μ A	
HM628128BLP-7SL	70 ns	15 μ A	
HM628128BLP-8SL	85 ns	15 μ A	
HM628128BLFP-7	70 ns	50 μ A	525-mil 32-pin plastic SOP (FP-32D)
HM628128BLFP-8	85 ns	50 μ A	
HM628128BLFP-7SL	70 ns	15 μ A	
HM628128BLFP-8SL	85 ns	15 μ A	
HM628128BLT-7	70 ns	50 μ A	Normal-bend type 32-pin plastic 8 mm $\times$ 20 mm TSOP (TFP-32D)
HM628128BLT-8	85 ns	50 μ A	
HM628128BLT-7SL	70 ns	15 μ A	
HM628128BLT-8SL	85 ns	15 μ A	
HM628128BLR-7	70 ns	50 μ A	Reverse-bend type 32-pin plastic 8 mm $\times$ 20 mm TSOP (TFP-32DR)
HM628128BLR-8	85 ns	50 μ A	
HM628128BLR-7SL	70 ns	15 μ A	
HM628128BLR-8SL	85 ns	15 μ A	

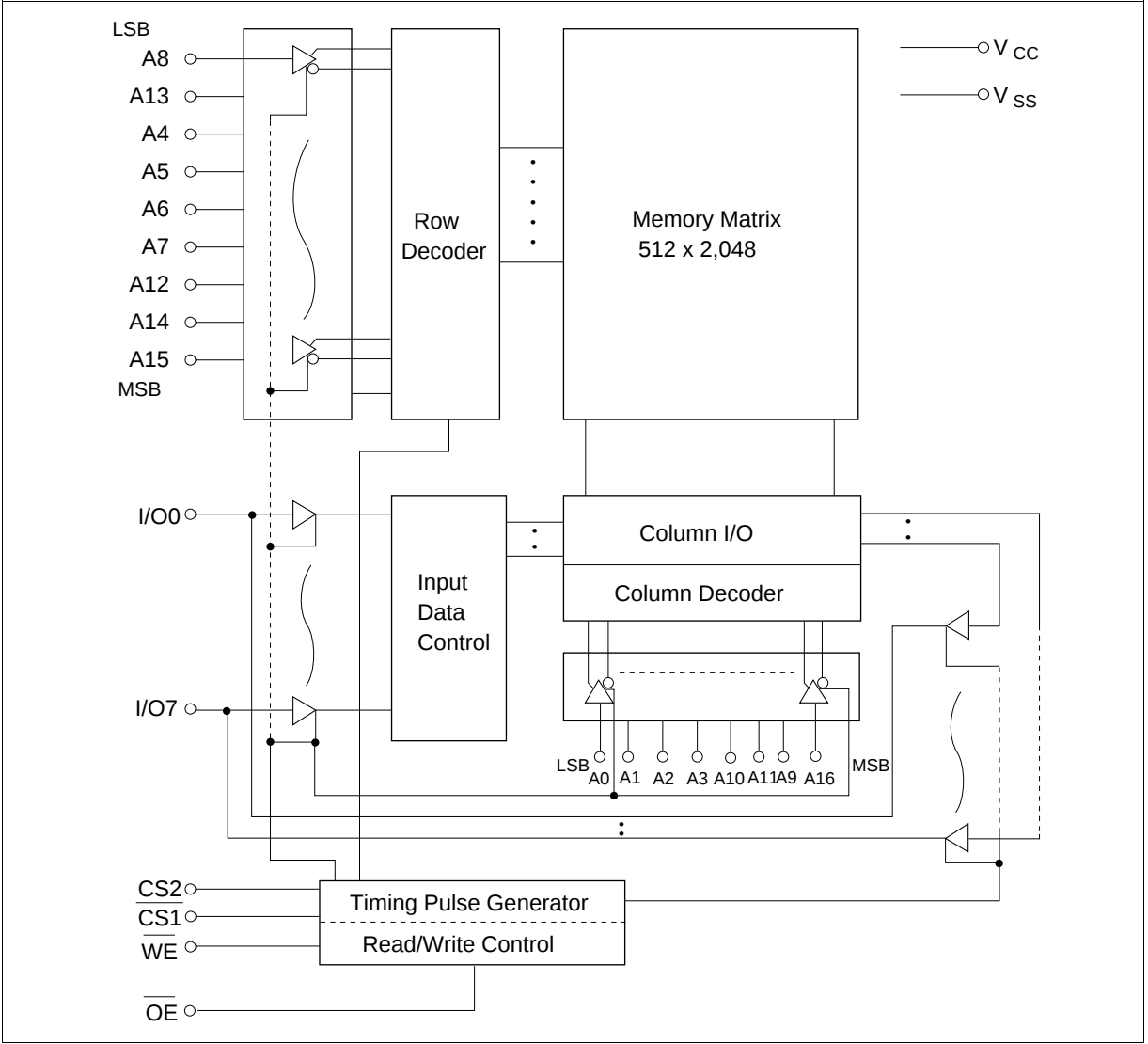
Pin Arrangement



Pin Description

Pin Name	Function
A0 - A16	Address
I/O0 - I/O7	Input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V _{cc}	Power supply
V _{ss}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	-0.5 ^{*1} to $V_{CC} + 0.3$ ^{*2}	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Notes: 1. -3.0 V for pulse half-width ≤ 30 ns

2. Maximum voltage is 7.0 V.

Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
X	X	L	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage (logic 1)	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage (logic 0)	V_{IL}	-0.3 ^{*1}	—	0.8	V

Note: 1. -3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
Input leakage current	I _{Li}	—	—	1	μA	Vin = V _{SS} to V _{CC}
Output leakage current	I _{Lo}	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current : DC	I _{CC}	—	15	25	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V _{IH} /V _{IL} , I _{I/O} = 0mA
Operating power supply current	I _{CC1}	—	35	70	mA	Min.cycle, duty = 100 %, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
	I _{CC2}	—	10	20	mA	Cycle time = 1 μs, duty = 100 % I _{I/O} = 0 mA, $\overline{CS1} \leq 0.2$ V $CS2 \geq V_{CC} - 0.2$ V, Others = V _{IH} /V _{IL} V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby V _{CC} current : DC	I _{SB}	—	1	2	mA	$CS2 = V_{IL}$ or $CS2 = V_{IH}$, $\overline{CS1} = V_{IH}$
Standby V _{CC} current (1): DC	I _{SB1}	—	2 ^{*2}	100 ^{*2}	μA	0V ≤ Vin ≤ V _{CC} , (1) 0 V ≤ CS2 ≤ 0.2V or (2) CS2 ≥ V _{CC} - 0.2V , CS1 ≥ V _{CC} - 0.2V
		—	2 ^{*3}	50 ^{*3}	μA	
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. For L-version
3. For L-SL version

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin ^{*1}	—	—	8	pF	Vin = 0 V
Input/output capacitance	C _{I/O} ^{*1}	—	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100 % tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, unless otherwise noted.)

Test Conditions

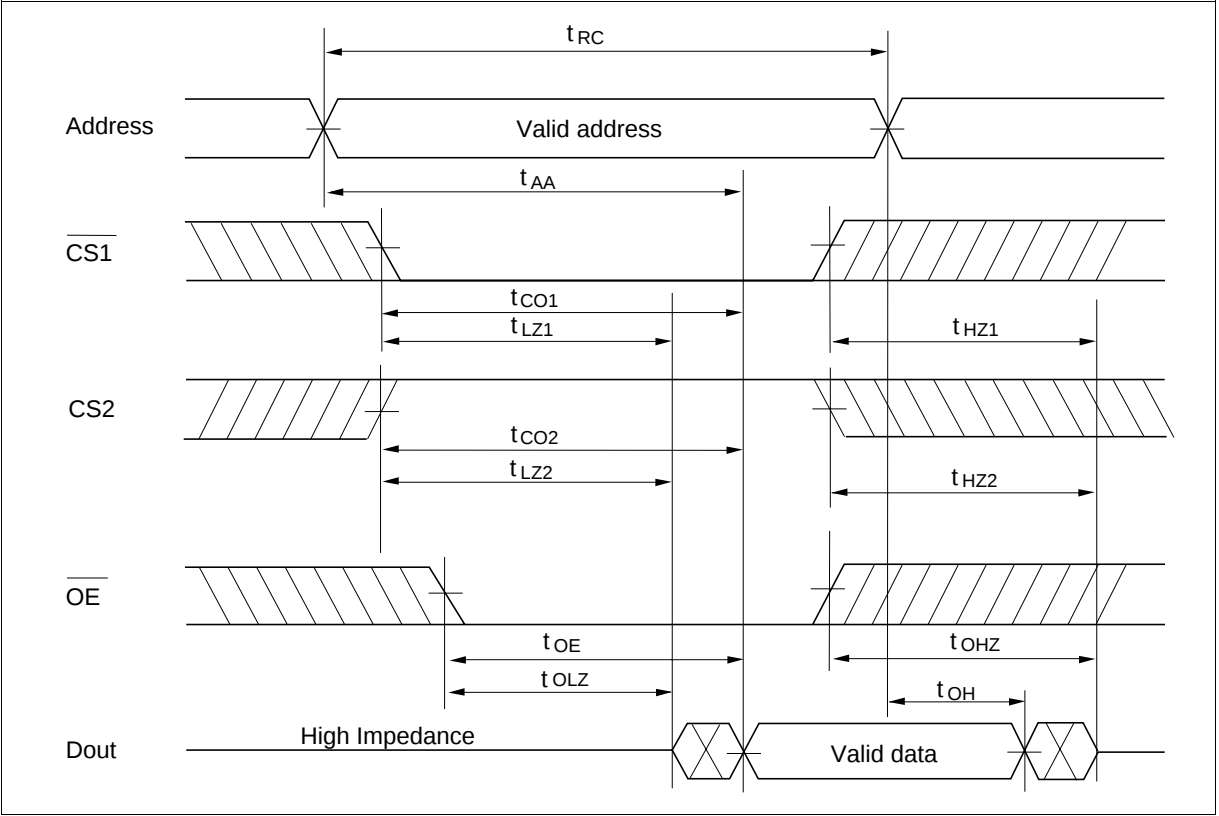
- Input pulse levels : 0.8 V to 2.4 V
- Input rise and fall time : 5 ns
- Input and output timing reference levels : 1.5 V
- Output load : 1 TTL Gate and C_L (100 pF) (Including scope and jig)

Read Cycle

		HM628128B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	70	—	85	—	ns	
Address access time	t _{AA}	—	70	—	85	ns	
Chip selection to output valid	t _{CO1}	—	70	—	85	ns	
	t _{CO2}	—	70	—	85	ns	
Output enable to output valid	t _{OE}	—	35	—	45	ns	
Chip selection to output in low-Z	t _{LZ1}	10	—	10	—	ns	2, 3
	t _{LZ2}	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t _{HZ1}	0	25	0	30	ns	1, 2, 3
	t _{HZ2}	0	25	0	30	ns	1, 2, 3
Output disable to output in high-Z	t _{OHZ}	0	25	0	30	ns	1, 2, 3
Output hold from address change	t _{OH}	10	—	10	—	ns	

- Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device to device.
3. This parameter is sampled and not 100% tested.

Read Cycle Timing ($\overline{WE} = V_{IH}$)

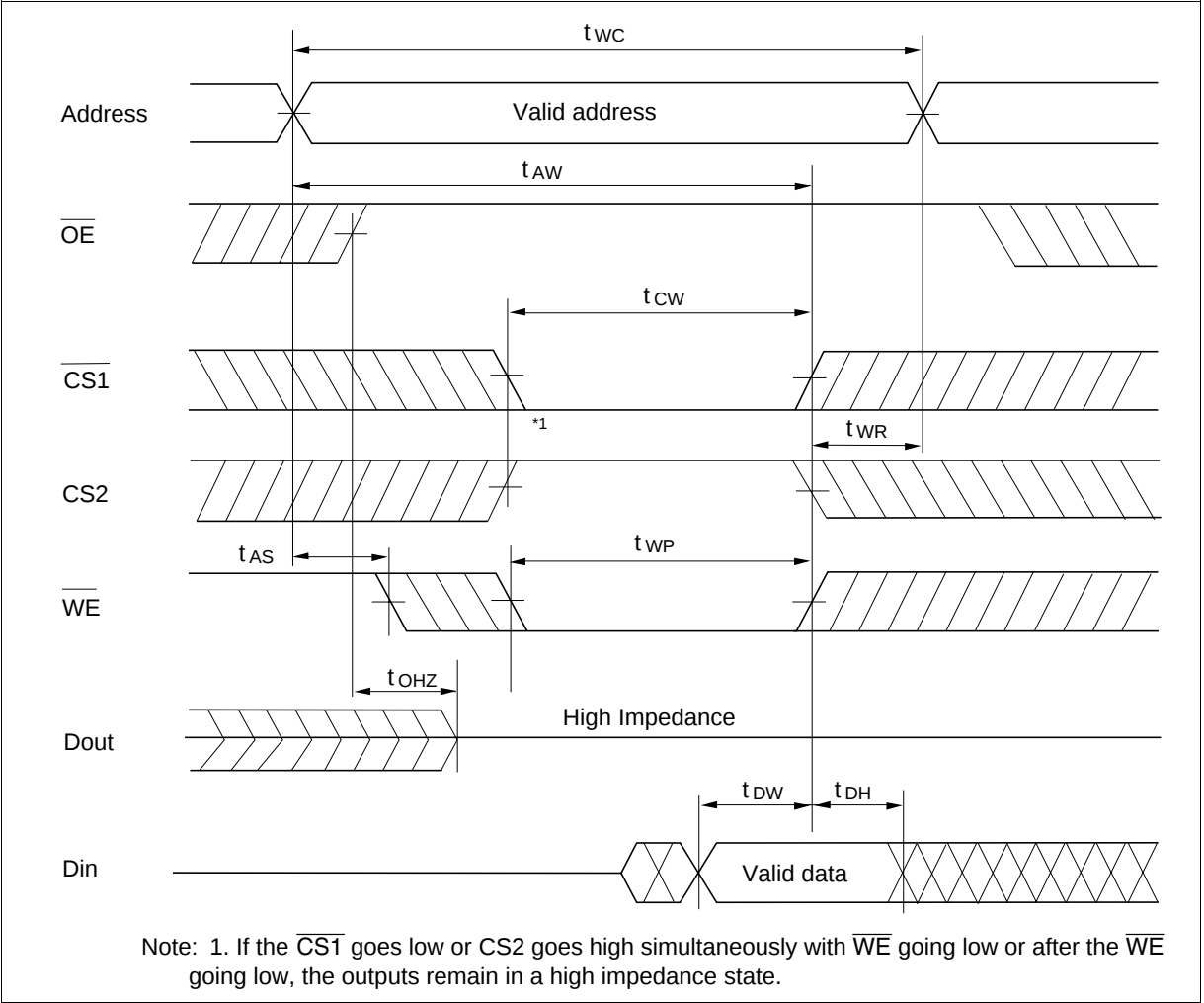


Write Cycle

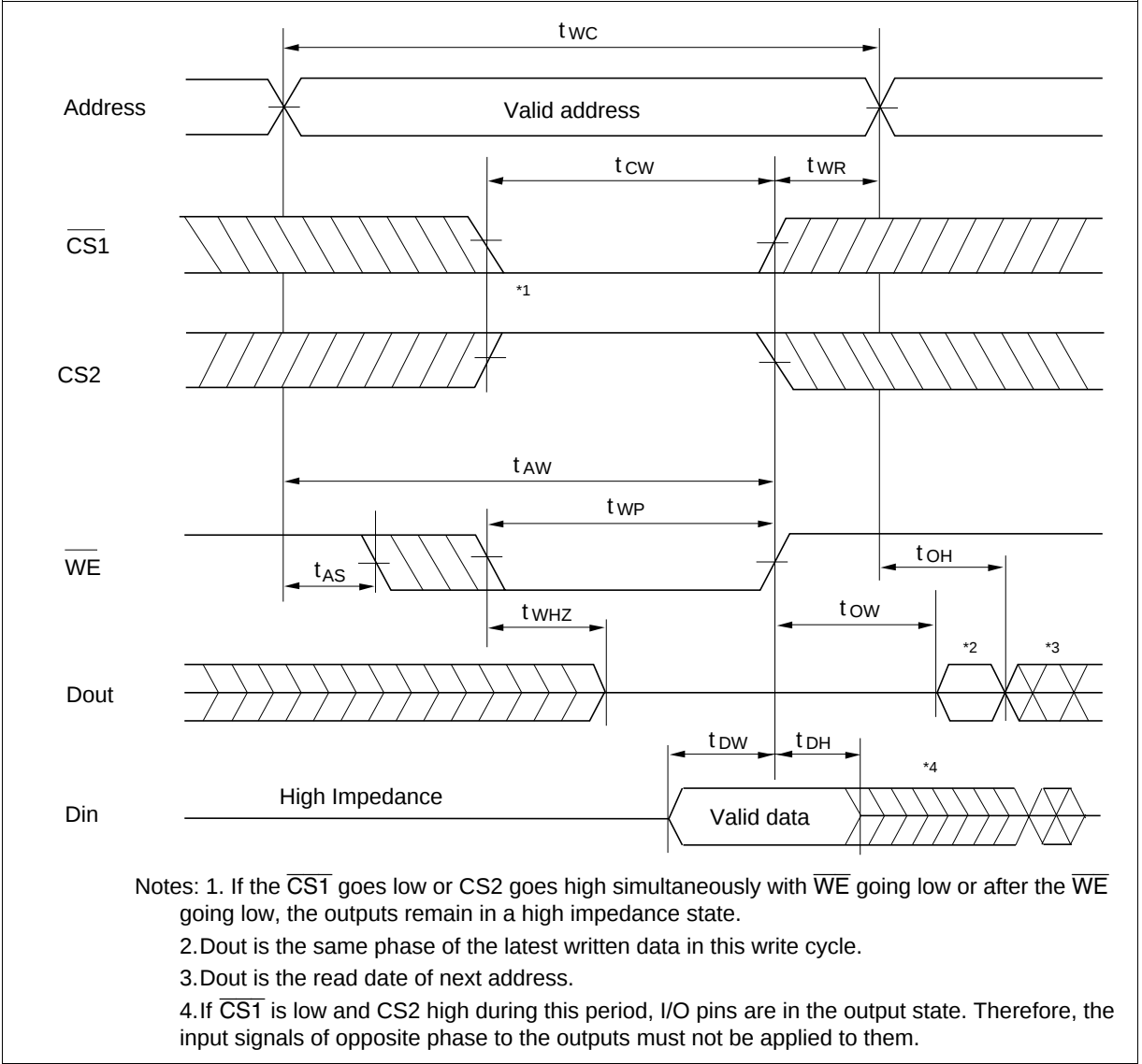
		HM628128B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	70	—	85	—	ns	
Chip selection to end of write	t _{CW}	60	—	75	—	ns	2
Address setup time	t _{AS}	0	—	0	—	ns	3
Address valid to end of write	t _{AW}	60	—	75	—	ns	
Write pulse width	t _{WP}	50	—	55	—	ns	1, 7
Write recovery time	t _{WR}	0	—	0	—	ns	4
Write to output in high-Z	t _{WHZ}	0	25	0	30	ns	5, 6
Data to write time overlap	t _{DW}	30	—	35	—	ns	
Write hold from write time	t _{DH}	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	ns	6
Output disable to output in High-Z	t _{OHz}	0	25	0	25	ns	5

- Notes:
- 1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 - 2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 - 3. t_{AS} is measured from the address valid to the beginning of write.
 - 4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
 - 5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
 - 6. This parameter is sampled and not 100% tested.
 - 7. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention, $t_{WP} \geq t_{DW} \text{ (min)} + t_{WHZ} \text{ (mix)}$.

Write Cycle Timing (1) ($\overline{\text{OE}}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ low fix)

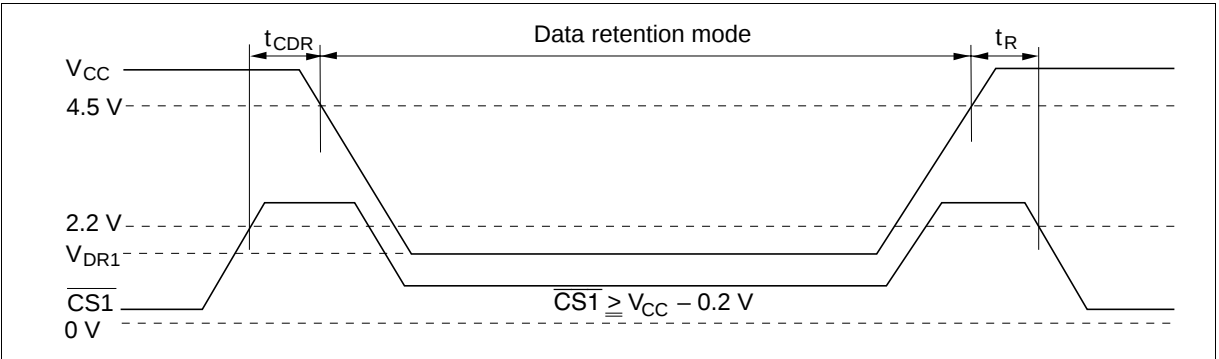


Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

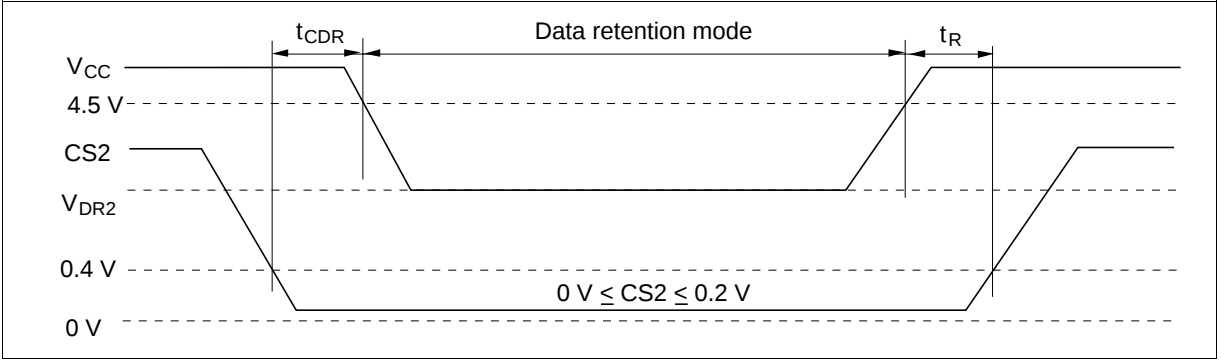
Parameter	Symbol	Min	Typ ^{*3}	Max	Unit	Test conditions ^{*4}
V _{CC} for data retention	V _{DR}	2.0	—	—	V	0 V ≤ Vin ≤ V _{CC} , (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} − 0.2 V, $\overline{\text{CS1}} \geq V_{\text{CC}} - 0.2 \text{ V}$
Data retention current	I _{CCDR} (L)	—	1	50 ^{*1}	μA	V _{CC} = 3 V, 0 V ≤ Vin ≤ 3 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{CC} − 0.2 V, $\overline{\text{CS1}} \geq V_{\text{CC}} - 0.2 \text{ V}$
	(L-SL)	—	1	15 ^{*2}	μA	
Chip deselect to data retention time	t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t _R	5	—	—	ms	

- Notes:
- 1. This characteristics is guaranteed only for L-version, 20 μA max at Ta = 0 to 40°C.
 - 2. This characteristics is guaranteed only for L-SL version, 3 μA max at Ta = 0 to 40°C.
 - 3. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
 - 4. CS2 controls address buffer, $\overline{\text{WE}}$ buffer, $\overline{\text{CS1}}$ buffer, $\overline{\text{OE}}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CS1}}$, I/O) can be in the high impedance state. If $\overline{\text{CS1}}$ controls data retention mode, CS2 must be CS2 ≥ V_{SS} − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Waveform (1) ($\overline{\text{CS1}}$ Controlled)



Low V_{CC} Data Retention Waveform (2) (CS2 Controlled)

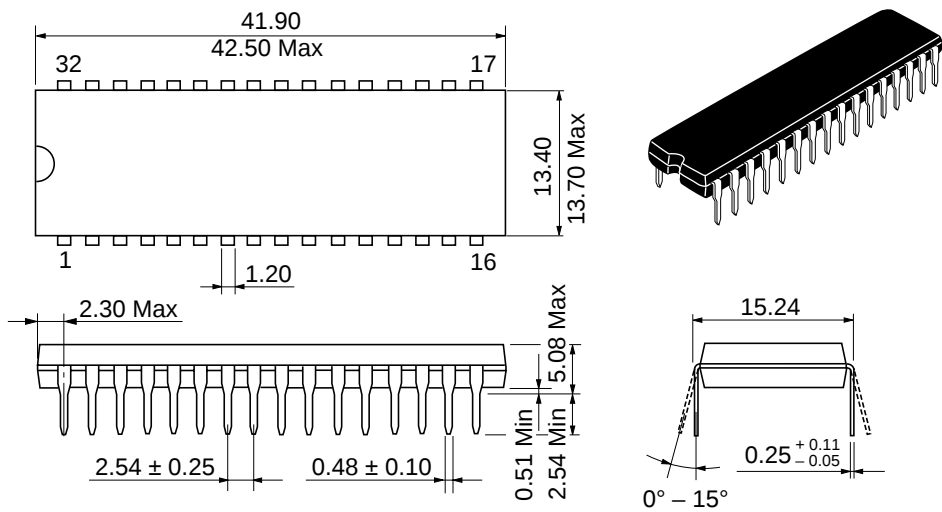


HM628128B Series

Package Dimensions

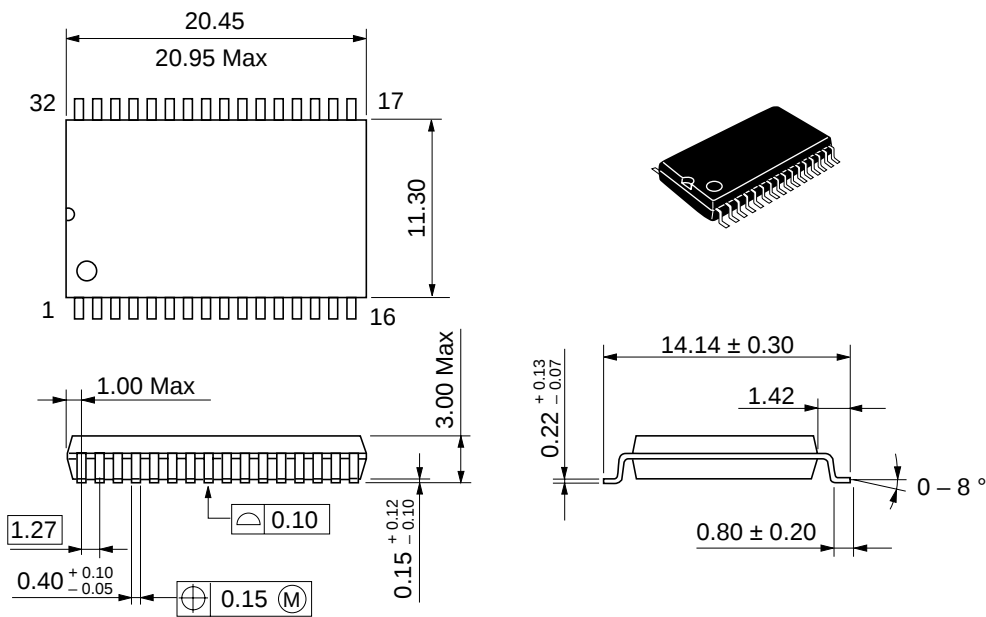
HM628128BLP Series (DP-32)

Unit: mm



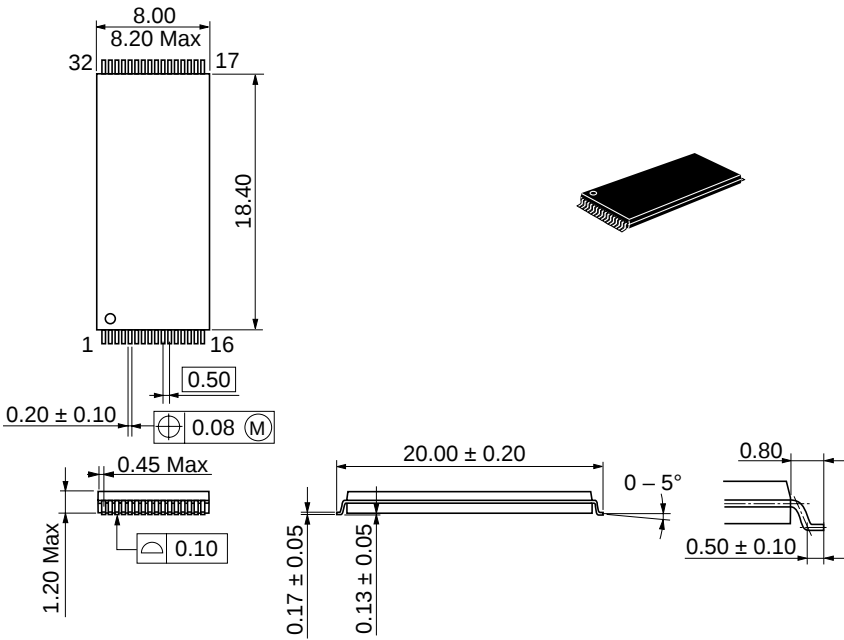
HM628128BLFP Series (FP-32D)

Unit: mm



HM628128BLT Series (TFP-32D)

Unit: mm



HM628128B Series

HM628128BLR Series (TFP-32DR)

Unit: mm

