
HB56E836 Series, HB56E436 Series

8388608-word $\times$ 36-bit High Density Dynamic RAM Module
4194304-word $\times$ 36-bit High Density Dynamic RAM Module

HITACHI

ADE-203-673 (Z)
Preliminary
Rev. 0.0
Oct. 18, 1996

Description

The HB56E836 Series is a 8 M $\times$ 36 Dynamic RAM Module, mounted 16 pieces of 16-Mbit DRAM (HM5117405) sealed in SOJ package and 8 piece of of 4-Mbit DRAM (HM514105) sealed in SOJ package. The HB56E436 Series is a 4 M $\times$ 36 Dynamic RAM Module, mounted 8 pieces of 16-Mbit DRAM (HM5117405) sealed in SOJ package and 4 piece of of 4-Mbit DRAM (HM514105) sealed in SOJ package. The HB56E836 Series, HB56E436 Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56E836 Series, HB56E436 Series are 72-pin single in-line package. Therefore, the HB56E836 Series, HB56E436 Series make high density mounting possible without surface mount technology. The HB56E836 Series, HB56E436 Series provide common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the module board.

Features

- 72-pin single in-line package
 - Outline: 107.95 mm (Length) $\times$ 31.75/25.4 mm (Height) $\times$ 9.14 mm (Thickness)
 - Lead pitch : 1.27 mm
- Single 5 V ($\pm 5\%$)
- High speed
 - Access time: 60 ns/70 ns (max)
- Low power dissipation
 - Active mode: 7.25 W/6.62 W (max) (HB56E836 Series)
 - Active mode: 6.93 W/6.30 W (max) (HB56E436 Series)
 - Standby mode: 252 mW (max) (HB56E836 Series)
 - Standby mode: 126 mW (max) (HB56E436 Series)
- EDO page mode capability

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

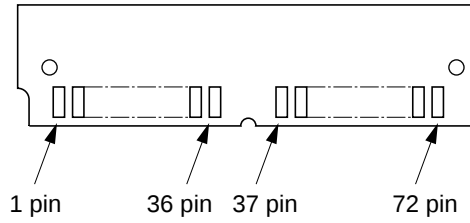
HB56E836 Series, HB56E436 Series

- 2048 refresh cycles: 32 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56E836BR-6	60 ns	72-pin SIP socket type	Gold
HB56E836BR-7	70 ns		
HB56E436BR-6	60 ns	72-pin SIP socket type	Solder
HB56E436BR-7	70 ns		
HB56E836SBR-6	60 ns	72-pin SIP socket type	Solder
HB56E836SBR-7	70 ns		
HB56E436SBR-6	60 ns	72-pin SIP socket type	Solder
HB56E436SBR-7	70 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	19	A10	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V _{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{\text{RAS1}}$ (NC)* ²	63	DQ15
10	V _{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	$\overline{\text{RAS3}}$ (NC)* ¹	51	DQ10	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V _{SS}

Notes: 1. $\overline{\text{RAS3}}$: HB56E836, NC: HB56E436

2. $\overline{\text{RAS1}}$: HB56E836, NC: HB56E436

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Pin Description

Pin name	Function
A0 to A10	Address input — Row addressA0 to A10 — Column addressA0 to A10 — Refresh addressA0 to A10
DQ0 to DQ35	Data input/output
$\overline{\text{RAS0}}$, to $\overline{\text{RAS3}}$	Row address strobe
$\overline{\text{CAS0}}$ to $\overline{\text{CAS3}}$	Column address strobe
$\overline{\text{WE0}}$, $\overline{\text{WE2}}$	Read/Write enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD4	Presence detect pin
NC	No connection

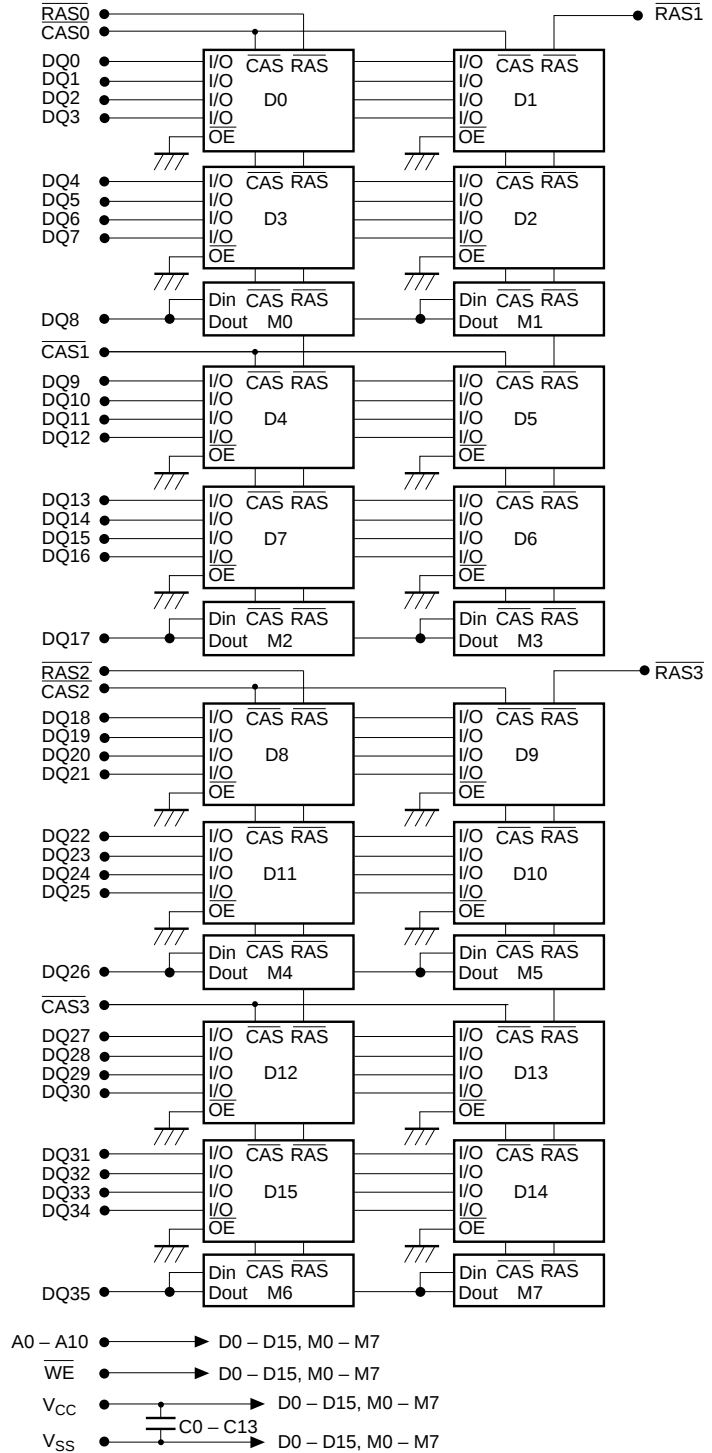
Presence Detect Pin Arrangement (HB56E836 Series)

Pin No.	Pin name	HB56E836	
		60 ns	70 ns
67	PD1	NC	NC
68	PD2	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}
70	PD4	NC	NC

Presence Detect Pin Arrangement (HB56E436 Series)

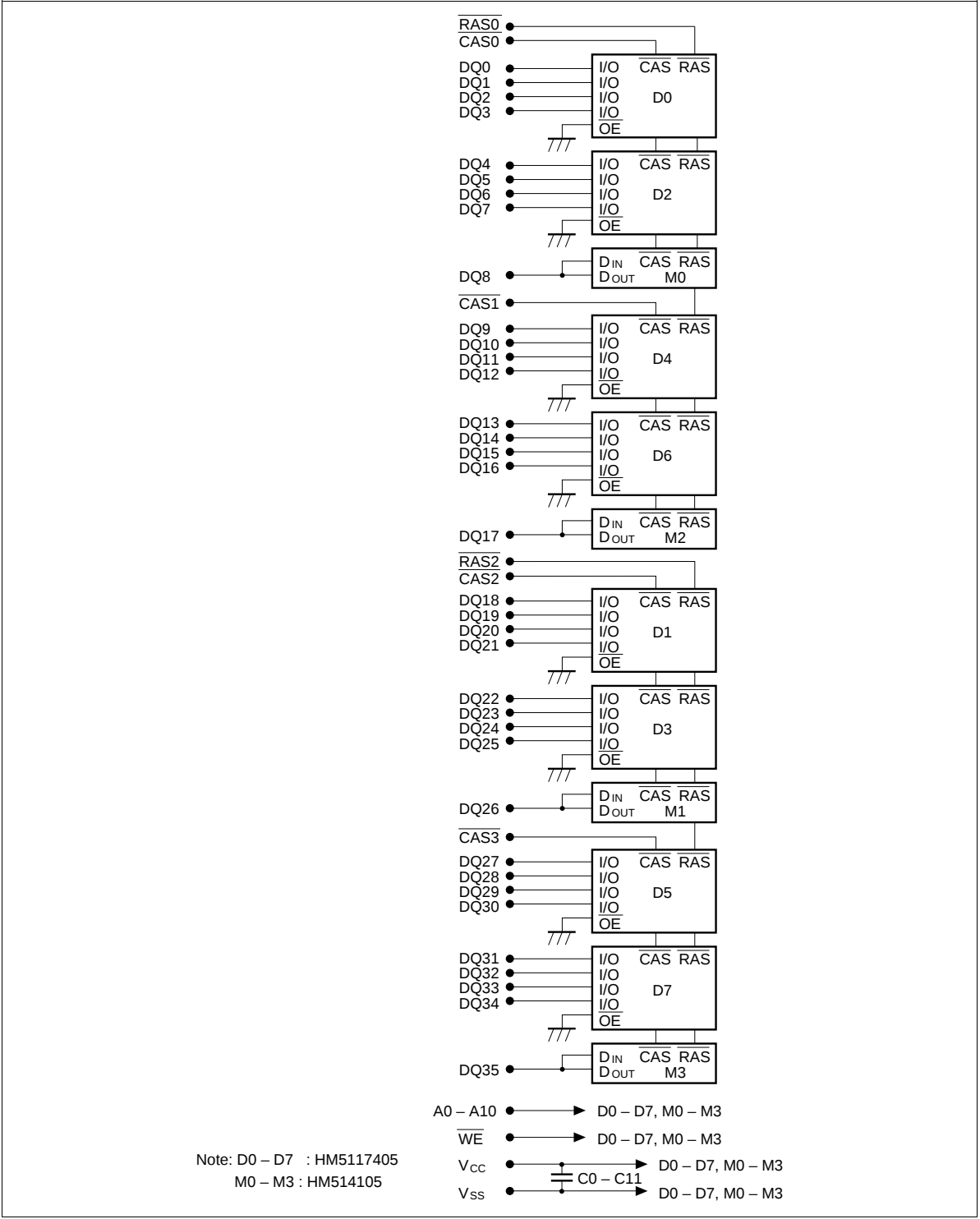
Pin No.	Pin name	HB56E436	
		60 ns	70 ns
67	PD1	V_{SS}	V_{SS}
68	PD2	NC	NC
69	PD3	NC	V_{SS}
70	PD4	NC	NC

Block Diagram (HB56E836)



HB56E836 Series, HB56E436 Series

Block Diagram (HB56E436)



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	12	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56E836)

		HB56E836					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	1380	—	1260	mA	t _{RC} = min
Standby current	I _{CC2}	—	48	—	48	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	24	—	24	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	1380	—	1260	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	120	—	120	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	1380	—	1260	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	1460	—	1340	mA	t _{HPC} = min
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

- Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56E436)

		HB56E436					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	1320	—	1200	mA	t _{RC} = min
Standby current	I _{CC2}	—	24	—	24	mA	TTL interface R _{AS} , C _{AS} = V _{IH} Dout = High-Z
		—	12	—	12	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} − 0.2 V Dout = High-Z
R _{AS} -only refresh current* ²	I _{CC3}	—	1320	—	1200	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	60	—	60	mA	R _{AS} = V _{IH} , C _{AS} = V _{IL} Dout = enable
C _{AS} -before-R _{AS} refresh current	I _{CC6}	—	1320	—	1200	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	1400	—	1280	mA	t _{HPC} = min
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while R_{AS} = V_{IL}.

3. Address can be changed once or less while C_{AS} = V_{IH}.

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Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56E836)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	161	pF	1
Input capacitance ($\overline{WE}$)	C _{I2}	—	193	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C _{I3}	—	62	pF	1
I/O capacitance (DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34)	C _{I/O1}	—	29	pF	1, 2
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C _{I/O2}	—	39	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56E436)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	88	pF	1
Input capacitance ($\overline{WE}$)	C _{I2}	—	104	pF	1
Input capacitance ($\overline{RAS}$)	C _{I3}	—	57	pF	1
Input capacitance ($\overline{CAS}$)	C _{I4}	—	36	pF	1
I/O capacitance (DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34)	C _{I/O1}	—	17	pF	1, 2
I/O capacitance (DQ8, DQ17, DQ26, DQ35)	C _{I/O2}	—	22	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) ^{*1, *2}
Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL} = 0\text{ V}$, $V_{IH} = 3\text{ V}$
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HB56E836/HB56E436					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	13	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	48	—	58	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	ns	
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t _T	2	50	2	50	ns	5

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Read Cycle

Parameter	Symbol	HB56E836/HB56E436				Unit	Notes
		60 ns		70 ns			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	6, 7
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	10
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	10
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	11
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	

Write Cycle

		HB56E836/HB56E436					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	12
Write command hold time	t _{WCH}	10	—	13	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	13
Data-in hold time	t _{DH}	10	—	13	—	ns	13

Refresh Cycle

		HB56E836/HB56E436					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{\text{WE}}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{\text{WE}}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t_{RPC}	10	—	10	—	ns	

EDO Page Mode Cycle

		HB56E836/HB56E436					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	25	—	30	—	ns	
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	ns	14
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	35	—	40	ns	7, 15
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	35	—	40	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	ns	7, 15
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHC}	35	—	40	—	ns	

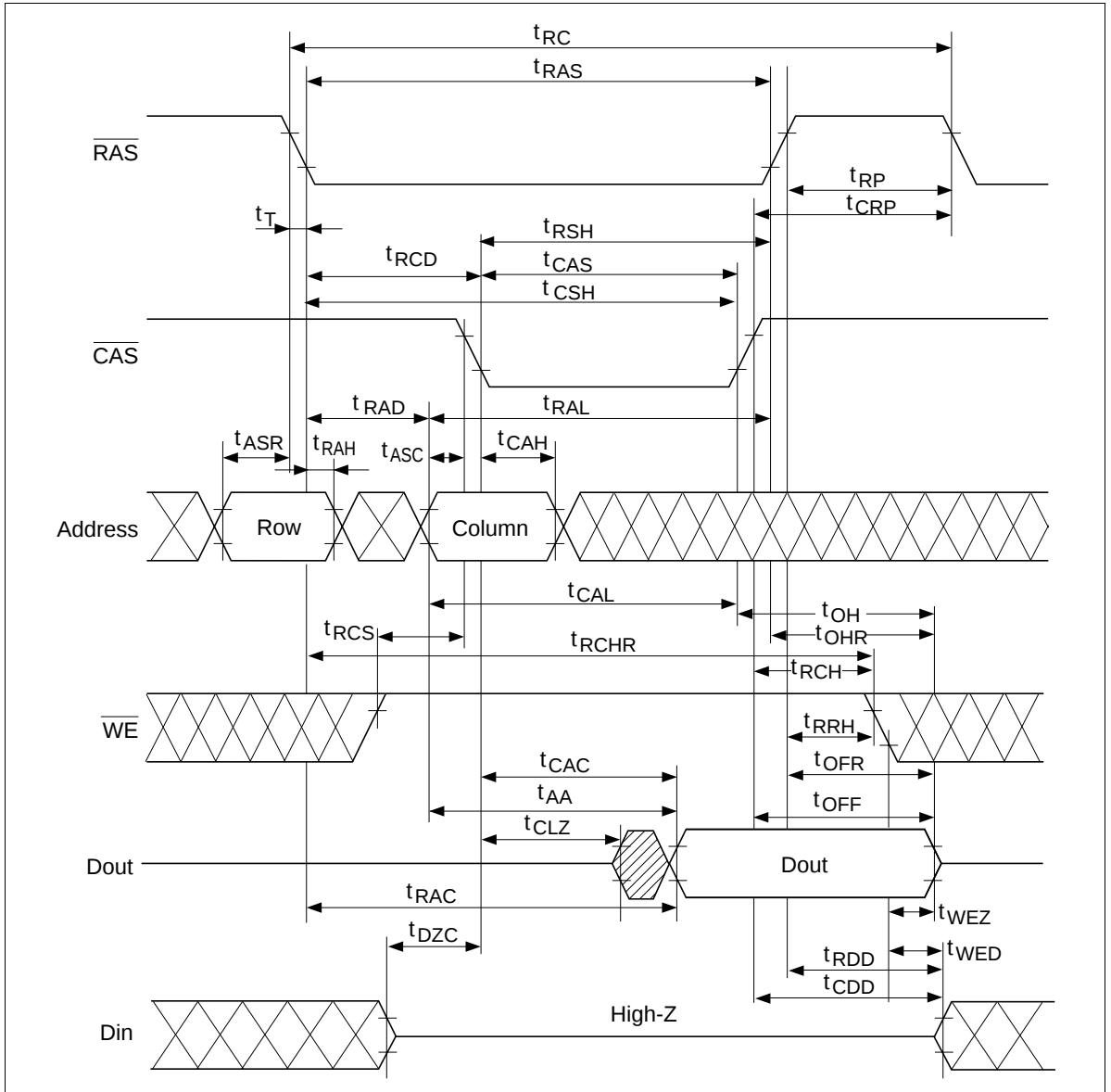
Refresh

Parameter	Symbol	Max	Unit	Notes
Refresh period	t_{REF}	32	ms	2048 cycles

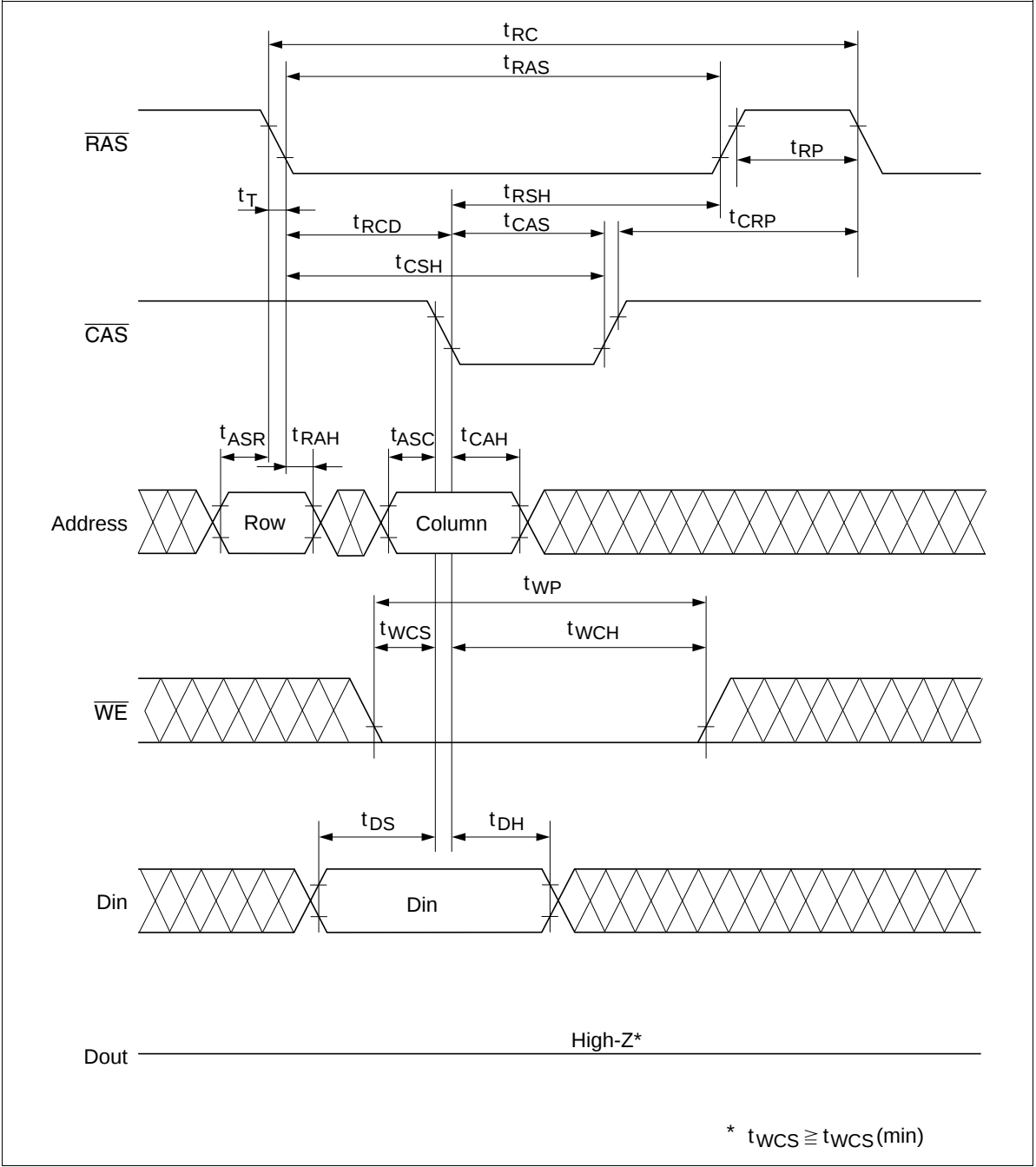
- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. An initial pause of $200 \mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh).
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 6. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 7. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 9. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 12. If $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
 13. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles.
 14. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 15. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 16. XXX: H or L (H: V_{IH} (min) $\leq V_{\text{IN}} \leq V_{\text{IH}}$ (max), L: V_{IL} (min) $\leq V_{\text{IN}} \leq V_{\text{IL}}$ (max))
////////: Invalid Dout
- When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*16

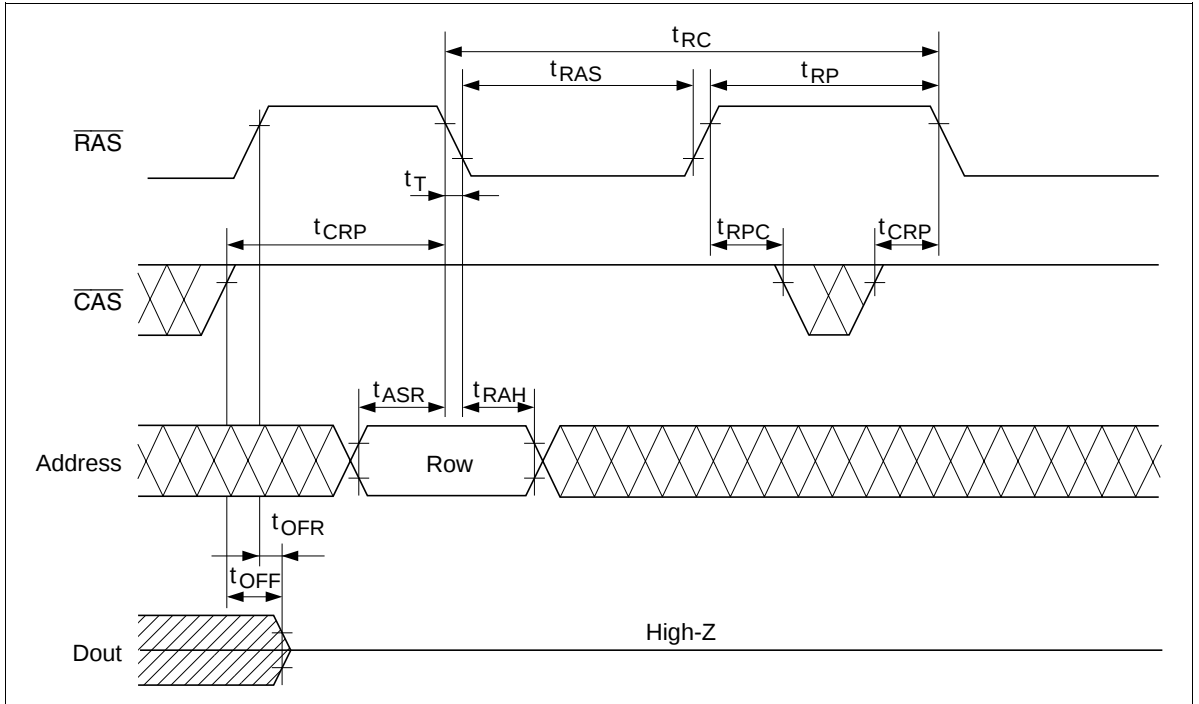
Read Cycle



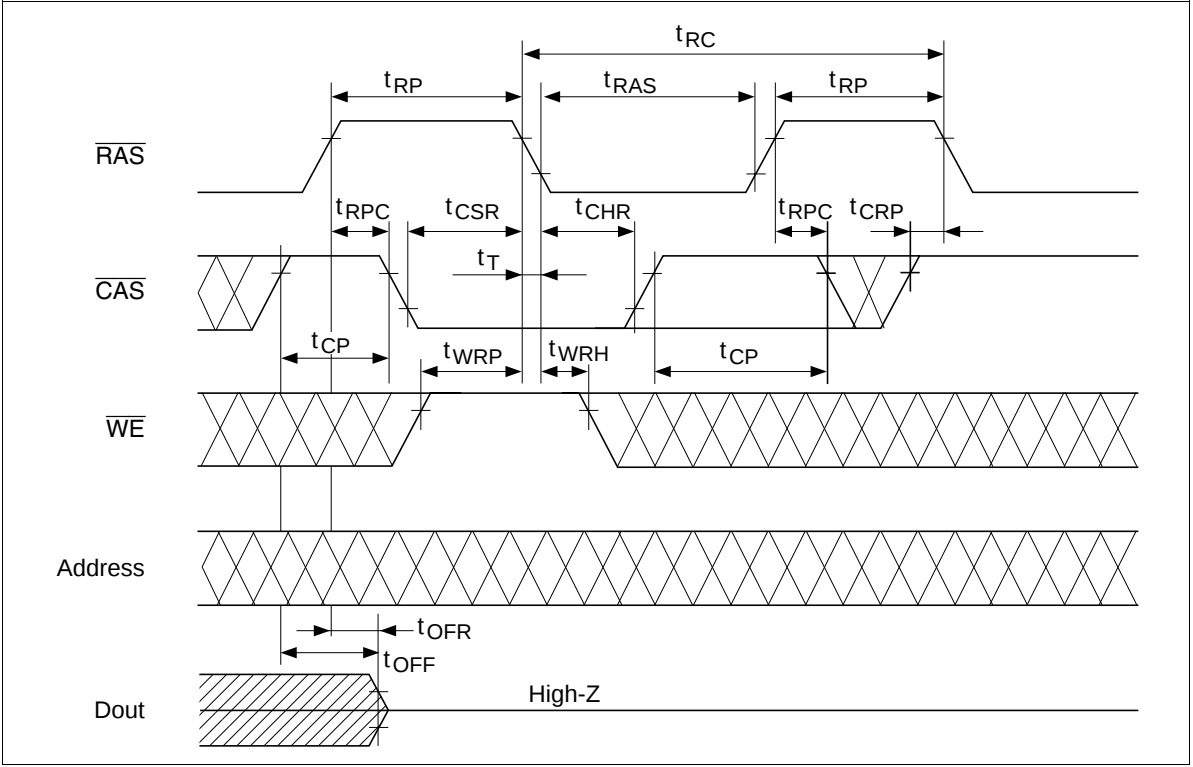
Early Write Cycle



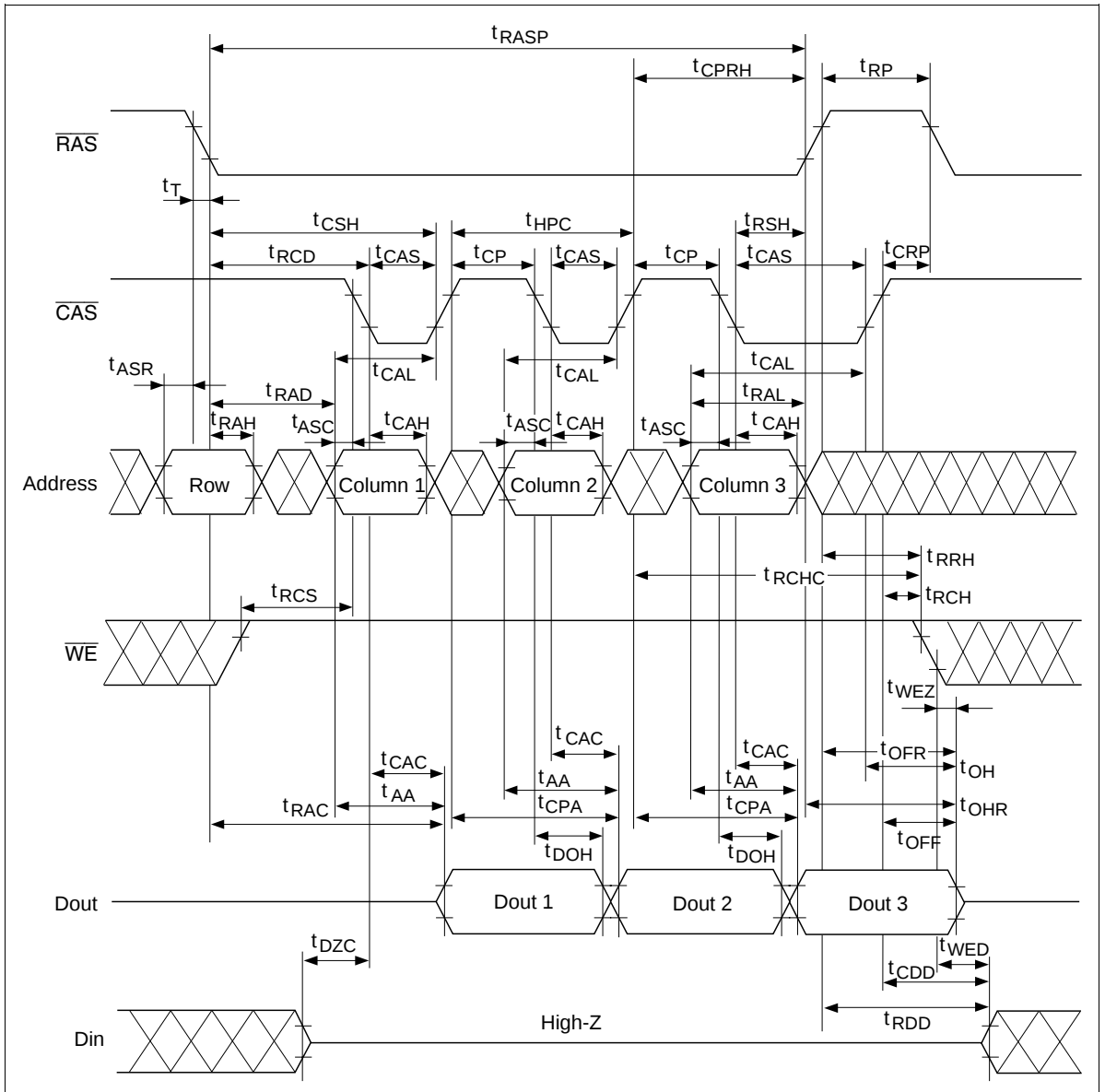
RAS-Only Refresh Cycle



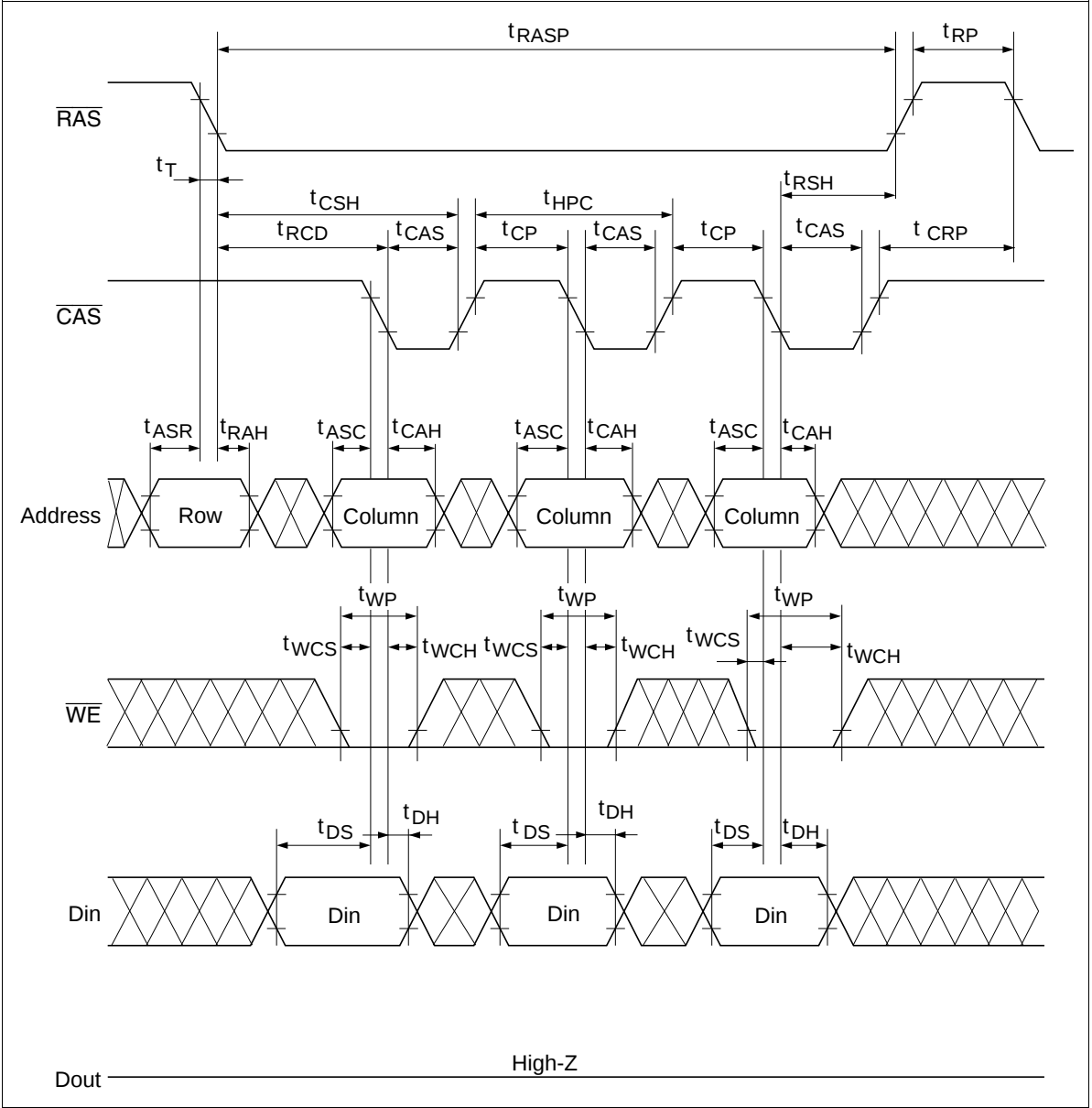
CAS-Before-RAS Refresh Cycle



EDO Page Mode Read Cycle



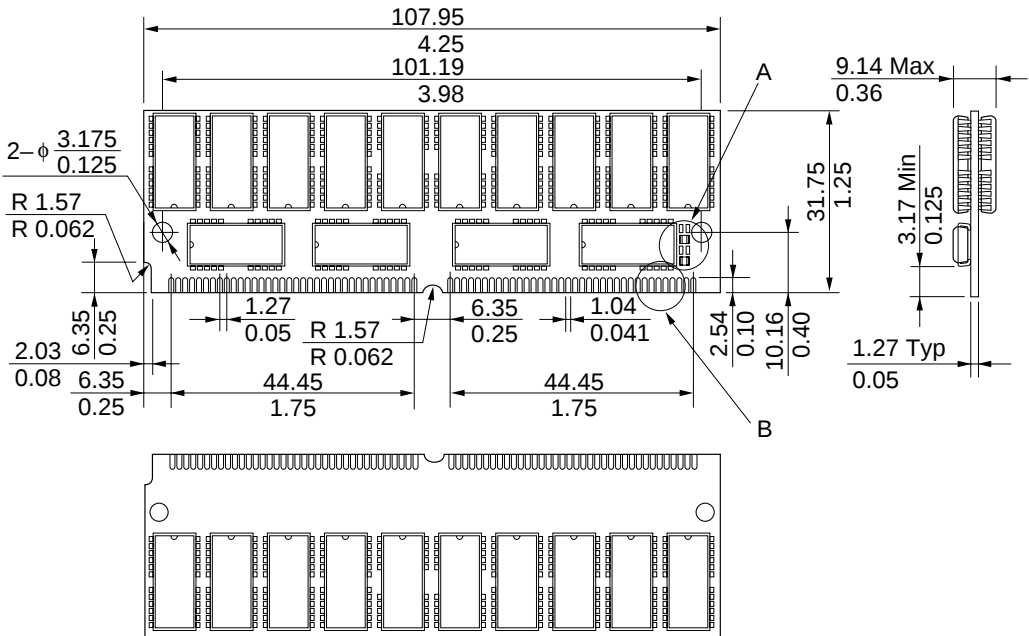
EDO Page Mode Early Write Cycle



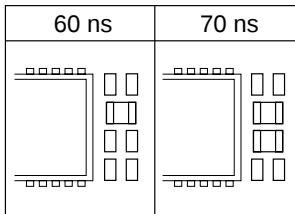
Physical Outline

HB56E836 Series

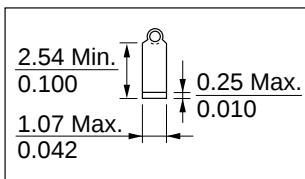
Unit: mm/inch



Detail A



Detail B



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