HB56D172EJ Series

1,048,576-word × 72-bit High Density Dynamic RAM Module

HITACHI

ADE-203-
Rev. 0.0
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Description

The HB56D172EJ belongs to 8 byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 byte processor applications.

The HB56D172EJ is a 1 M × 72 dynamic RAM module, mounted 16 pieces of 4-Mbit DRAM (HM514400CS) sealed in SOJ package and 4 pieces of 2-Mbit DRAM (HM512200BS) sealed in SOJ package and 2 pieces of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package. An outline of the HB56D172EJ is 168-pin socket type package (dual lead out). Therefore, the HB56D172EJ makes high density mounting possible without surface mount technology. The HB56D172EJ provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the module board.

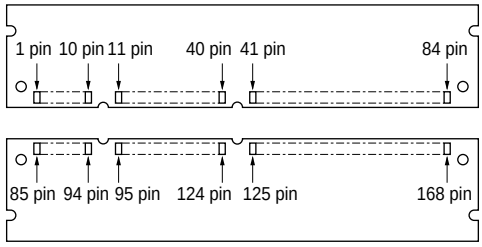
Features

- 168-pin socket type package (Dual lead out)
  - Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - Access time: t_{RAC} = 60/70/80 ns (max)
  - Access time: t_{CAC} = 20/25/25 ns (max)
- Low power dissipation
  - Active mode: 11.26/10.21/9.16 W (max)
  - Standby mode: 546 mW (max)
- Buffered input except $\overline{RAS}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 1,024 refresh cycle: 16 ms
- 2 variations of refresh
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56D172EJ-6C	60 ns	168-pin dual lead out socket type	gold
HB56D172EJ-7C	70 ns		
HB56D172EJ-8C	80 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	26	V_{CC}	51	NC	76	DQ34
2	DQ0	27	$\overline{WE0}$	52	DQ18	77	DQ35
3	DQ1	28	$\overline{CE0}$	53	DQ19	78	V_{SS}
4	DQ2	29	$\overline{CE2}$	54	V_{SS}	79	PD1
5	DQ3	30	$\overline{RE0}$	55	DQ20	80	PD3
6	V_{CC}	31	$\overline{OE0}$	56	DQ21	81	PD5
7	DQ4	32	V_{SS}	57	DQ22	82	PD7
8	DQ5	33	A0	58	DQ23	83	ID0 (NC)
9	DQ6	34	A2	59	V_{CC}	84	V_{CC}
10	DQ7	35	A4	60	DQ24	85	V_{SS}
11	DQ8	36	A6	61	NC	86	DQ36
12	V_{SS}	37	A8	62	NC	87	DQ37
13	DQ9	38	NC	63	NC	88	DQ38
14	DQ10	39	NC	64	NC	89	DQ39
15	DQ11	40	V_{CC}	65	DQ25	90	V_{CC}
16	DQ12	41	NC	66	DQ26	91	DQ40
17	DQ13	42	NC	67	DQ27	92	DQ41
18	V_{CC}	43	V_{SS}	68	V_{SS}	93	DQ42
19	DQ14	44	$\overline{OE2}$	69	DQ28	94	DQ43
20	DQ15	45	$\overline{RE2}$	70	DQ29	95	DQ44
21	DQ16	46	$\overline{CE4}$	71	DQ30	96	V_{SS}
22	DQ17	47	$\overline{CE6}$	72	DQ31	97	DQ45
23	V_{SS}	48	$\overline{WE2}$	73	V_{CC}	98	DQ46
24	NC	49	V_{CC}	74	DQ32	99	DQ47
25	NC	50	NC	75	DQ33	100	DQ48

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
101	DQ49	118	A3	135	NC	152	V_{SS}
102	V_{CC}	119	A5	136	DQ54	153	DQ64
103	DQ50	120	A7	137	DQ55	154	DQ65
104	DQ51	121	A9	138	V_{SS}	155	DQ66
105	DQ52	122	NC	139	DQ56	156	DQ67
106	DQ53	123	NC	140	DQ57	157	V_{CC}
107	V_{SS}	124	V_{CC}	141	DQ58	158	DQ68
108	NC	125	NC	142	DQ59	159	DQ69
109	NC	126	B0	143	V_{CC}	160	DQ70
110	V_{CC}	127	V_{SS}	144	DQ60	161	DQ71
111	NC	128	NC	145	NC	162	V_{SS}
112	$\overline{CE1}$	129	NC	146	NC	163	PD2
113	$\overline{CE3}$	130	$\overline{CE5}$	147	NC	164	PD4
114	NC	131	$\overline{CE7}$	148	NC	165	PD6
115	NC	132	$\overline{PDE}$	149	DQ61	166	PD8
116	V_{SS}	133	V_{CC}	150	DQ62	167	ID1 (V_{SS})
117	A1	134	NC	151	DQ63	168	V_{CC}

Pin Description

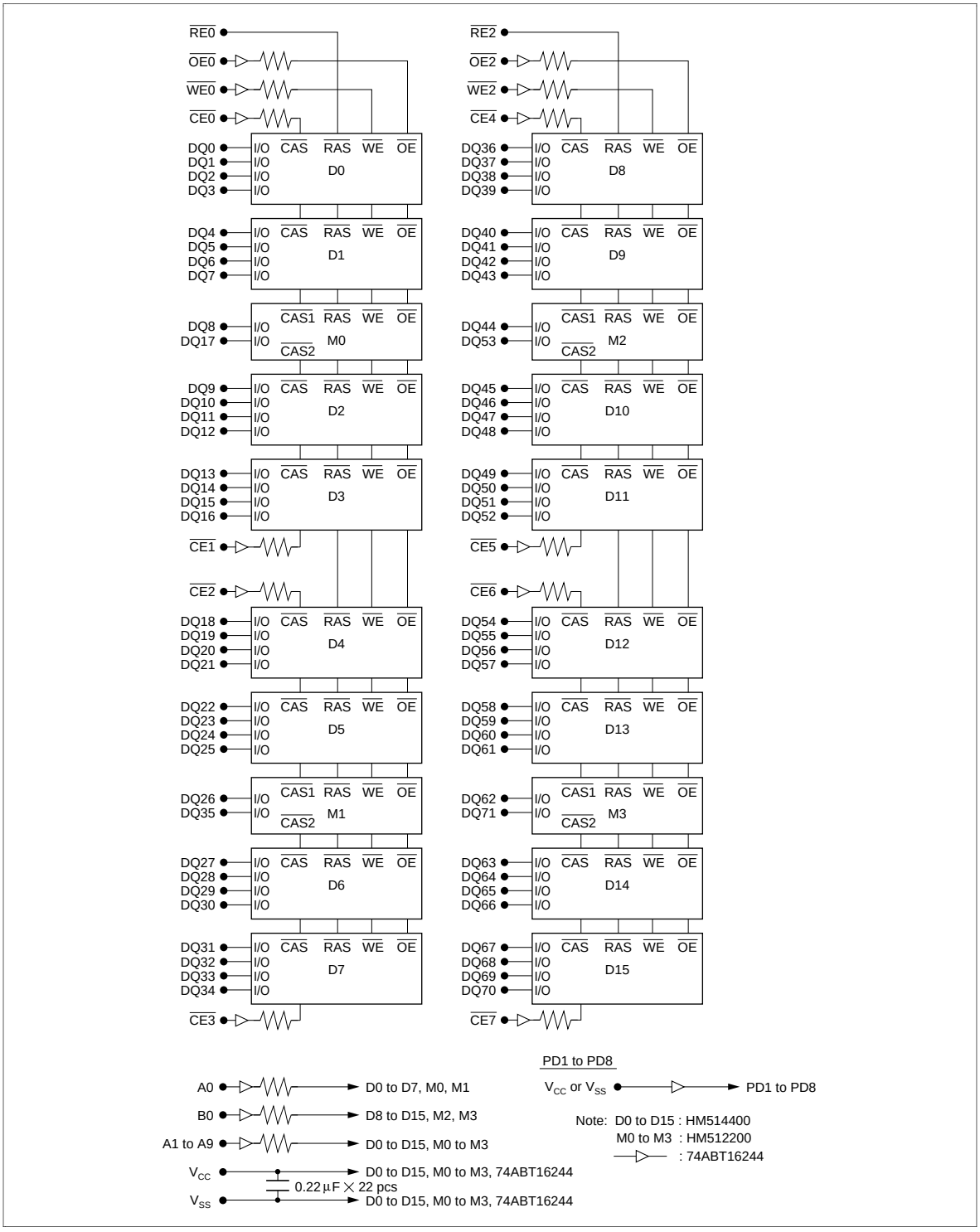
Pin name	Function
A0 to A9, B0	Address input: A0 to A9, B0 Row address: A0 to A9, B0 Column address: A0 to A9, B0 Refresh address: A0 to A9, B0
DQ0 to DQ71	Data-in/data-out
$\overline{RE0}$, $\overline{RE2}$	Row Address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE7}$	Column address strobe ($\overline{CAS}$)
$\overline{WE0}$, $\overline{WE2}$	Read/write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
$\overline{PDE}$	Presence Detect enable
NC	No connection

Presence Detect Pin Assignment

		$\overline{PDE}$ = Low			$\overline{PDE}$ = High
Pin name	**Pin No.**	**60 ns**	**70 ns**	**80 ns**	**All**
PD1	79	0	0	0	High-Z
PD2	163	0	0	0	High-Z
PD3	80	1	1	1	High-Z
PD4	164	0	0	0	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	1	1	1	High-Z

Note: 1: High level (Driver output)
0: Low level (Driver output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	21	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D172EJ								
		60 ns		70 ns		80 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	2144	—	1944	—	1744	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	104	—	104	—	104	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	84	—	84	—	84	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	2144	—	1944	—	1744	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	164	—	164	—	164	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	2144	—	1944	—	1744	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	2144	—	1944	—	1744	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	20	pF	1
Input capacitance (Clock)	C_{I2}	—	20	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	85	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)[*1, *14, *15]

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	55	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	15	—	15	—	15	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	25	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	—	25	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	3
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	16
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	16
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	25	0	25	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	25	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	25	—	25	—	ns	
$\overline{OE}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	

Write Cycle

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	25	—	25	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	20	—	20	—	20	—	ns	11

Read-Modify-Write Cycle

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	150	—	180	—	200	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	—	100	—	110	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	35	—	45	—	45	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	50	—	60	—	65	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	

Refresh Cycle

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	15	—	15	—	15	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time	t_{WS}	5	—	5	—	5	—	ns	
$\overline{WE}$ hold time	t_{WH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HB56D172EJ							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{PCM}	80	—	95	—	100	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	55	—	65	—	70	—	ns	10

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{CPW} \geq t_{CPW}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
    If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied.

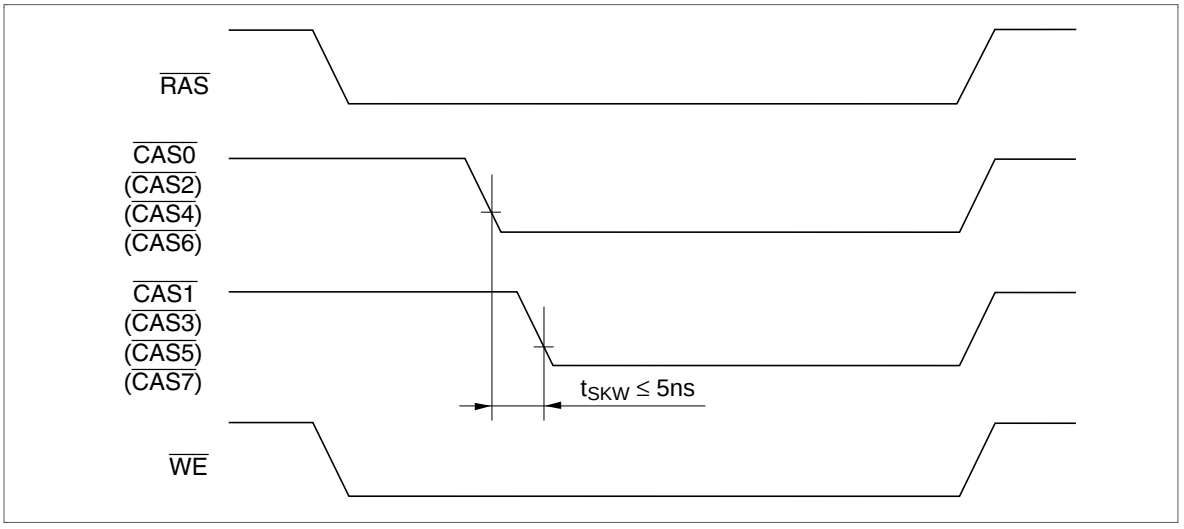
Timing Waveforms

- Refer to the HM514400C Series data sheet.

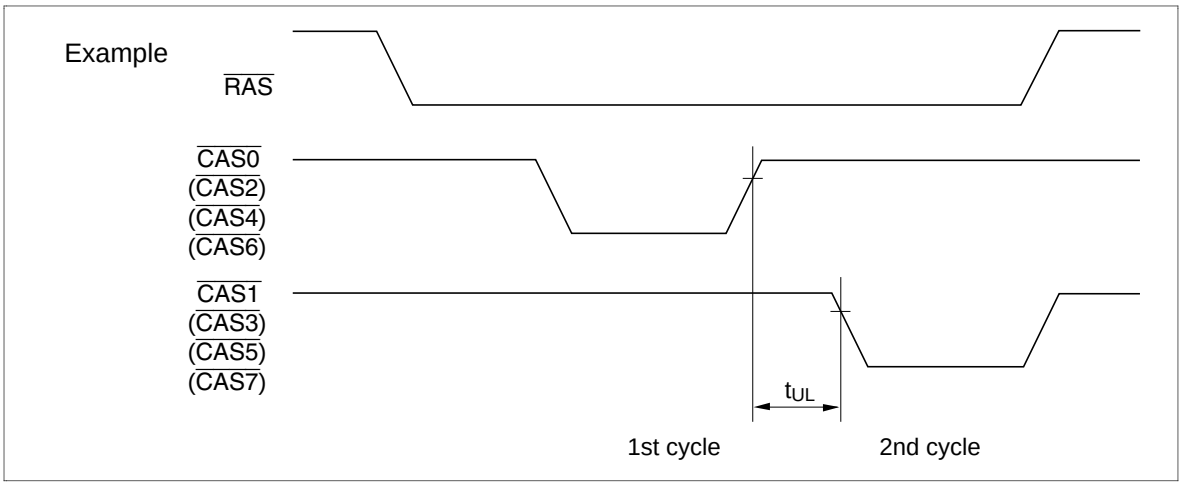
Notes concerning 2$\overline{CAS}$ control

(1) In one memory cycle, activate both of 2CASs ($\overline{CAS0}$ and $\overline{CAS1}$ (or $\overline{CAS2}$, $\overline{4}$, $\overline{6}$ and $\overline{CAS3}$, $\overline{5}$, $\overline{7}$)) or only one of them or neither of them.

(2) To activate both of 2$\overline{CAS}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{CAS0}$ and $\overline{CAS1}$ (or $\overline{CAS2}$, $\overline{4}$, $\overline{6}$ and $\overline{CAS3}$, $\overline{5}$, $\overline{7}$)) 5 ns or less.



(3) If the different $\overline{CAS}$s are activated in the consecutive page cycles, t_{UL}, the period that both $\overline{CAS}$s are high, should be keep t_{CP} spec (t_{CP} min ≤ t_{UL}).



Physical Outline

Unit: mm