
HB56A832BS/SBS Series, HB56A432BR/SBR Series

8,388,608-word $\times$ 32-bit High Density Dynamic RAM Module
4,194,304-word $\times$ 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-728A (Z)

Rev.1.0

Feb. 20, 1997

Description

The HB56A832BS/SBS is a $8\text{M} \times 32$ dynamic RAM module, mounted 16 pieces of 16-Mbit DRAM (HM5117400) sealed in SOJ package. The HB56A432BR/SBR is a $4\text{M} \times 32$ dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117400) sealed in SOJ package. An outline of the HB56A832BS/SBS, HB56A432BR/SBR is 72-pin single in-line package. Therefore, the HB56A832BS/SBS, HB56A432BR/SBR make high density mounting possible without surface mount technology. The HB56A832BS/SBS, HB56A432BR/SBR provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 72-pin single in-line package
 - Outline: 107.95 mm (Length) $\times$ 25.40 mm (Height) $\times$ 9.14/5.28 mm (Thickness)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{\text{RAC}} = 50/60/70\text{ns}$ (max)
- Low power dissipation
 - Active mode: 4.41/3.99/3.57 W (max) (HB56A832BS/SBS Series)
4.20/3.78/3.36 W (max) (HB56A432BR/SBR Series)
 - Standby mode (TTL): 168 mW (max) (HB56A832BS/SBS Series)
(TTL): 84 mW (max) (HB56A432BR/SBR Series)
(CMOS): 12.6 mW (max) (L-version) (HB56A832BS/SBS Series)
(CMOS): 6.3 mW (max) (L-version) (HB56A432BR/SBR Series)
- Fast page mode capability
- Refresh period
 - 2048 refresh cycles: 32 ms
128 ms (L-version)

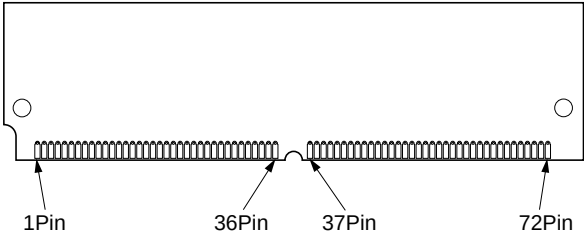
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- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56A832BS-5	50 ns	72-pin SIP socket type	Gold
HB56A832BS-6	60 ns		
HB56A832BS-7	70 ns		
HB56A832BS-5L	50 ns		
HB56A832BS-6L	60 ns		
HB56A832BS-7L	70 ns		
HB56A432BR-5	50 ns		
HB56A432BR-6	60 ns		
HB56A432BR-7	70 ns		
HB56A432BR-5L	50 ns	72-pin SIP socket type	Solder
HB56A432BR-6L	60 ns		
HB56A432BR-7L	70 ns		
HB56A832SBS-5	50 ns		
HB56A832SBS-6	60 ns		
HB56A832SBS-7	70 ns		
HB56A832SBS-5L	50 ns		
HB56A832SBS-6L	60 ns		
HB56A832SBS-7L	70 ns		
HB56A432SBR-5	50 ns		
HB56A432SBR-6	60 ns		
HB56A432SBR-7	70 ns		
HB56A432SBR-5L	50 ns		
HB56A432SBR-6L	60 ns		
HB56A432SBR-7L	70 ns		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{\text{CAS1}}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{\text{RAS1}}$ (NC)* ²	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	$\overline{\text{RAS3}}$ (NC)* ¹	51	DQ9	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

Notes: 1. $\overline{\text{RAS3}}$: HB56A832BS/SBS, NC: HB56A432BR/SBR
2. $\overline{\text{RAS1}}$: HB56A832BS/SBS, NC: HB56A432BR/SBR

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Pin Description

Pin name	Function
A0 to A10	Address inputs: — Row address: A0 to A10 — Column address: A0 to A10 — Refresh address: A0 to A10
DQ0 to DQ31	Data-in/Data-out
$\overline{\text{CAS0}}$ to $\overline{\text{CAS3}}$	Column address strobe
$\overline{\text{RAS0}}$ to $\overline{\text{RAS3}}$	Row address strobe
$\overline{\text{WE}}$	Read/Write enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD4	Presence detect pin
NC	No connection

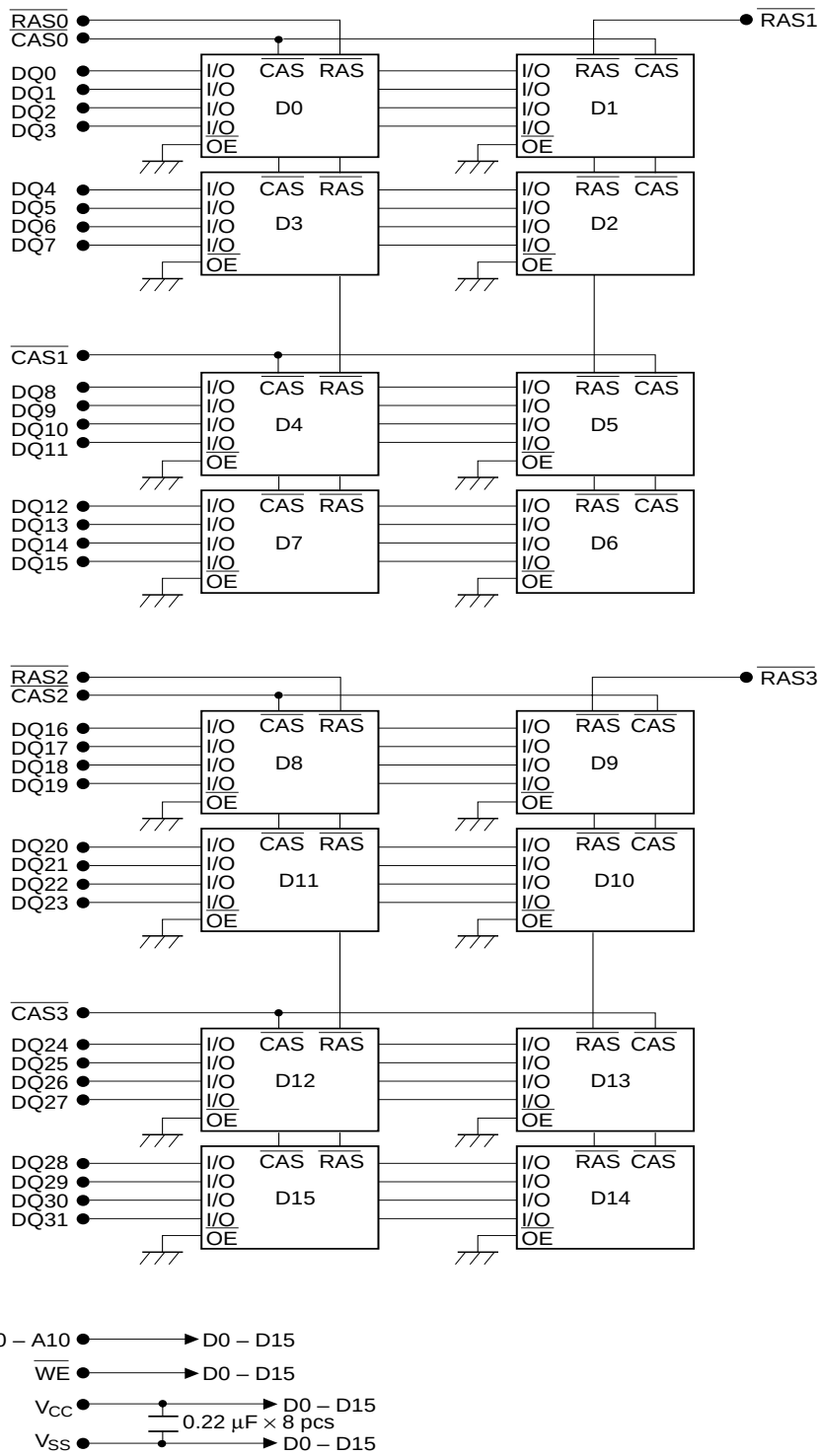
Presence Detect Pin Arrangement (HB56A832BS/SBS)

Pin No.	Pin name	Function		
		50 ns	60 ns	70 ns
67	PD1	NC	NC	NC
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	V_{SS}	NC	V_{SS}
70	PD4	V_{SS}	NC	NC

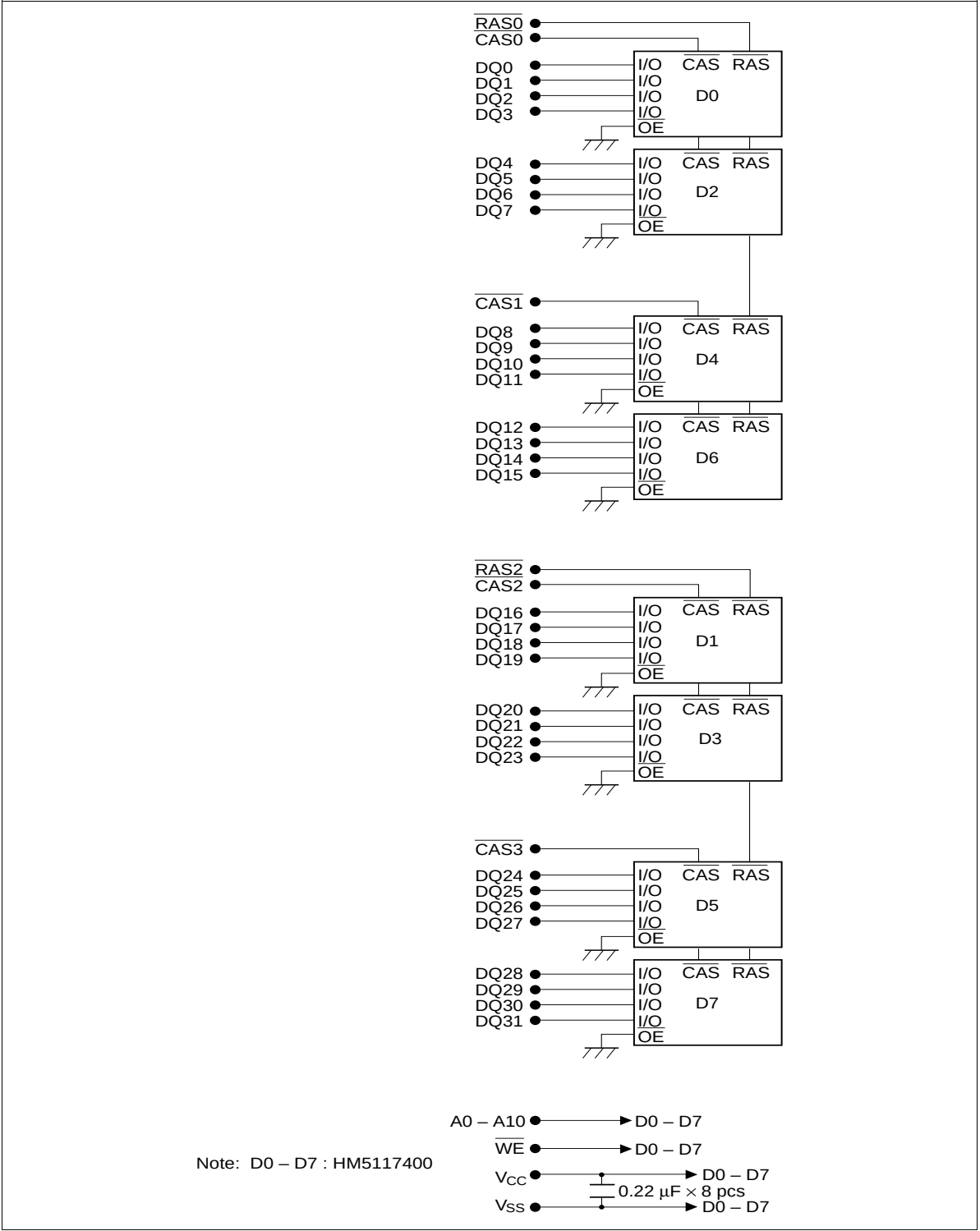
Presence Detect Pin Arrangement (HB56A432BR/SBR)

Pin No.	Pin name	Function		
		50 ns	60 ns	70 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	NC	NC	NC
69	PD3	V_{SS}	NC	V_{SS}
70	PD4	V_{SS}	NC	NC

Block Diagram (HB56A832BS/SBS)



Block Diagram (HB56A432BR/SBR)



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	8	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56A832BS/SBS)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	840	—	760	—	680	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	32	—	32	—	32	mA	TTL interface, RAS, CAS = V _{IH} , Dout = High-Z	
		—	16	—	16	—	16	mA	CMOS interface, RAS, CAS ≥ V _{CC} − 0.2 V, Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	2.4	—	2.4	—	2.4	mA	CMOS interface, RAS, CAS ≥ V _{CC} − 0.2 V, Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	840	—	760	—	680	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	80	—	80	—	80	mA	RAS = V _{IH} , CAS = V _{IL} , Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	840	—	760	—	680	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	760	—	680	—	600	mA	t _{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	5.6	—	5.6	—	5.6	mA	CMOS interface, Dout = High-Z, CBR refresh: t _{RC} = 62.5 μs, t _{RAS} ≤ 0.3 μs	
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 5.5 V, Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

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DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) (HB56A432BR/SBR)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	800	—	720	—	640	mA	$t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface, $\overline{RAS}, \overline{CAS} = V_{IH}$, Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface, $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2\text{ V}$, Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface, $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2\text{ V}$, Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	800	—	720	—	640	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$, Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	800	—	720	—	640	mA	$t_{RC} = \min$	
Fast page mode current	I_{CC7}	—	720	—	640	—	560	mA	$t_{PC} = \min$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	2.8	—	2.8	—	2.8	mA	CMOS interface, Dout = High-Z, CBR refresh: $t_{RC} = 62.5\text{ }\mu\text{s}$, $t_{RAS} \leq 0.3\text{ }\mu\text{s}$	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 5.5\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 5.5\text{ V}$, Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

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Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56A832BS/SBS)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	121	pF	1
Input capacitance ($\overline{WE}$)	C _{I2}	—	137	pF	1
Input capacitance ($\overline{RAS}$)	C _{I3}	—	48	pF	1
Input capacitance ($\overline{CAS}$)	C _{I4}	—	48	pF	1
I/O capacitance (DQ)	C _{I/O}	—	29	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%) (HB56A432BR/SBR)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	68	pF	1
Input capacitance ($\overline{WE}$)	C _{I2}	—	76	pF	1
Input capacitance ($\overline{RAS}$)	C _{I3}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C _{I4}	—	29	pF	1
I/O capacitance (DQ)	C _{I/O}	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 5\%$, $V_{SS} = 0 \text{ V}$) *¹, *², *¹⁷

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90	—	110	—	130	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	7	—	10	—	10	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10000	15	10000	18	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	13	—	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ delay time from D_{in}	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	5
Refresh period (2,048 cycles)	t_{REF}	—	32	—	32	—	32	ms	
Refresh period (2,048 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	

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Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	6, 7
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	25	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	5	—	ns	10
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	11
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	

Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	7	—	10	—	15	—	ns	
Write command pulse width	t_{WCP}	7	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	7	—	10	—	15	—	ns	13

Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	5	—	ns	
CAS hold time (CBR refresh cycle)	t _{CHR}	7	—	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t _{WRP}	0	—	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t _{WRH}	7	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	5	—	5	—	5	—	ns	

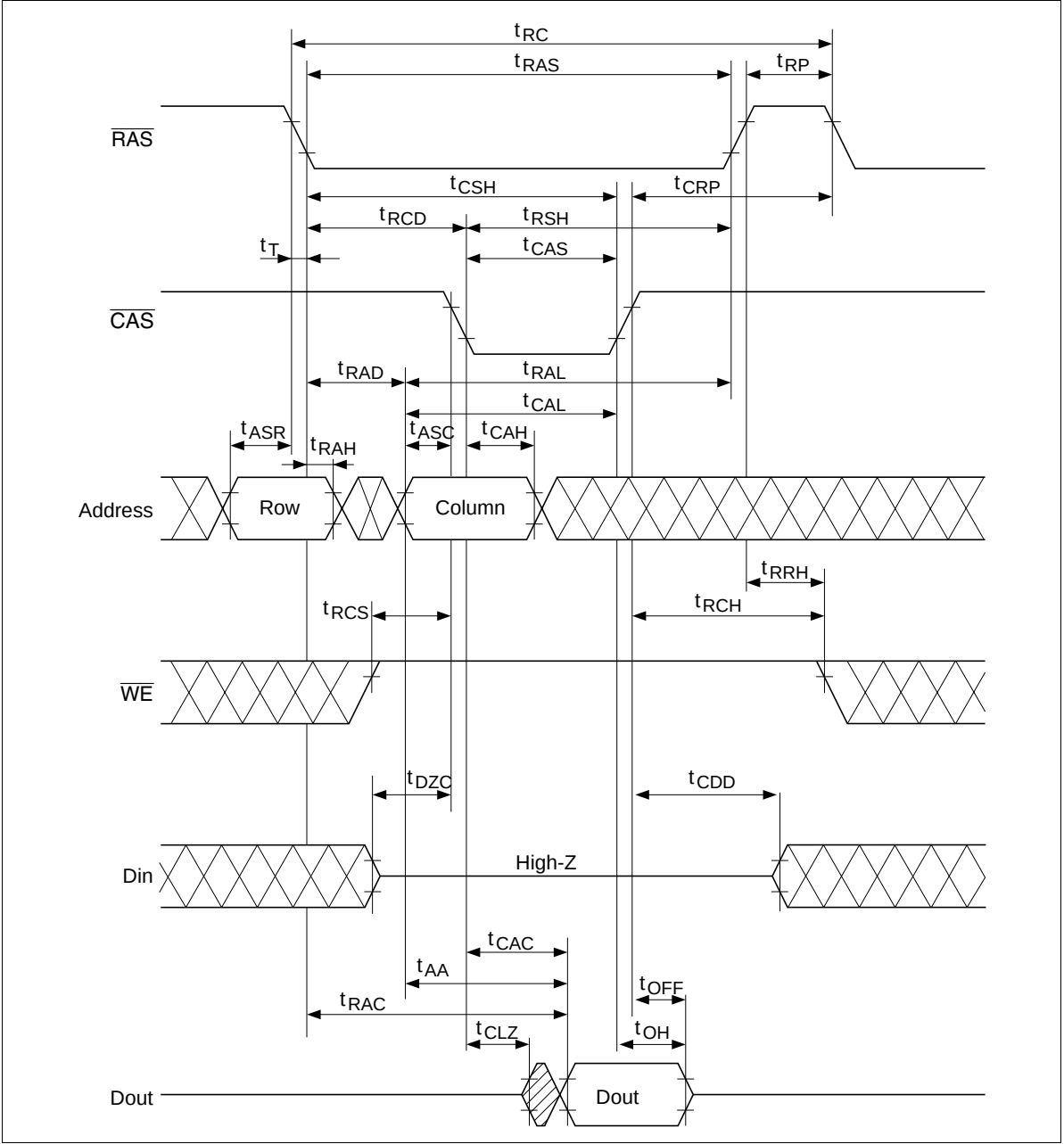
Fast Page Mode Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t _{PC}	35	—	40	—	45	—	ns	
Fast page mode RAS pulse width	t _{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from CAS precharge	t _{CPA}	—	30	—	35	—	40	ns	7, 15
RAS hold time from CAS precharge	t _{CPRH}	30	—	35	—	40	—	ns	

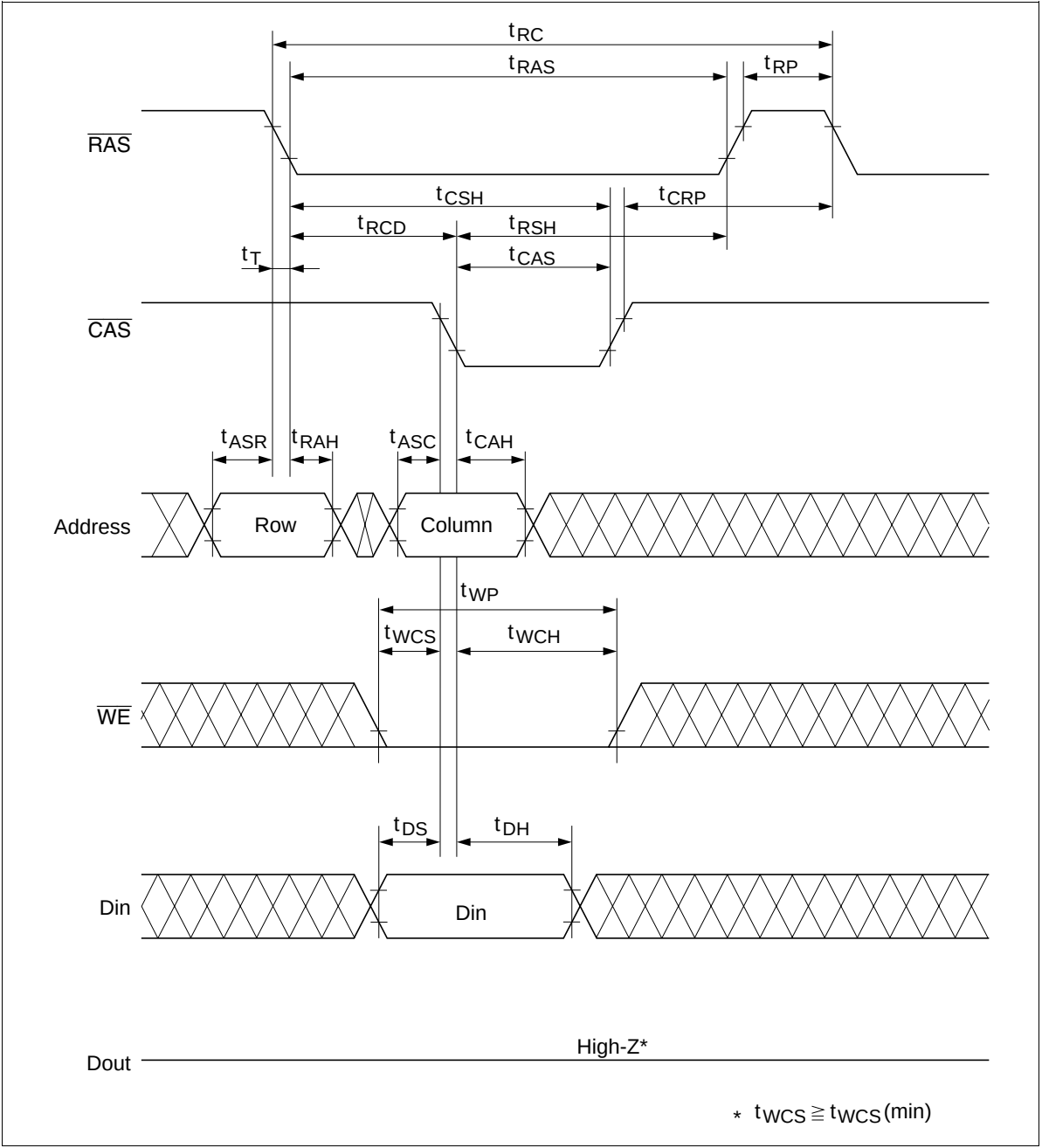
- Notes:
1. AC measurements assume $t_r = 5$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh cycle or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 6. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 9. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 12. Early write cycle only ($t_{\text{WCS}} \geq t_{\text{WCS}}$ (min)).
 13. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles.
 14. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in Fast page mode cycles.
 15. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 16. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}} / V_{\text{SS}}$ line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
 17. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 18. XXX: H or L (H: V_{IH} (min) $\leq V_{\text{IN}} \leq V_{\text{IH}}$ (max), L: V_{IL} (min) $\leq V_{\text{IN}} \leq V_{\text{IL}}$ (max))
/////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*18

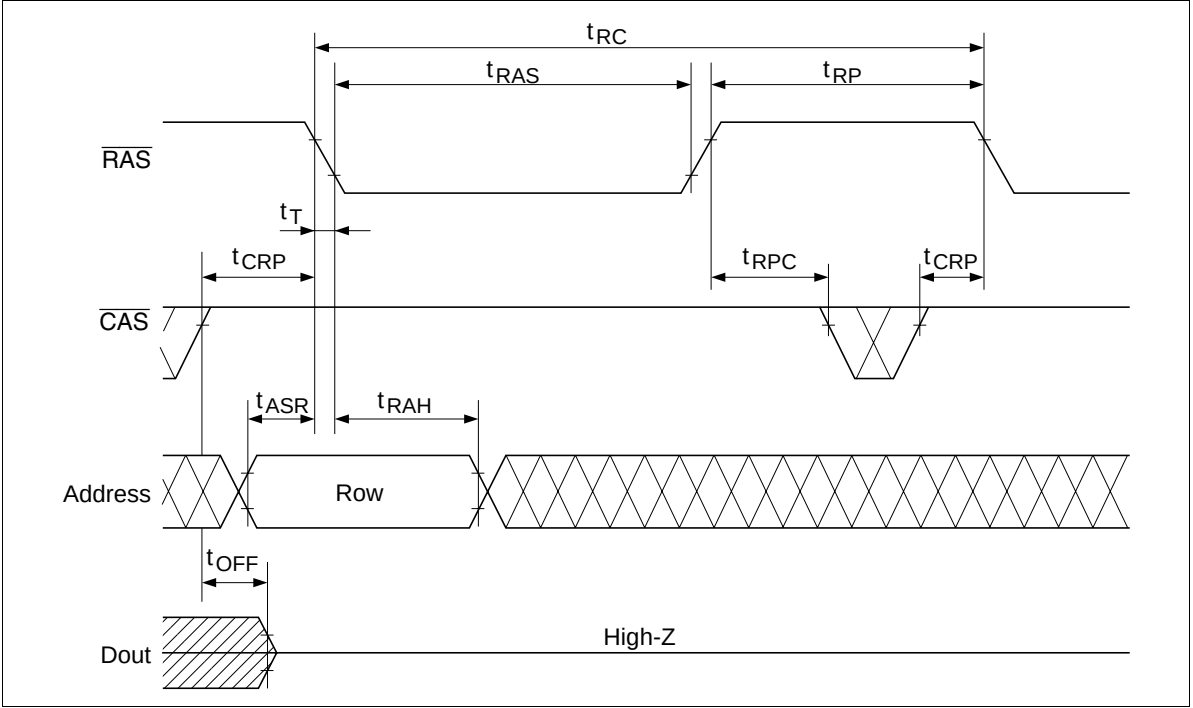
Read Cycle



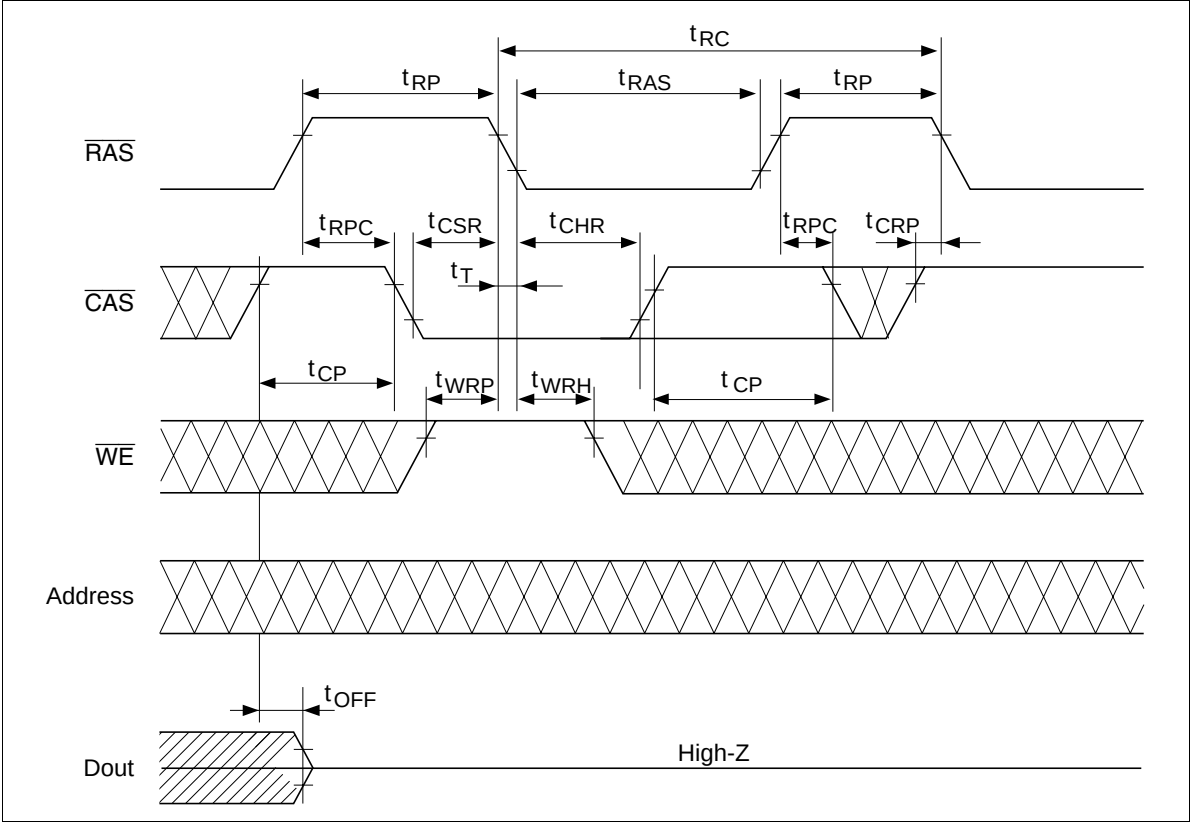
Early Write Cycle



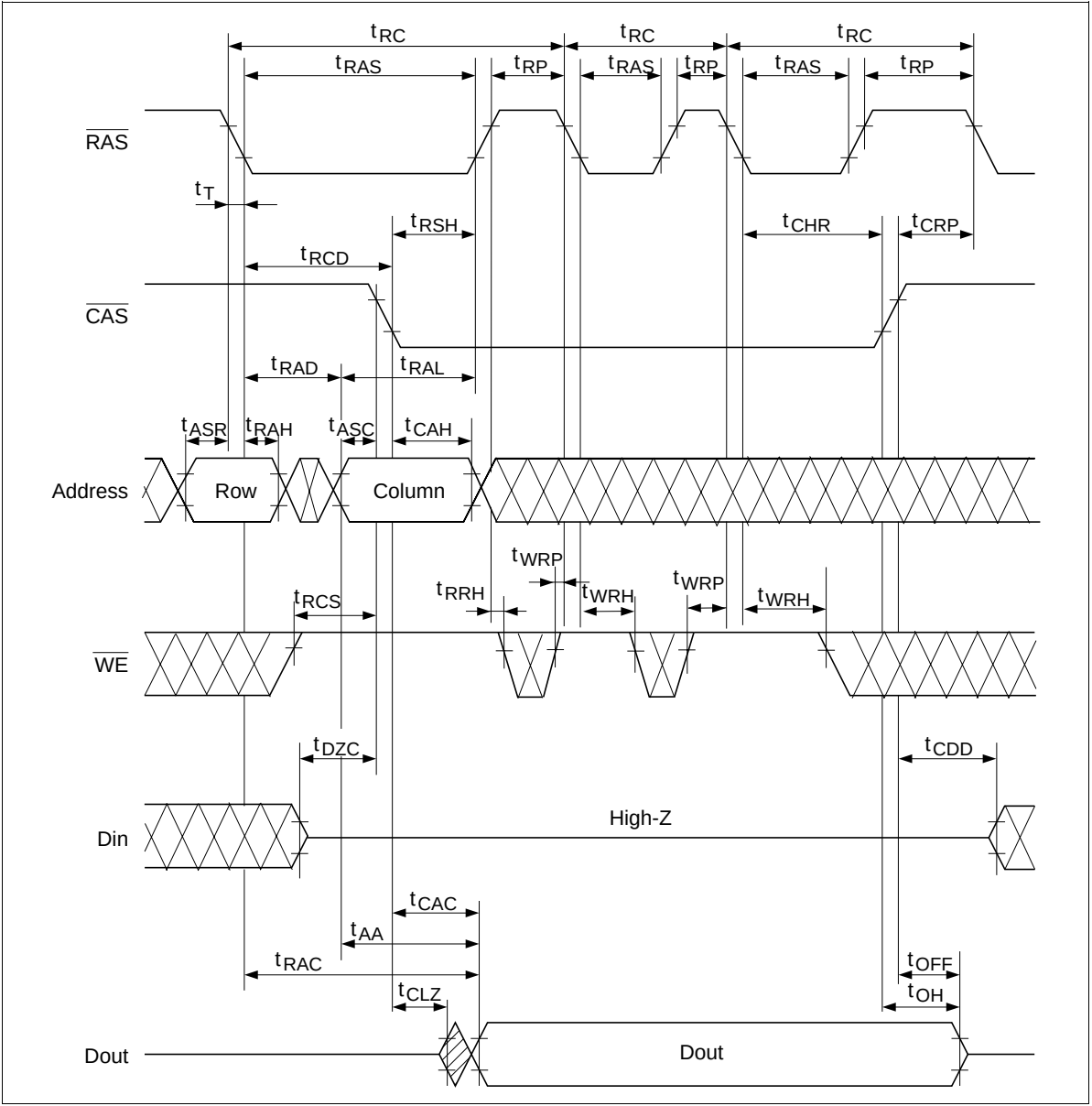
RAS-Only Refresh Cycle



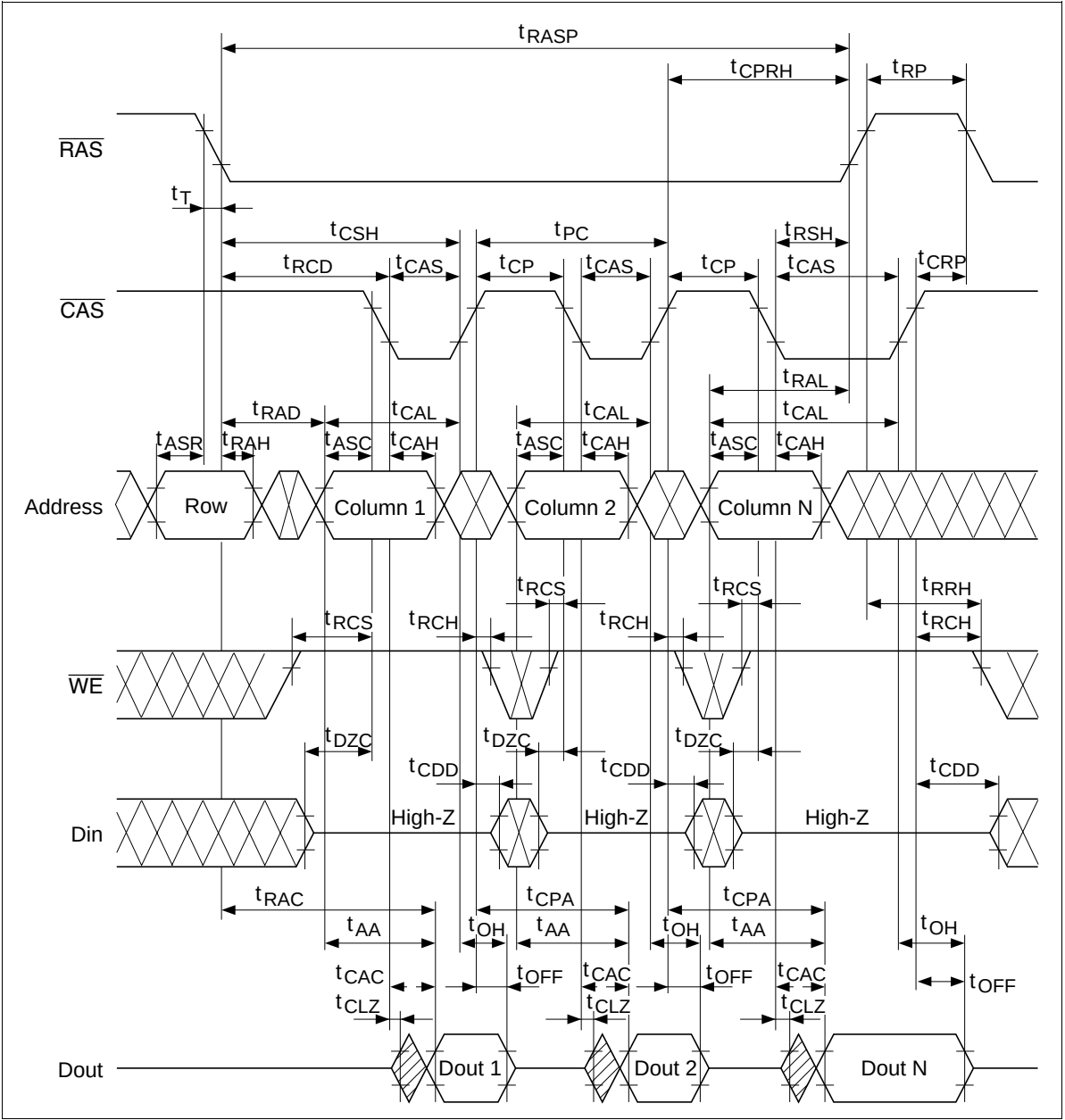
CAS-Before-RAS Refresh Cycle



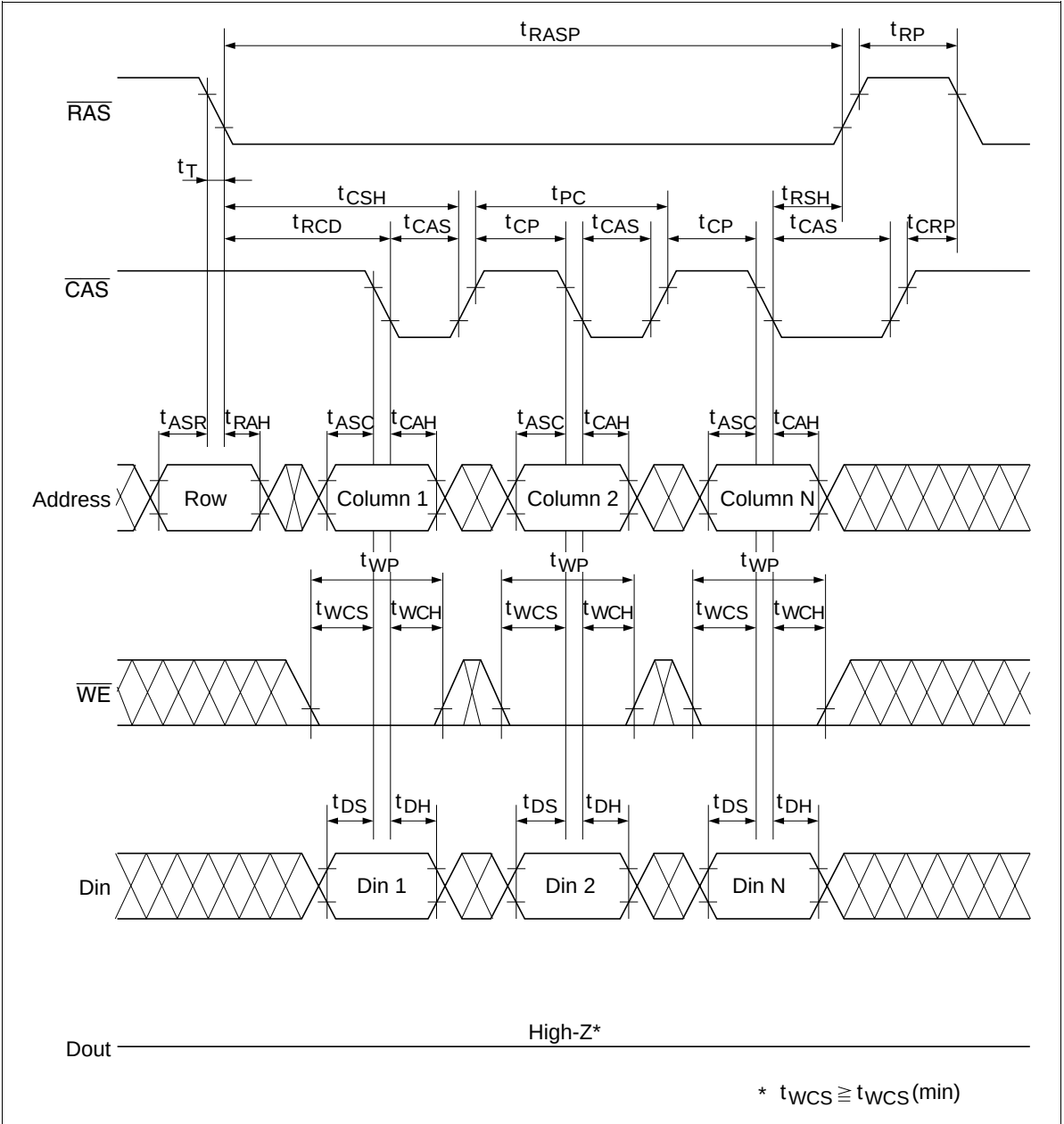
Hidden Refresh Cycle



Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle

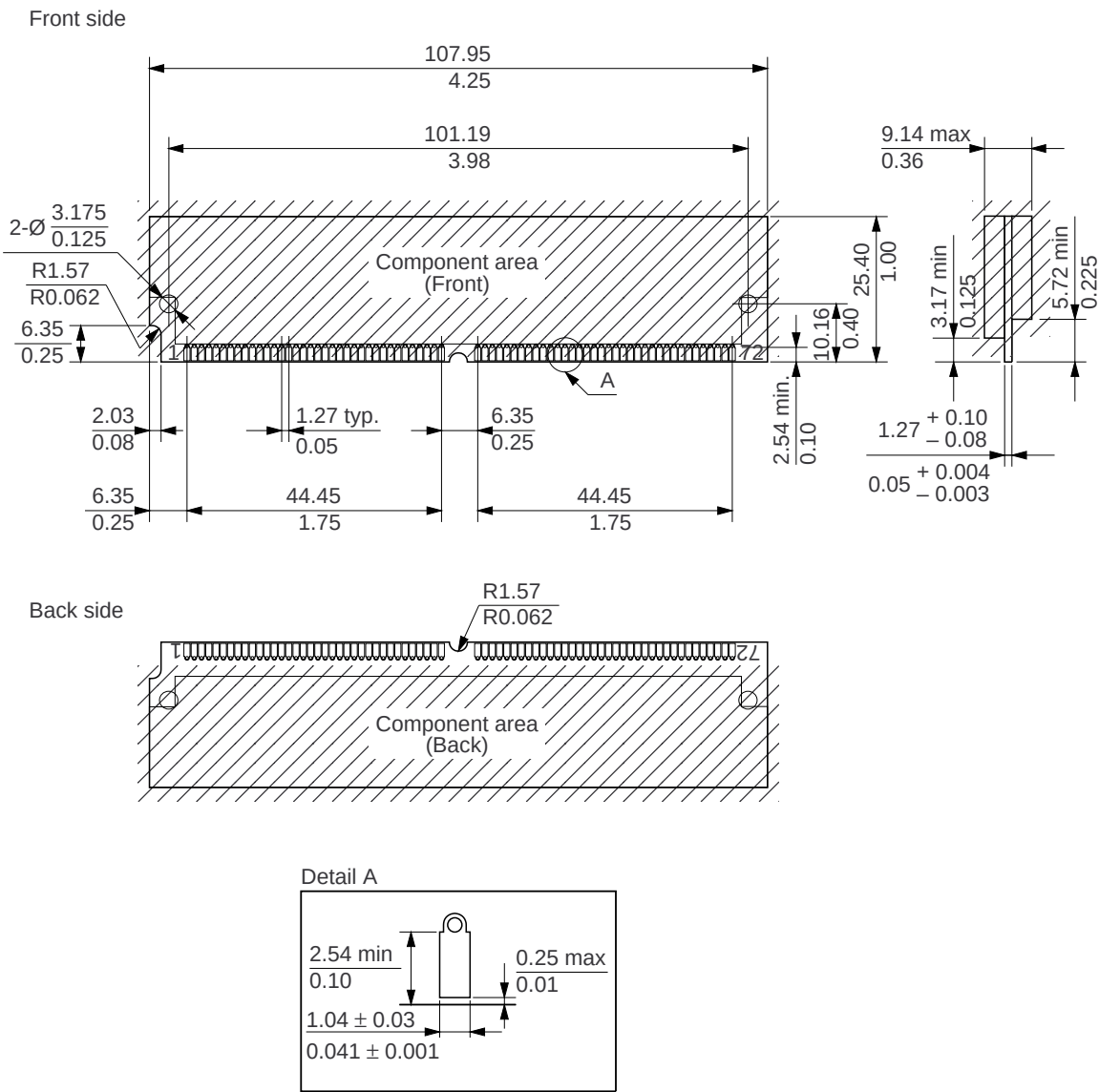


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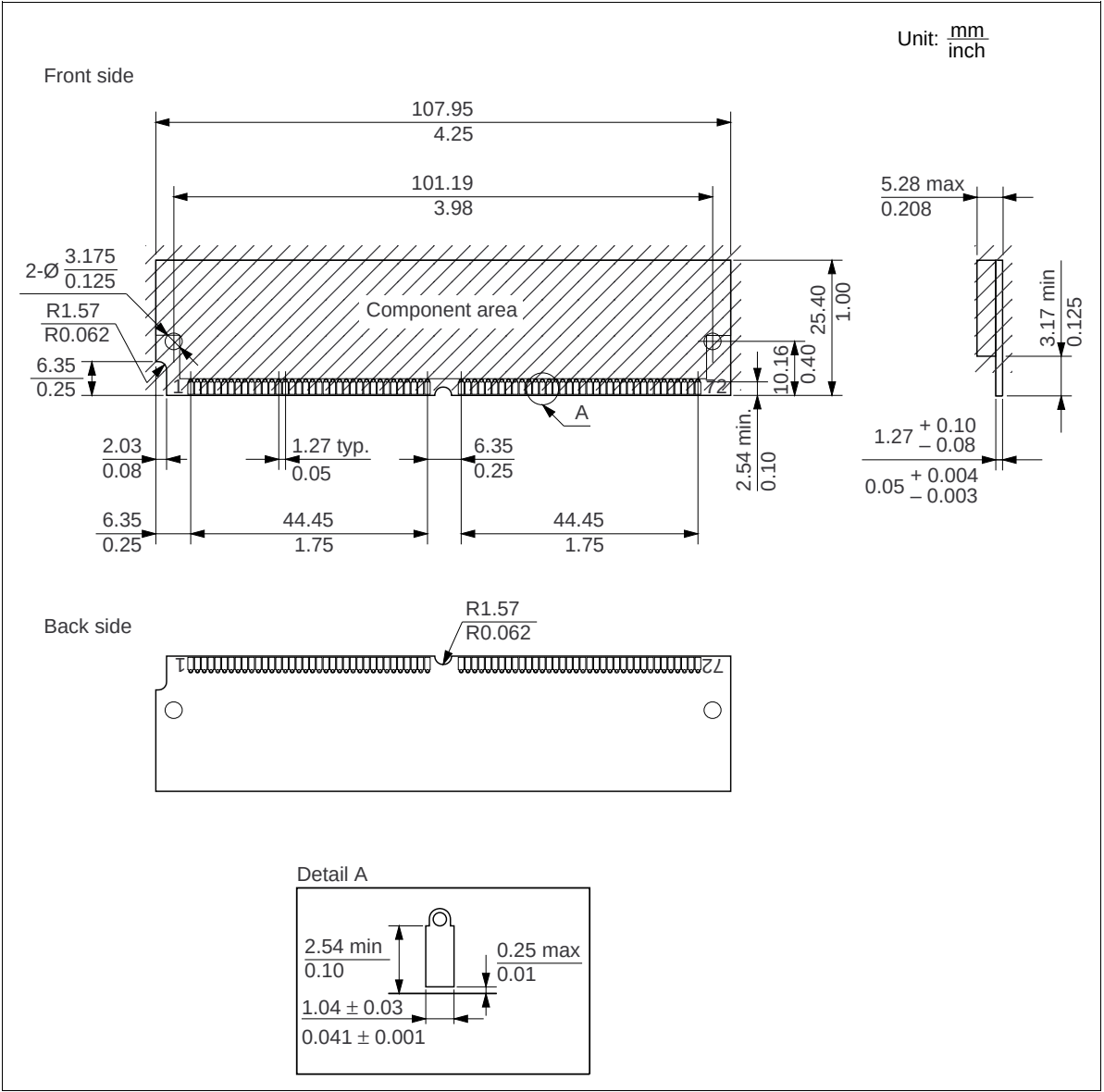
Physical Outline

HB56A832BS/SBS Series

Unit: $\frac{\text{mm}}{\text{inch}}$



HB56A432SBR/SBR Series



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Feb. 20, 1997	Initial issue		
