4AK27

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

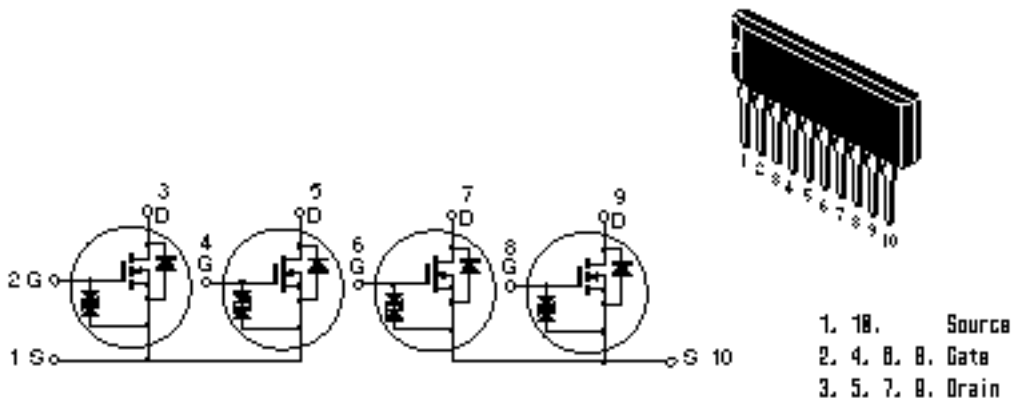
ADE-208-728 (Z)
1st. Edition
January 1999

Features

- Low on-resistance
  $R_{DS(on)} \leq 0.15\Omega$, V_{GS} = 10V, I_D = 3.0A
- 4V gate drive devices.
- High density mounting

Outline

SP-10



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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$ Note1	20	A
Body-drain diode reverse drain current	I_{DR}	5	A
Avalanche current	I_{AP}	5	A
Avalanche energy1	E_{AR}	2.1	mJ
Channel dissipation	Pch(Tc=25˚C) Note2	28	W
Channel dissipation	Pch Note2	4	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

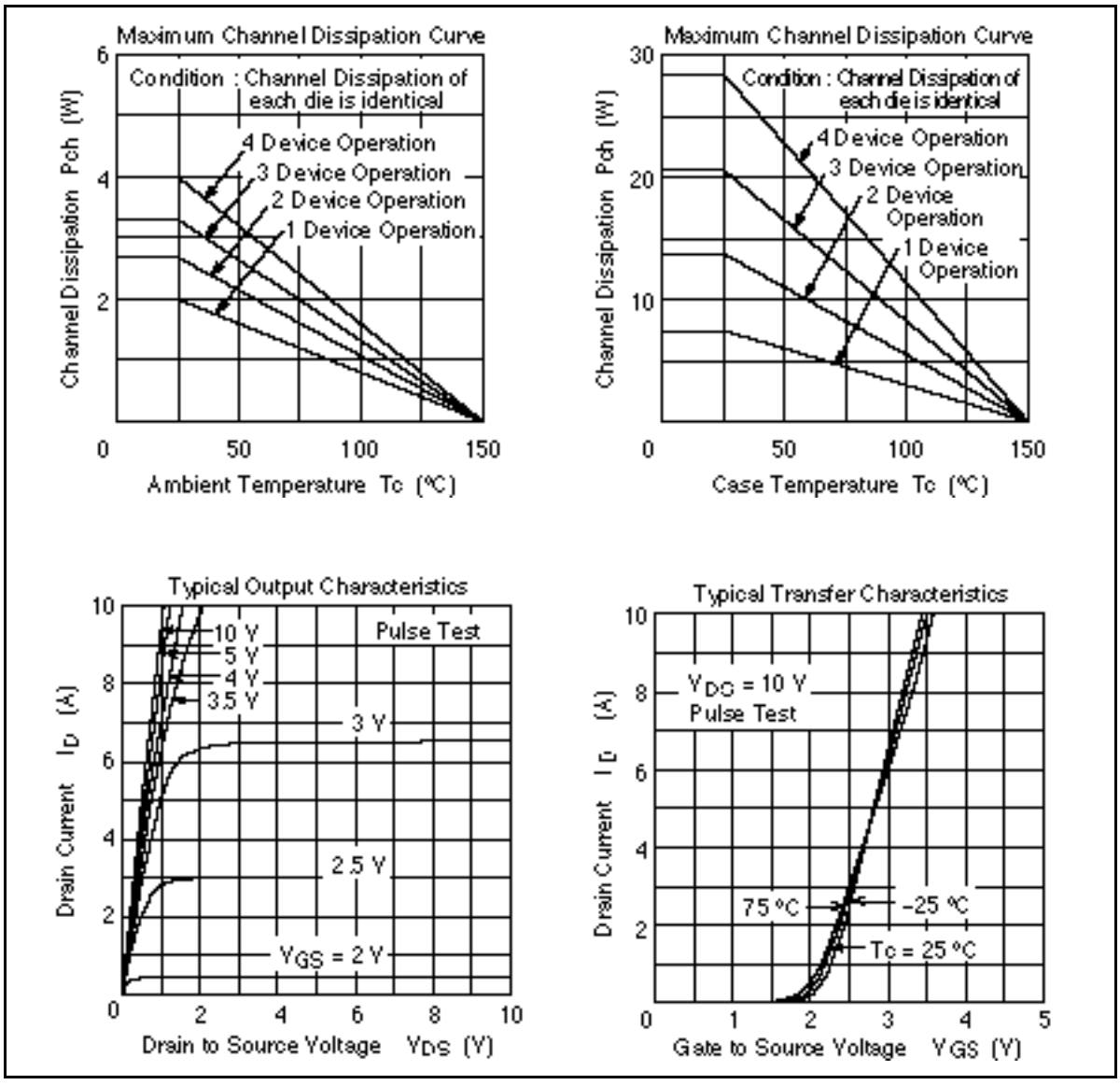
Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. 4 devices poeration
3. Value at Tch=25˚C, Rg ≥ 50Ω

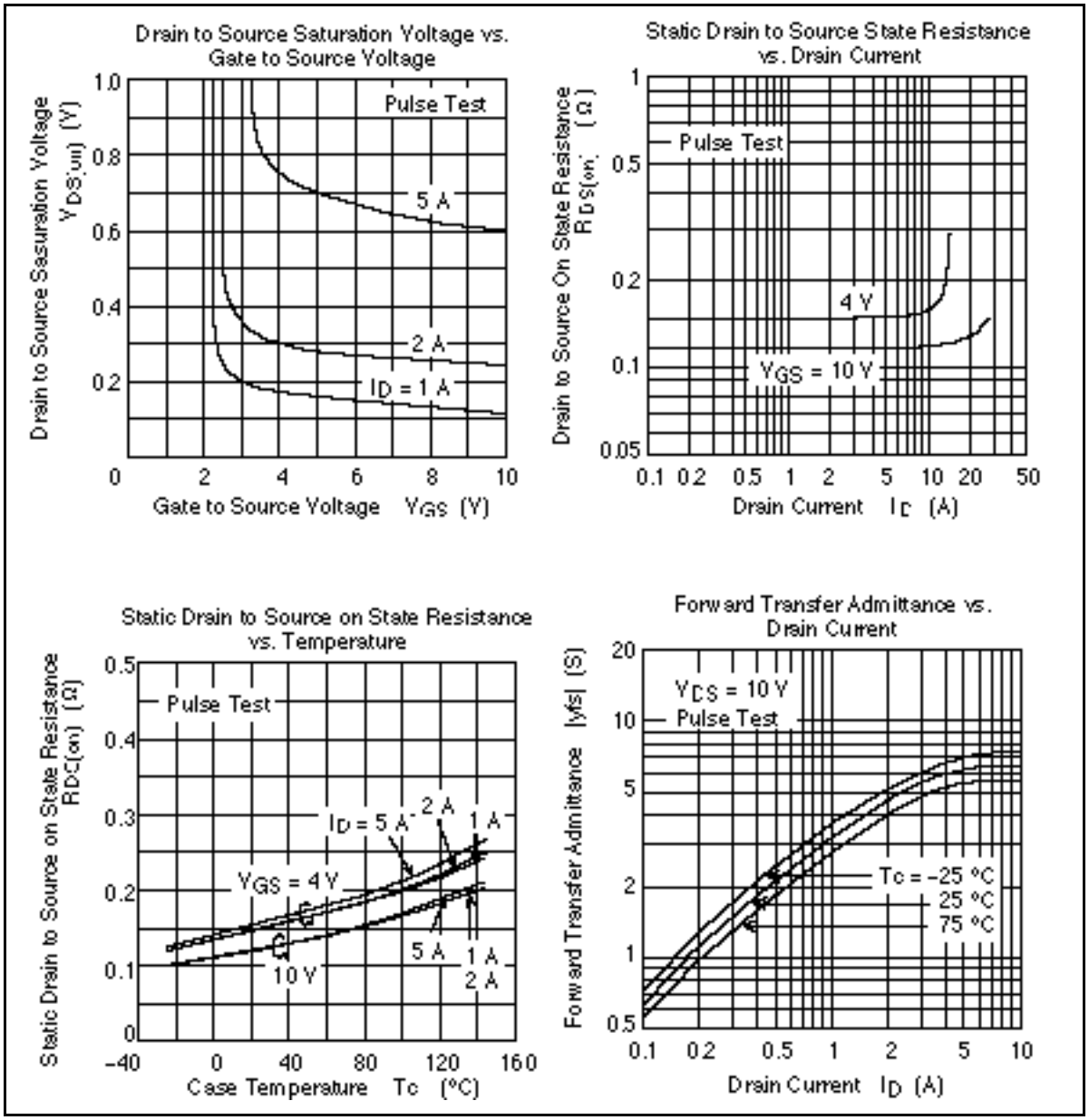
Electrical Characteristics (Ta = 25°C)

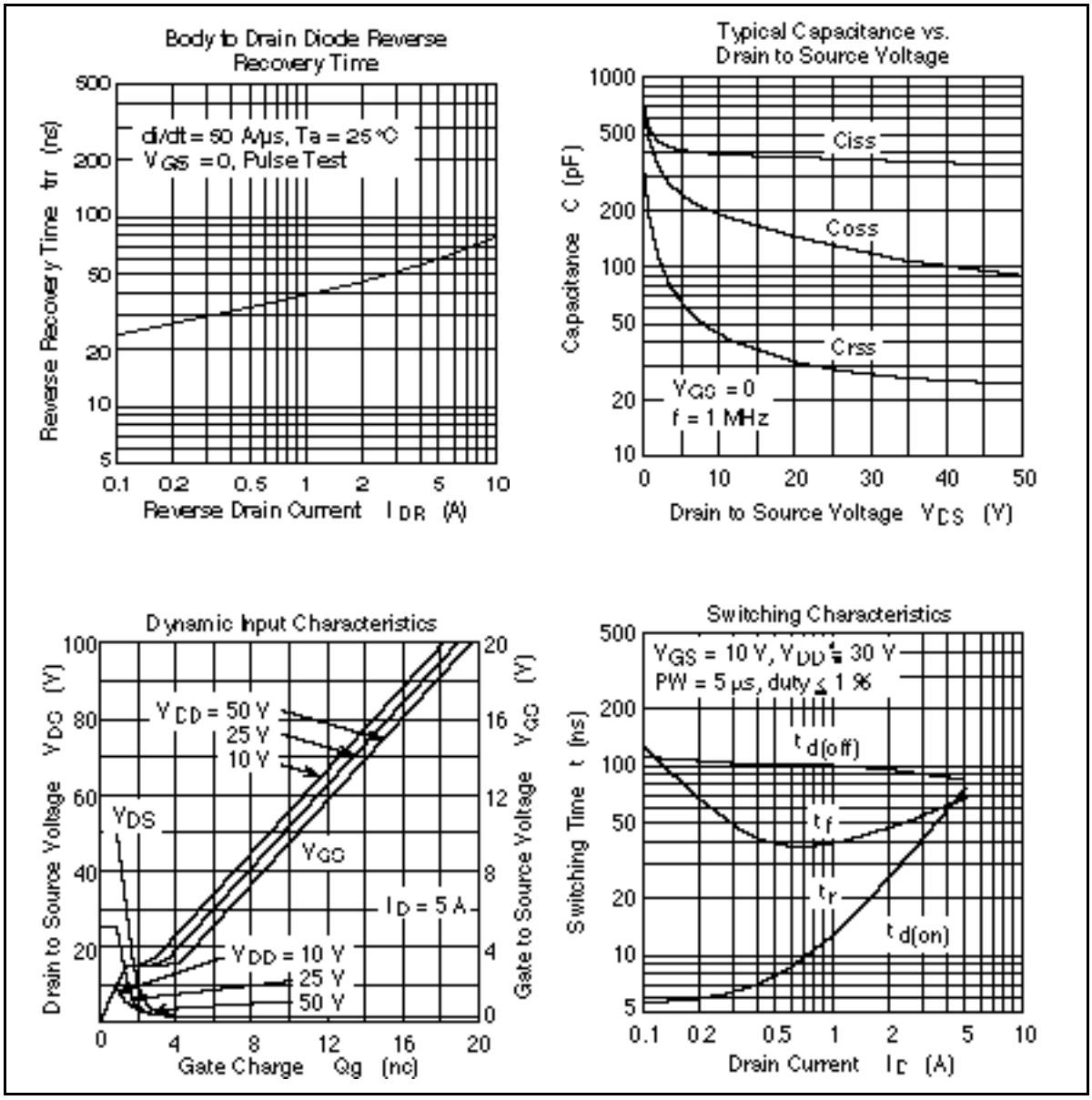
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	100	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.15	Ω	I_D = 3A, V_{GS} = 10V Note4
Static drain to source on state resistance	$R_{DS(on)}$	—	0.15	0.2	Ω	I_D = 3A, V_{GS} = 4V Note4
Forward transfer admittance	$\|y_{fs}\|$	3.0	5.5	—	S	I_D = 3A, V_{DS} = 10V Note4
Input capacitance	Ciss	—	390	—	pF	V_{DS} = 10V
Output capacitance	Coss	—	190	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	45	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = 10V, I_D = 3A
Rise time	t_r	—	42	—	ns	R_L = 10Ω
Turn-off delay time	$t_{d(off)}$	—	90	—	ns	
Fall time	t_f	—	55	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 5A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	60	—	ns	I_F = 5A, V_{GS} = 0 diF/ dt =50A/µs

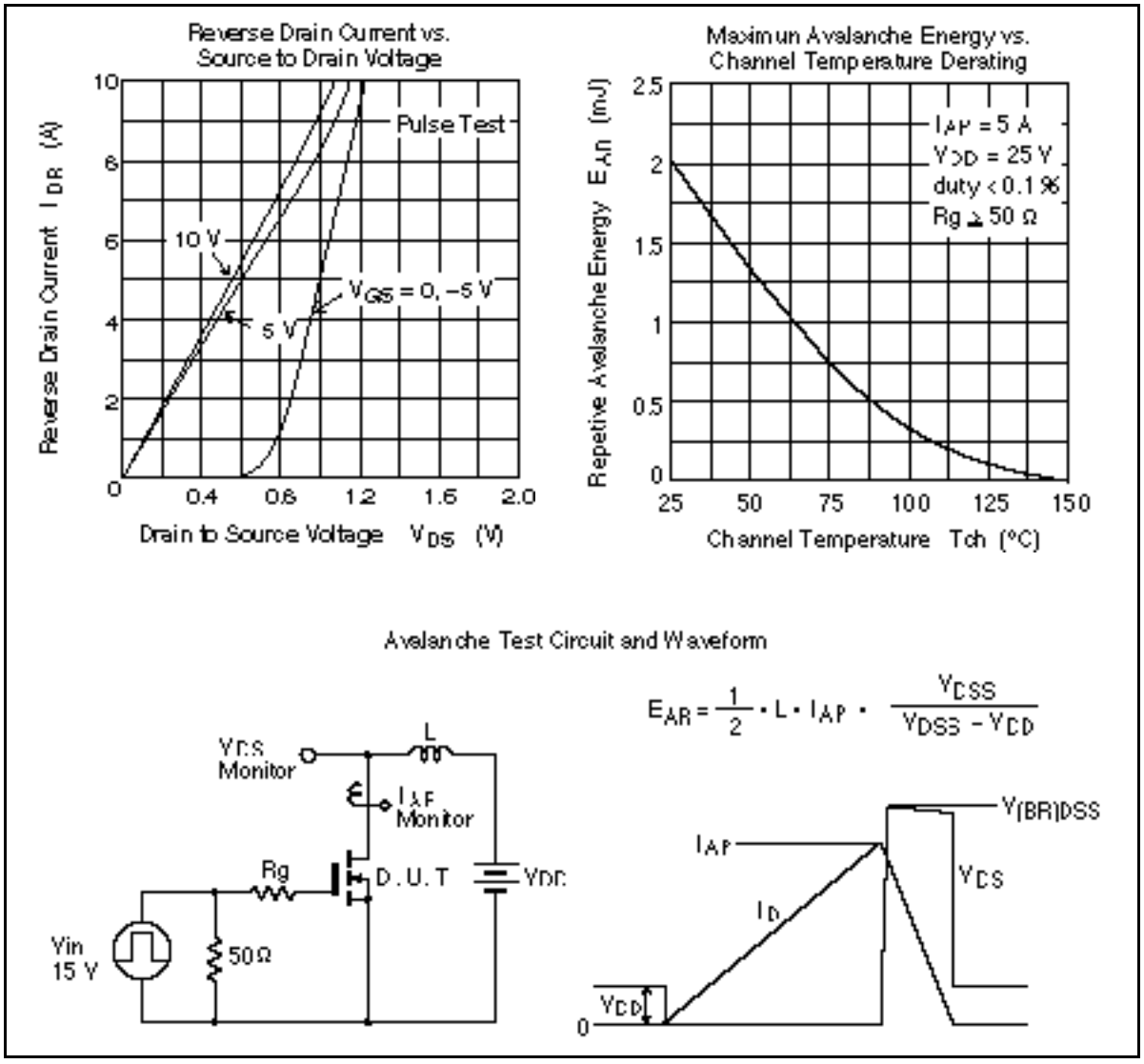
Note: 4. Pulse test

Main Characteristics



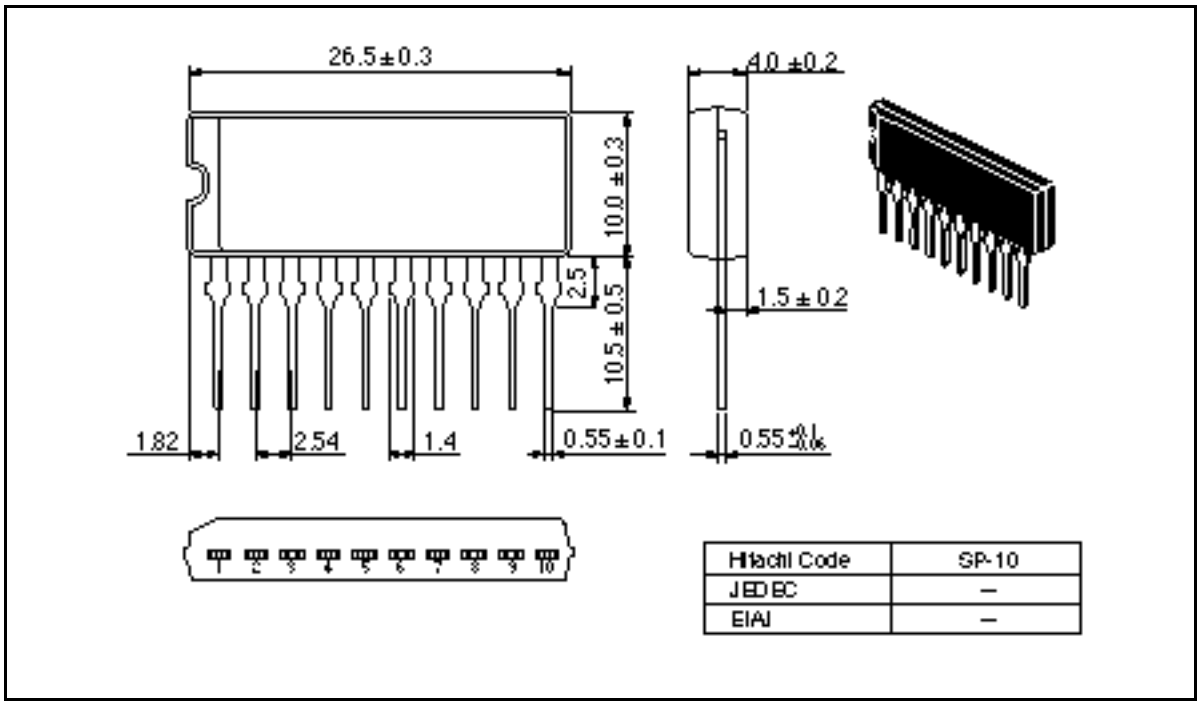

Drain to Source Saturation Voltage vs. Gate to Source Voltage
Drain to Source Sasuration Voltage $V_{DS(sat)}$ (V)
Pulse Test
5 A
2 A
I_D = 1 A
Gate to Source Voltage V_{GS} (V)
Static Drain to Source State Resistance vs. Drain Current
Drain to Source On State Resistance $R_{DS(on)}$ (Ω)
Pulse Test
4 V
V_{GS} = 10 V
Drain Current I_D (A)
Static Drain to Source on State Resistance vs. Temperature
Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)
Pulse Test
I_D = 5 A
2 A
1 A
V_{GS} = 4 V
10 V
5 A
1 A
2 A
Case Temperature Tc (°C)
Forward Transfer Admittance vs. Drain Current
Forward Transfer Admittance |yfs| (S)
V_{DS} = 10 V
Pulse Test
Tc = −25 °C
25 °C
75 °C
Drain Current I_D (A)


Body to Drain Diode Reverse Recovery Time
di/dt = 50 A/µs, Ta = 25°C
VGS = 0, Pulse Test
Reverse Recovery Time trr (ns)
Reverse Drain Current IDR (A)
Typical Capacitance vs. Drain to Source Voltage
Ciss
Coss
Crss
VGS = 0
f = 1 MHz
Capacitance C (pF)
Drain to Source Voltage VDS (V)
Dynamic Input Characteristics
VDD = 50 V
25 V
10 V
VDS
VGS
ID = 5 A
VDD = 10 V
25 V
50 V
Drain to Source Voltage VDS (V)
Gate to Source Voltage VGS (V)
Gate Charge Qg (nc)
Switching Characteristics
VGS = 10 V, VDD = 30 V
PW = 5 µs, duty ≤ 1 %
td(off)
tf
tr
td(on)
Switching Time t (ns)
Drain Current ID (A)


Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I DR (A)
Drain to Source Voltage V DS (V)
Pulse Test
10 V
5 V
V GS = 0, −5 V
Maximun Avalanche Energy vs.
Channel Temperature Derating
Repetive Avalanche Energy E AR (mJ)
Channel Temperature Tch (°C)
I AP = 5 A
V DD = 25 V
duty < 0.1 %
Rg ≧ 50 Ω
Avalanche Test Circuit and Waveform
L
V DS Monitor
I AP Monitor
Rg
D.U.T
V DD
Vin 15 V
50 Ω
E AR = 1/2 · L · I AP · V DSS / (V DSS − V DD)
V (BR)DSS
I AP
I D
V DS
V DD
0

Package Dimensions

Unit: mm



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HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1897
Tel: <1> (800) 285-1601
Fax: <1> (303) 297-0447

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITECHX