

SERIAL ACCESS EXTENDED ADDRESSING COMPATIBLE WITH I²C BUS 32K (4K x 8) EEPROM

BRIEF DATA

- COMPATIBLE WITH I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES, OVER THE FULL SUPPLY VOLTAGE RANGE
- 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
 - 4.5V to 5.5V FOR THE ST14E32F
 - 2.7V to 5.5V FOR THE ST15E32F
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (UP TO 32 BYTES)
- BYTE, RANDOM AND SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

Figure 1 Delivery forms

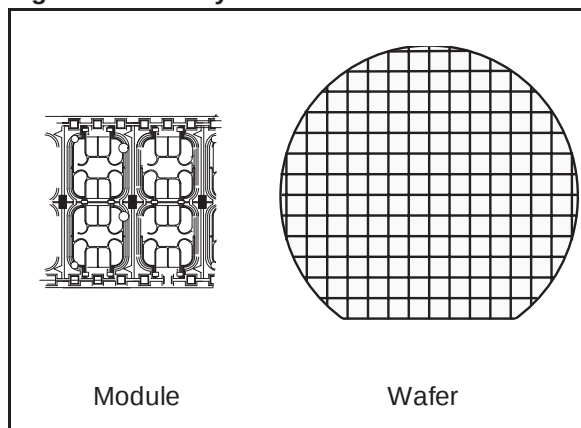


Figure 2 Pin Connection

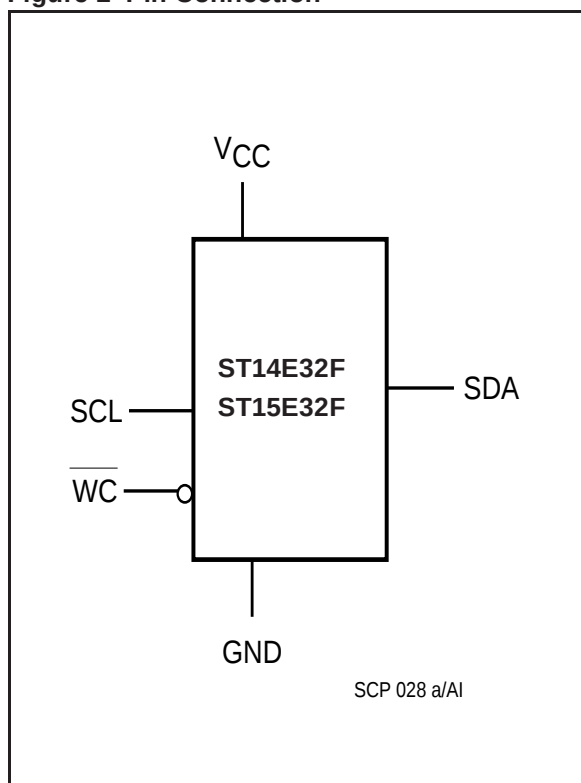


Table 1 Signal Names

SDA	Serial Data Address Input Output
SCL	Serial Clock
WC	Write Control
VCC	Supply Voltage
GND	Ground

DESCRIPTION

The ST14/15E32F are 32K bit electrically erasable programmable memory products (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST15E32F circuit operates with a power supply value as low as 2.7V.

The ST14/15E32F are compatible with the I²C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock.

The ST14/15E32F carry a built-in 4 bit, unique device identification code (1010) corresponding to the I²C bus definition. The ST14/15E32F behave as a slave device in the I²C protocol with all memory operations synchronized by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master.

The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Both wafers (sawn or unsawn) and micromodules (on film) are available.

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