

2SK543

T-31-25

2024A

N-Channel MOS Silicon FET

**FM Tuner, VHF-Band
Amp Applications**

©1791C

Features

- Low noise. $NF=1.8\text{dB typ}(f=100\text{MHz})$
- High power gain. $PG=27\text{dB typ}(f=100\text{MHz})$
- Small reverse transfer capacitance. $c_{rss}=0.035\text{pF}(V_{DS}=10\text{V}, f=1\text{MHz})$

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

			unit
Drain to Source Voltage	V_{DS}	20	V
Gate to Source Voltage	V_{GS}	± 5	V
Drain Current	I_D	30	mA
Allowable Power Dissipation	P_D	200	mW
Channel Temperature	T_{ch}	125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Electrical Characteristics at $T_a=25^\circ\text{C}$

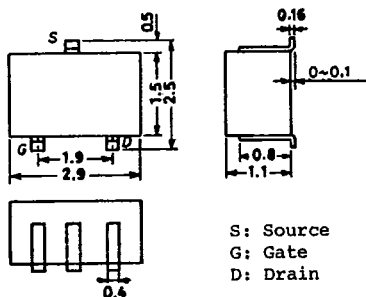
			min	typ	max	unit
Drain to Source Voltage	V_{DSX}	$V_{GS}=-4\text{V}, I_D=100\mu\text{A}$	20			V
Common Source Gate Cutoff Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 5\text{V}$			10	nA
Drain Current	I_{DSS}	$V_{DS}=10\text{V}, V_{GS}=0\text{V}$	1.2*		12*	mA
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=10\text{V}, I_D=100\mu\text{A}$			-2.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=10\text{V}, V_{GS}=0\text{V}$ $f=1\text{kHz}$		11		mS
Input Capacitance	c_{iss}	$V_{DS}=10\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		2.4		pF
Reverse Transfer Capacitance	c_{rss}	$V_{DS}=10\text{V}, V_{GS}=0\text{V}$ $f=100\text{MHz}$		0.035		pF
Power Gain	PG	$V_{DS}=10\text{V}, V_{GS}=0\text{V}$ $f=100\text{MHz}$		27		dB
Noise Figure	NF	$f=100\text{MHz}$		1.8	3.0	dB

See specified Test Circuit.

*: The 2SK543 is classified by I_{DSS} as follows (unit: mA):

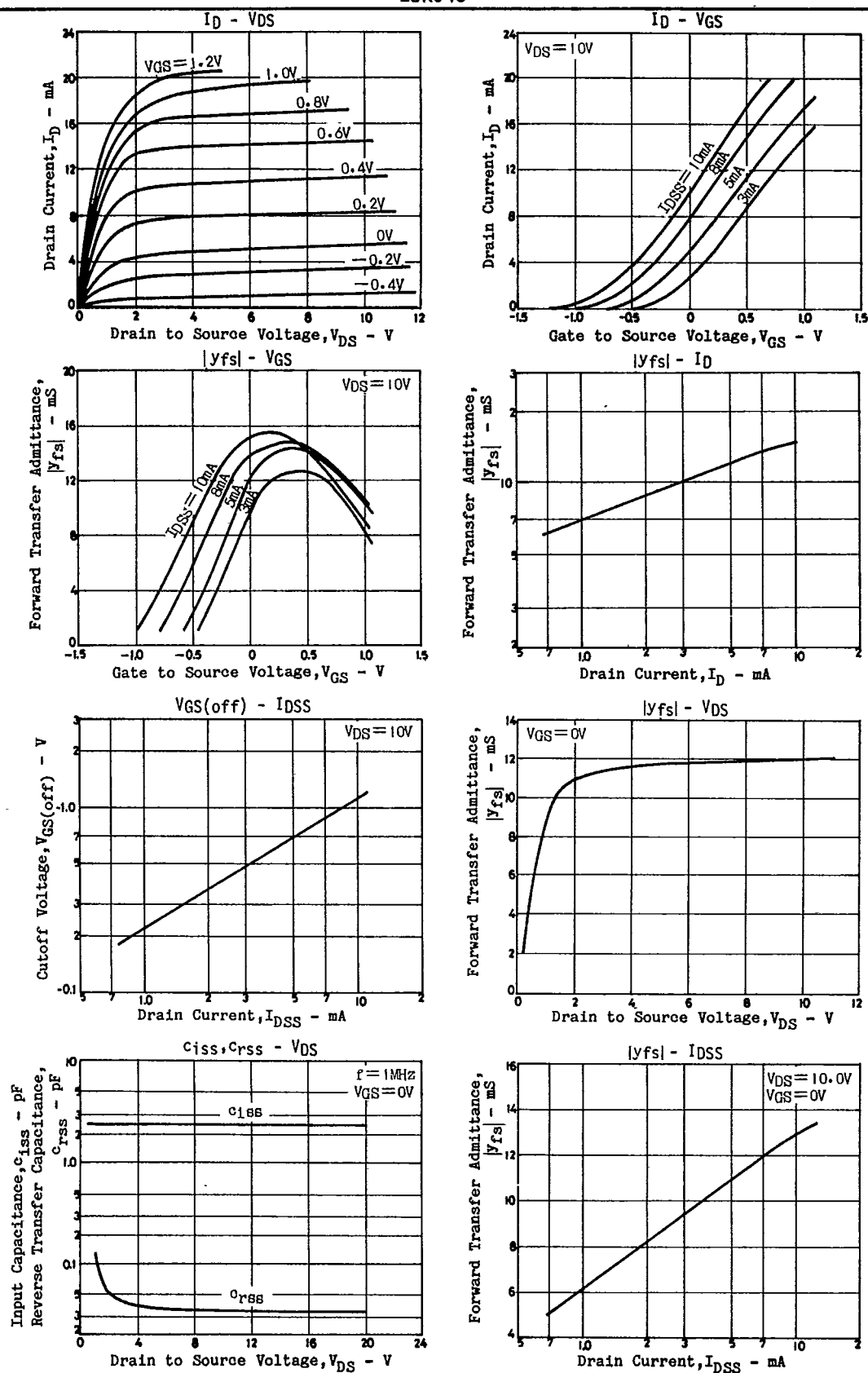
1.2	3	3.0	2.5	4	6.0	5.0	5	12
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(Note) Marking :CJ

 I_{DSS} rank: 3,4,5**Case Outline 2024A**
(unit:mm)S: Source
G: Gate
D: Drain

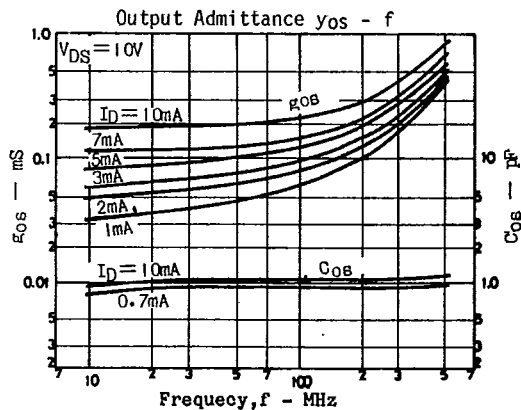
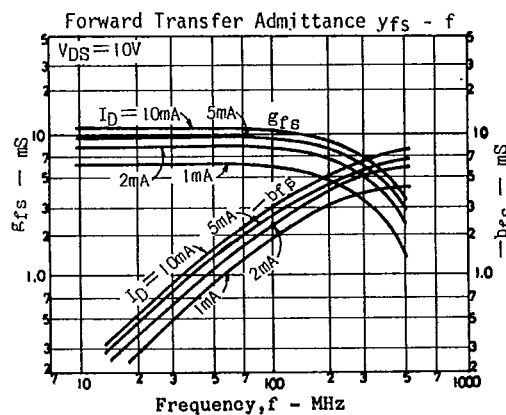
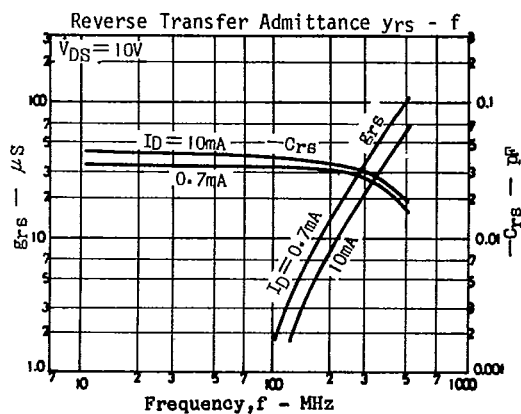
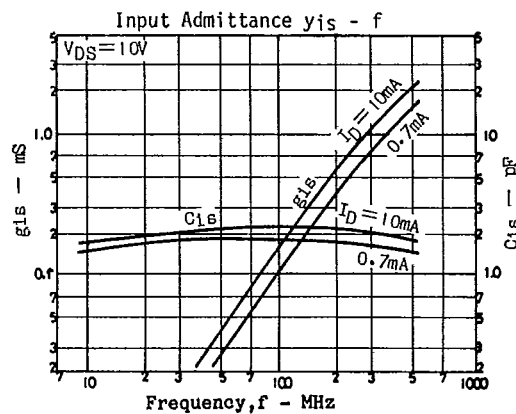
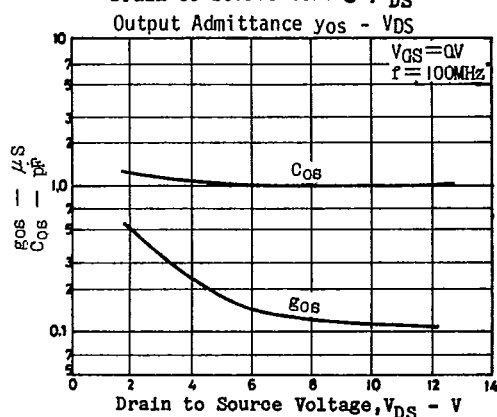
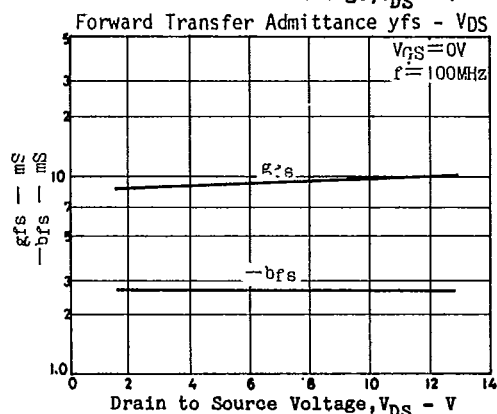
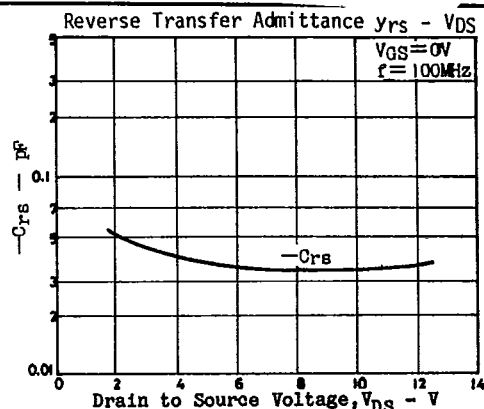
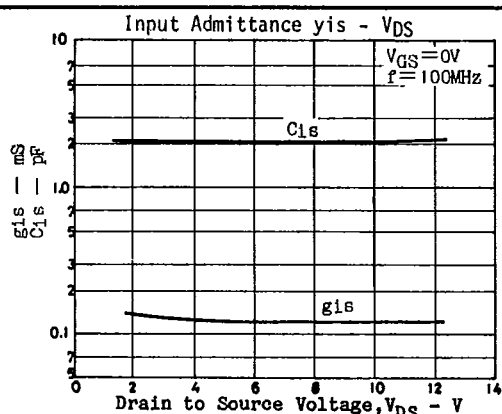
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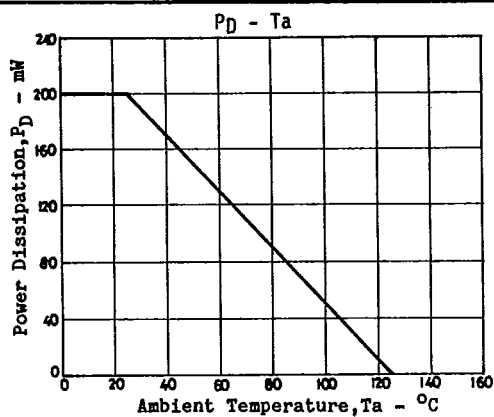
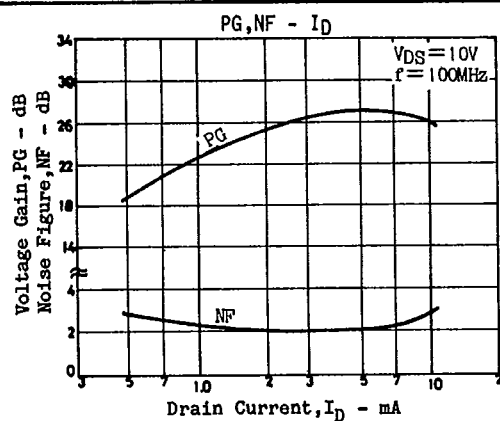
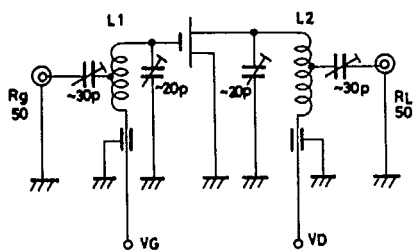
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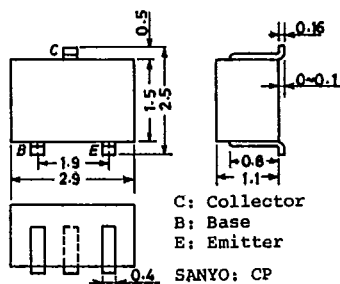
**PG, NF Test Circuit**L1: 1mm ϕ plated wire 10mm ϕ 6T, tap: 3T from H sideL2: 1mm ϕ plated wire 10mm ϕ 7T, tap: 4T from H side

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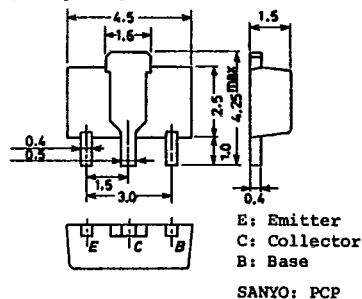
CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

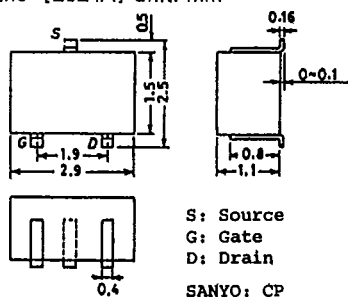
Case Outline—[2018A] unit: mm



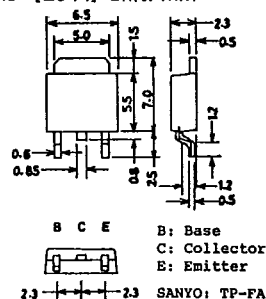
Case Outline—[2038] unit: mm



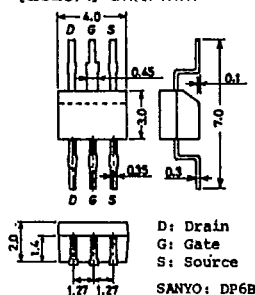
Case Outline—[2024A] unit: mm



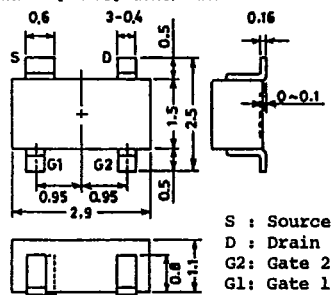
Case Outline—[2044] unit: mm



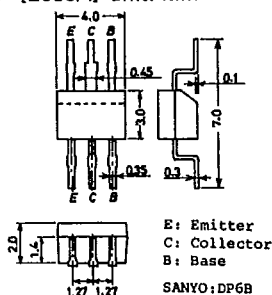
Case Outline—[2028A] unit: mm



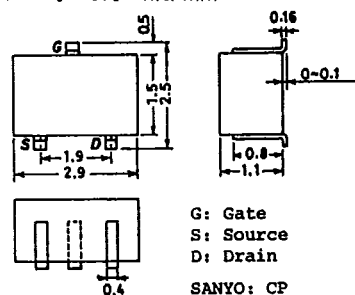
Case Outline—[2046] unit: mm



Case Outline—[2030A] unit: mm

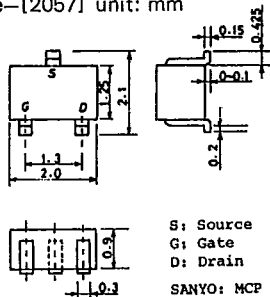


Case Outline—[2050] unit: mm

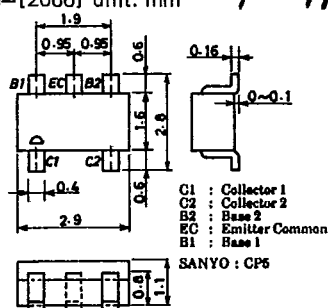


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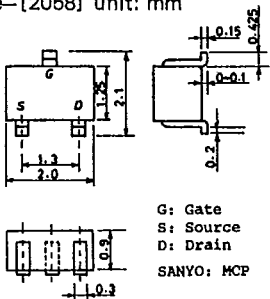
Case Outline—[2057] unit: mm



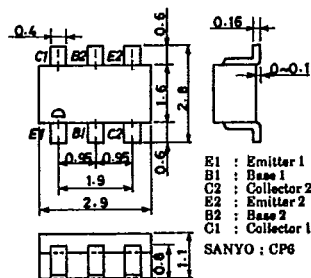
Case Outline—[2066] unit: mm



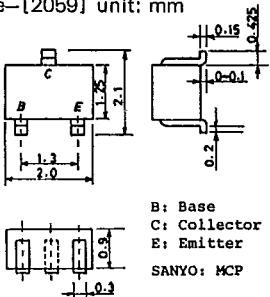
Case Outline—[2058] unit: mm



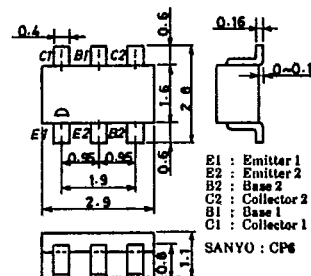
Case Outline—[2067] unit: mm



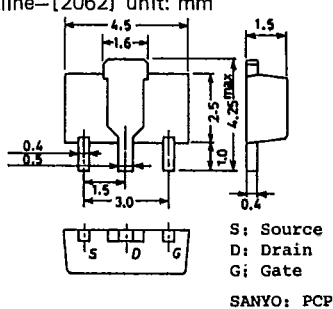
Case Outline—[2059] unit: mm



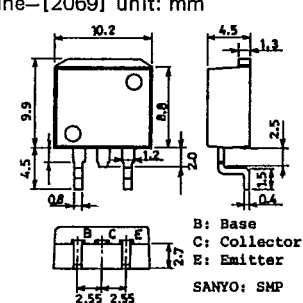
Case Outline—[2068] unit: mm



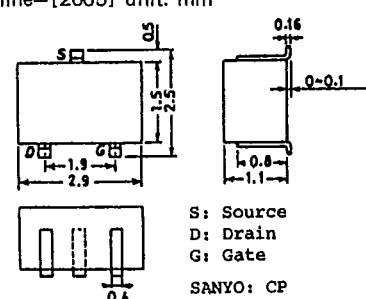
Case Outline—[2062] unit: mm



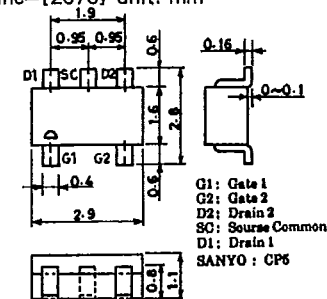
Case Outline—[2069] unit: mm



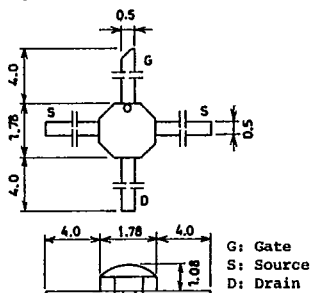
Case Outline—[2065] unit: mm



Case Outline—[2070] unit: mm

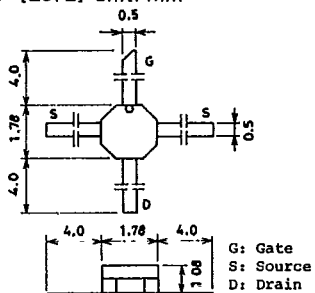


Case Outline—[2071] unit: mm



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Case Outline—[2072] unit: mm



Case Outline—[2073] unit: mm

