2SJ556

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

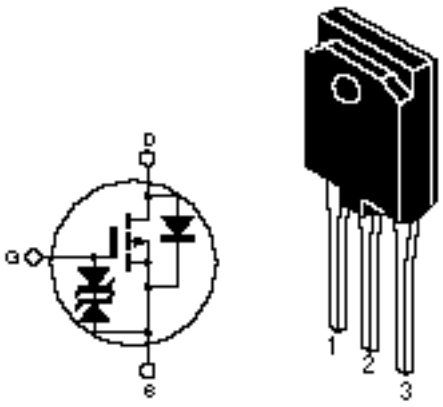
ADE-208-645A (Z)
2nd. Edition
Jun 1998

Features

- Low on-resistance
  $R_{DS(on)}$ = 0.028Ω typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

TO-3PFM



1. Gate
2. Drain
3. Source

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–45	A
Drain peak current	$I_{D(pulse)}$ Note1	–180	A
Body-drain diode reverse drain current	I_{DR}	–45	A
Avalanche current	I_{AP} Note3	–45	A
Avalanche energy	E_{AR} Note3	173	mJ
Channel dissipation	Pch Note2	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

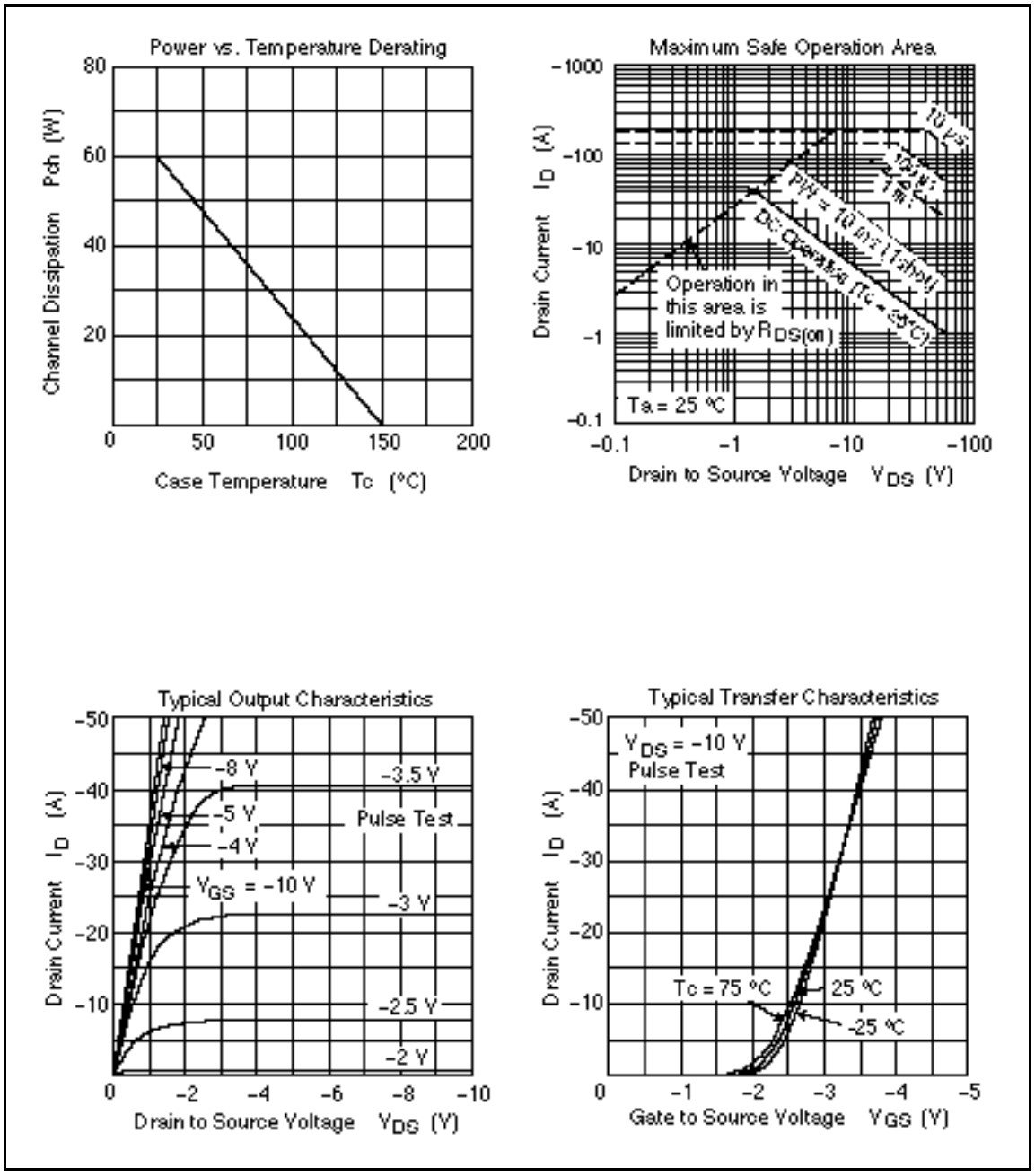
Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

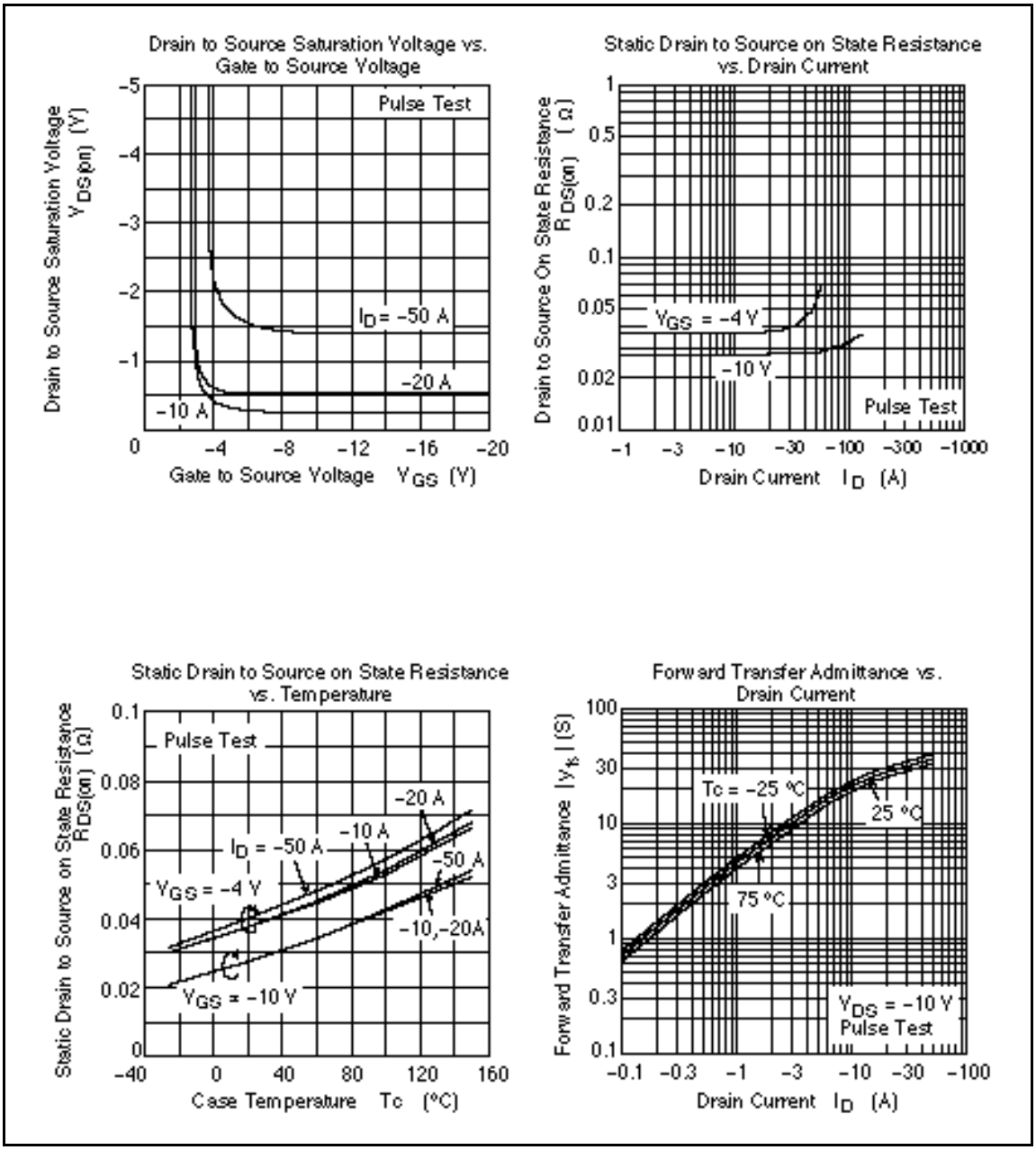
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100µA, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.0	V	I_D = –1mA, V_{DS} = –10V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.028	0.037	Ω	I_D = –25A, V_{GS} = –10V Note4
	$R_{DS(on)}$	—	0.038	0.055	Ω	I_D = –25A, V_{GS} = –4V Note4
Forward transfer admittance	$\|y_{fs}\|$	18	30	—	S	I_D = –25A, V_{DS} = –10V Note4
Input capacitance	Ciss	—	2500	—	pF	V_{DS} = –10V
Output capacitance	Coss	—	1300	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	V_{GS} = –10V, I_D = –25A
Rise time	t_r	—	160	—	ns	R_L = 1.2Ω
Turn-off delay time	$t_{d(off)}$	—	350	—	ns	
Fall time	t_f	—	240	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–1.1	—	V	I_F = –45A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = –45A, V_{GS} = 0 diF/ dt =50A/µs

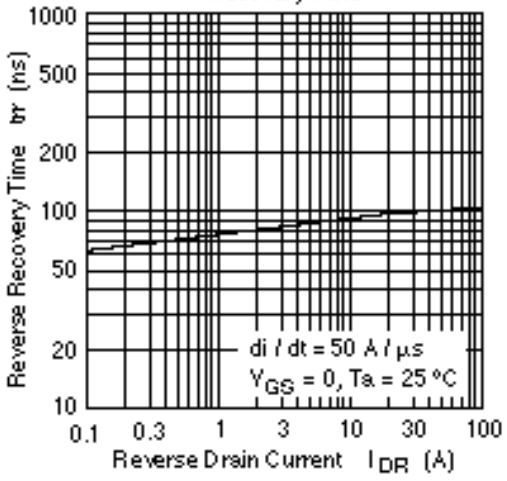
Note: 4. Pulse test

Main Characteristics

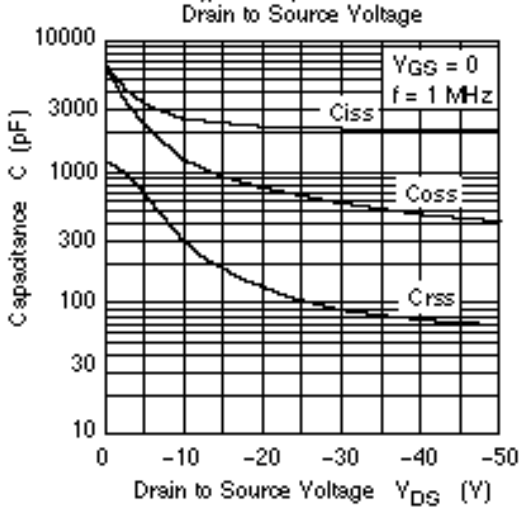



Drain to Source Saturation Voltage vs. Gate to Source Voltage
Drain to Source Saturation Voltage $V_{DS(on)}$ (V)
Pulse Test
I_D = −50 A
−20 A
−10 A
Gate to Source Voltage V_{GS} (V)
Static Drain to Source on State Resistance vs. Drain Current
Drain to Source On State Resistance $R_{DS(on)}$ (Ω)
V_{GS} = −4 V
−10 V
Pulse Test
Drain Current I_D (A)
Static Drain to Source on State Resistance vs. Temperature
Static Drain to Source on State Resistance $R_{DS(on)}$ (Ω)
Pulse Test
−20 A
−10 A
I_D = −50 A
−50 A
V_{GS} = −4 V
−10, −20A
V_{GS} = −10 V
Case Temperature Tc (°C)
Forward Transfer Admittance vs. Drain Current
Forward Transfer Admittance $|y_{fs}|$ (S)
Tc = −25 °C
25 °C
75 °C
V_{DS} = −10 V
Pulse Test
Drain Current I_D (A)

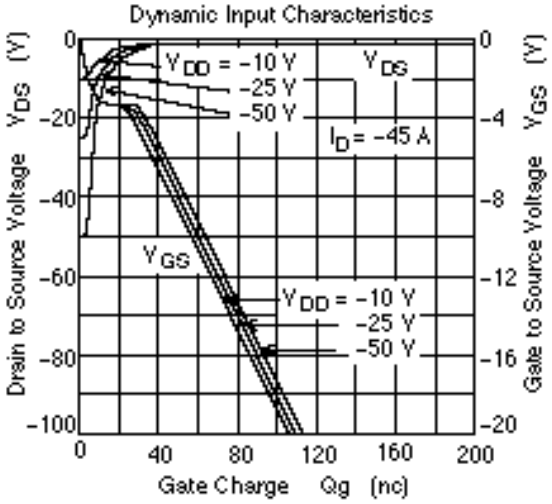
Body-Drain Diode Reverse Recovery Time



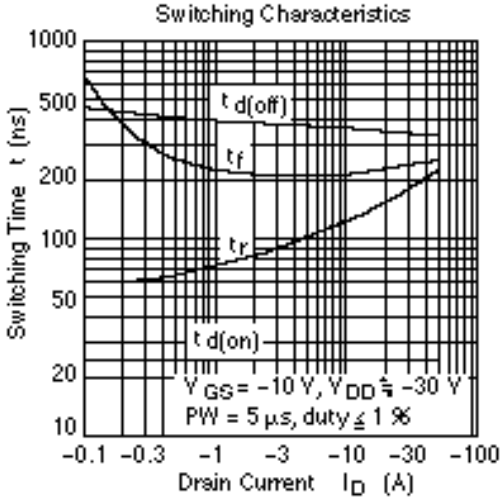
Typical Capacitance vs. Drain to Source Voltage



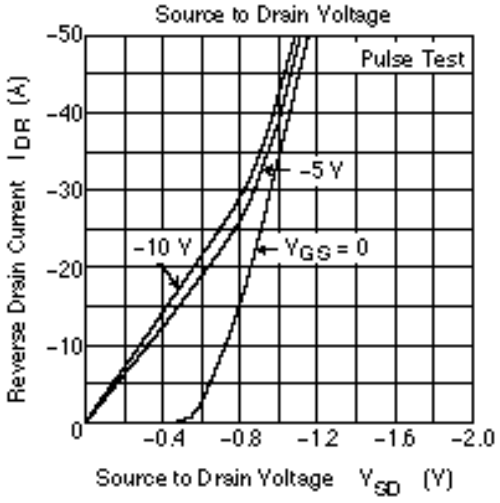
Dynamic Input Characteristics



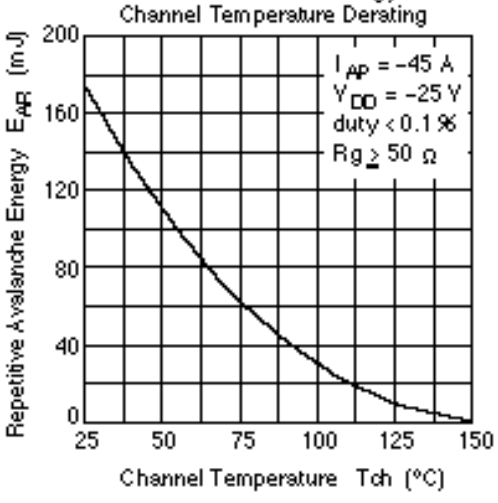
Switching Characteristics



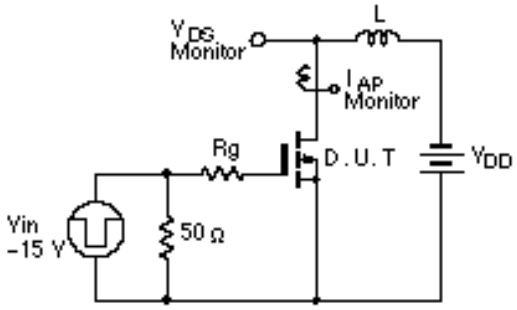
Reverse Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

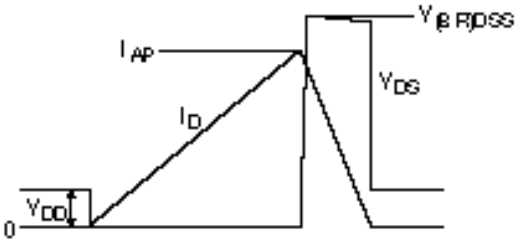


Avalanche Test Circuit

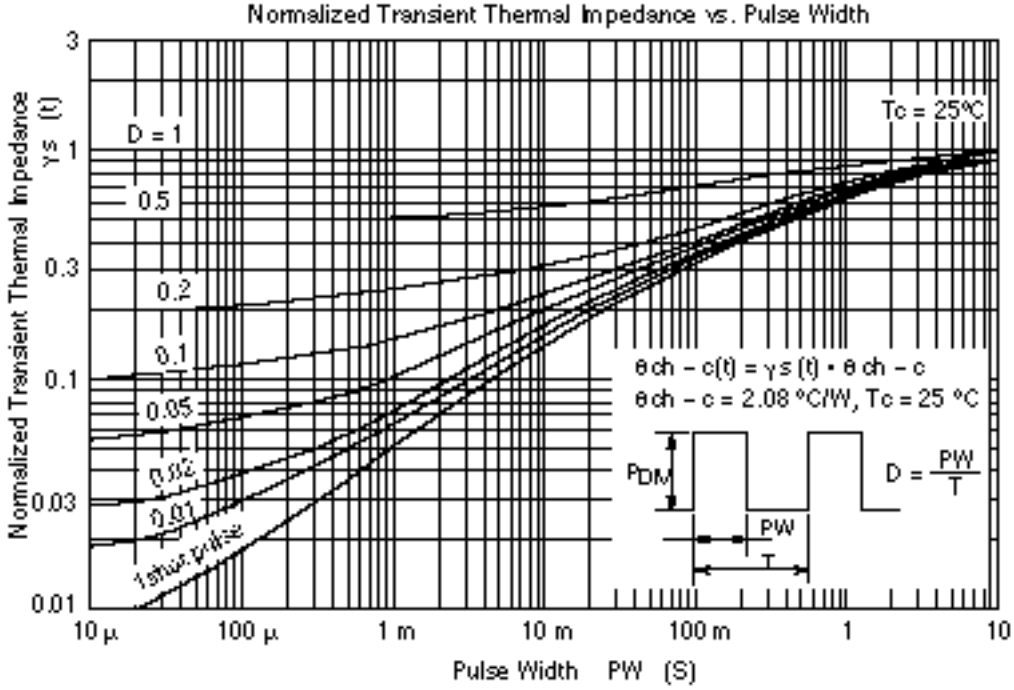


Avalanche Waveform

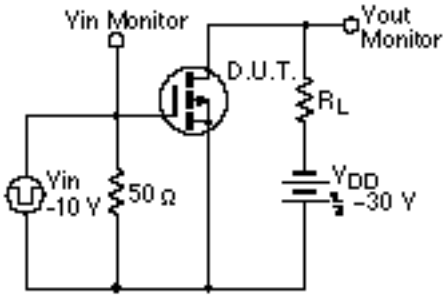
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



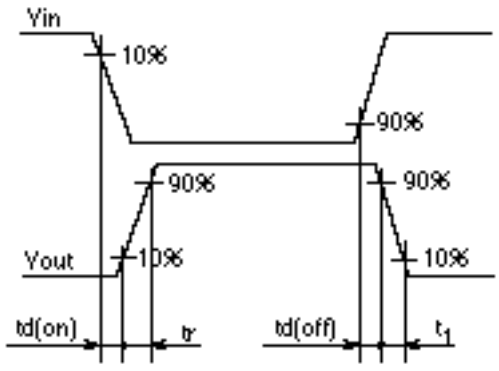
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

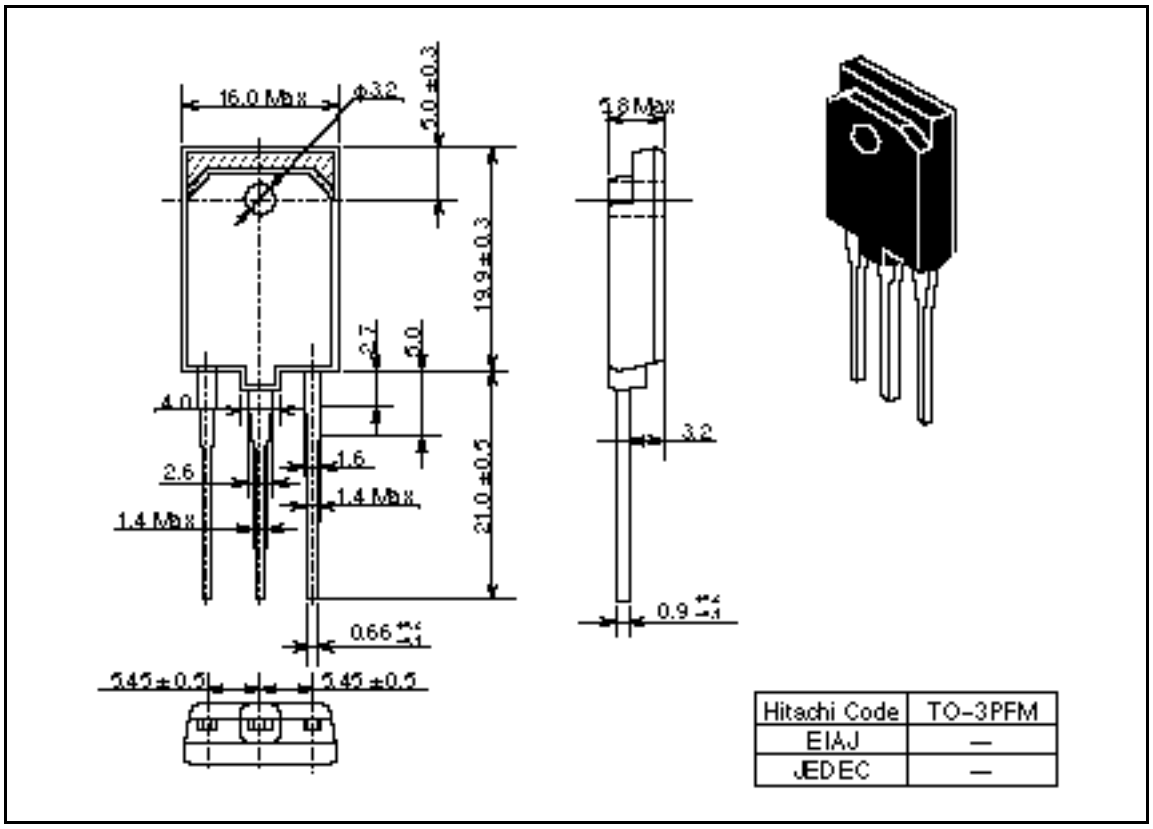


Waveform



Package Dimensions

Unit: mm



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